

256K x 16 Low Power SRAM

Preliminary, Rev 1.6 Dec/2007

Features

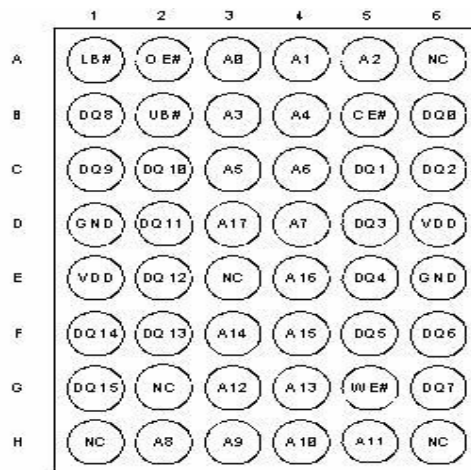
- Single power supply voltage of 2.7V to 3.6V
- Power down features using CE#
- Low power dissipation
- Data retention supply voltage: 1.5V to 3.6V
- Direct TTL compatibility for all input and output
- Wide operating temperature range: -40°C to 85°C
- Standby current @ VDD = 3.6 V

Ordering Information

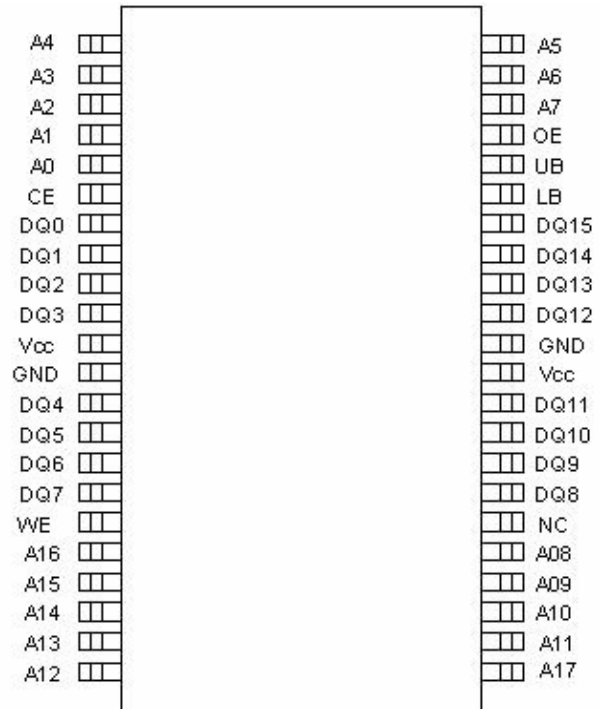
Part Number	Speed	Ibbs2	Package
EM564166BC/TS-55G	55 ns	35μA	48-Ball BGA
EM564166BC/TS-70G	70 ns	35 μA	44-L TSOP
EM564166BC/TS-85G	85 ns	35 μA	

Pin Configuration

48-Ball BGA (CSP), Top View



44-L TSOP II, Top View



Pin Description

Symbol	Function
A0 - A17	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
CE#	Chip Enable Inputs
OE#	Output Enable
WE#	Read / Write Control Input
LB#, UB#	Data Byte Control Inputs
GND	Ground
VDD	Power Supply
NC	No Connection

Overview

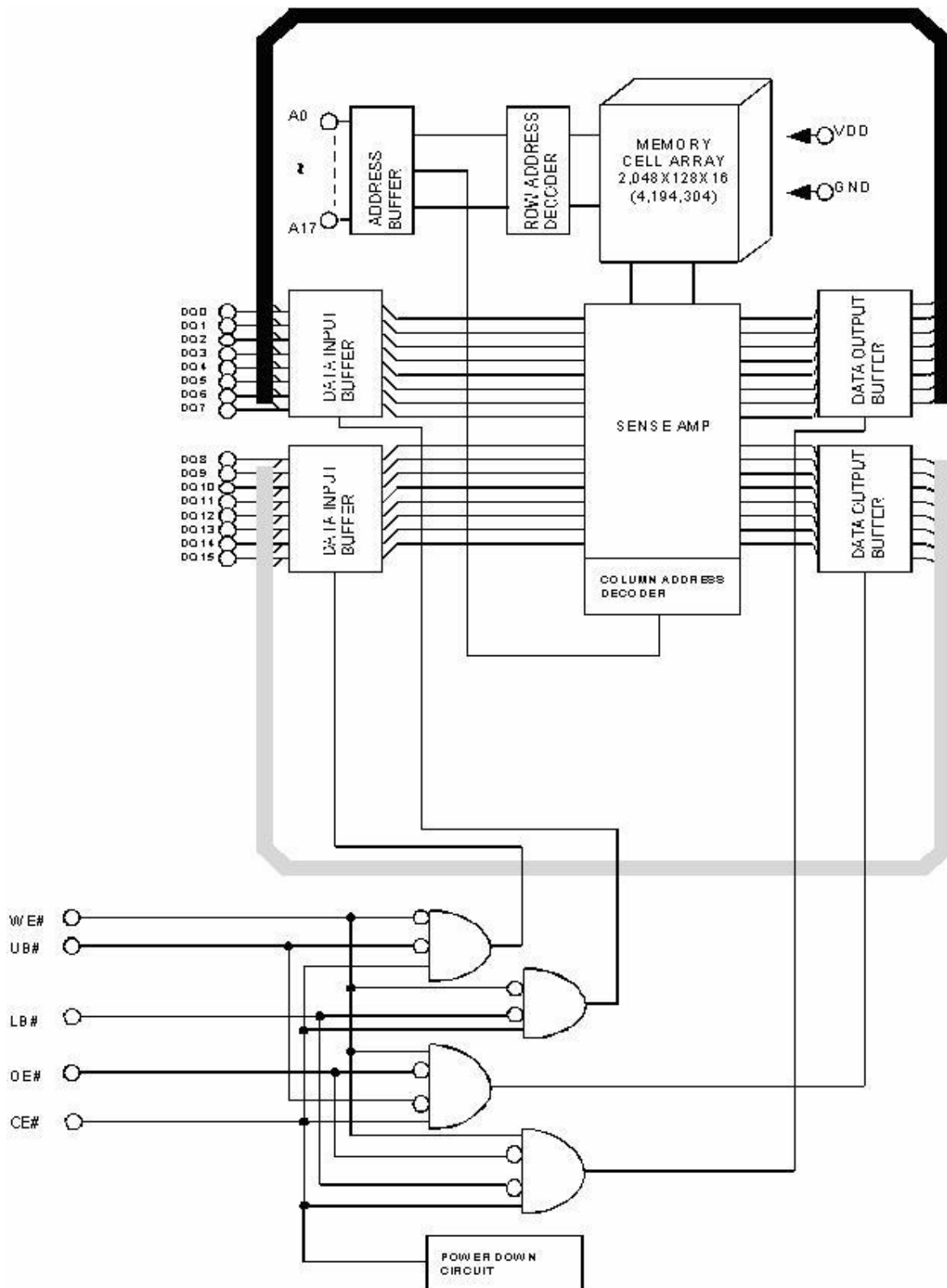
The EM564166 is a 4,194,304-bit SRAM organized as 262,144 words by 16 bits. It is designed with advanced CMOS technology. This Device operates from a single 2.7V to 3.6V power supply. Advanced circuit technology provides both high speed and low power. It is automatically placed in low-power mode when chip enable (CE#) is asserted high. There are two control inputs. CE# are used to select the device and for data retention control, and output enable (OE#) provides fast memory access. Data byte control pin (LB#,UB#) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range from -40°C to 85°C, the EM564166 can be used in environments exhibiting extreme temperature conditions.

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Block Diagram



Operating Mode

Mode	CE#	OE#	WE#	LB#	UB#	DQ0~DQ7	DQ8~DQ15
Read	L	L	H	L	L	D _{OUT}	D _{OUT}
				H	L	High-Z	D _{OUT}
				L	H	D _{OUT}	High-Z
Write	L	X	L	L	L	D _{IN}	D _{IN}
				H	L	High-Z	D _{IN}
				L	H	D _{IN}	High-Z
Output Deselect	L	H	H	X	X	High-Z	High-Z
	L	X	X	H	H		
Standby	H	X	X	X	X	High-Z	High-Z

Note: X = don't care. H=logic high. L=logic low.

Absolute Maximum Ratings

Supply voltage, V _{DD}	-0.3 to +4.6V
Input voltages, V _{IN}	-0.3 to +4.6V
Input and output voltages, V _{I/O}	-0.5 to V _{DD} +0.5V
Operating temperature, T _{OPR}	-40 to +85°C
Storage temperature, T _{STRG}	-55 to +150°C
Soldering Temperature (10s), T _{SOLDER}	260°C
Power dissipation, P _D	0.6 W

DC Recommended Operating Conditions (Ta=-40°C to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Power Supply Voltage	2.7	-	3.6	V
V _{IH}	Input High Voltage	2.7	-	V _{DD} + 0.3 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽²⁾	-	0.6	V
V _{DR}	Data Retention Supply Voltage	1.5	-	3.6	V

Note:

(1) Overshoot : V_{DD} +2.0V in case of pulse width ≤ 20ns

(2) Undershoot : -2.0V in case of pulse width ≤ 20ns

DC Characteristics (Ta = -40°C to 85°C, V_{DD} = 2.7V to 3.6V)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Input low current	I _{IL}	I _{IN} = 0V to V _{DD}			- 1	1	μA
Output low voltage	V _{OL}	I _{OL} = 2.1 mA			-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA			V _{DD} - 0.15	-	V
Operating current	I _{DD1}	CE# = V _{IL} and I _{OUT} = 0mA	Cycle time = min	V _{DD} = 3.6 V	-	25	mA
	I _{DD2}	Other Input = V _{IH} / V _{IL}	Cycle time = 1μs		-	5	
Standby current	I _{DD2}	CE# ≥ V _{DD} - 0.2V	-55/70/85	V _{DD} = 3.6 V	-	35	μA

Capacitance (Ta = 25°C; f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C _{IN}	-	-	10	pF	V _{IN} = GND
Output capacitance	C _{OUT}	-	-	10	pF	V _{OUT} = GND

Notes: This parameter is periodically sampled and is not 100% tested.

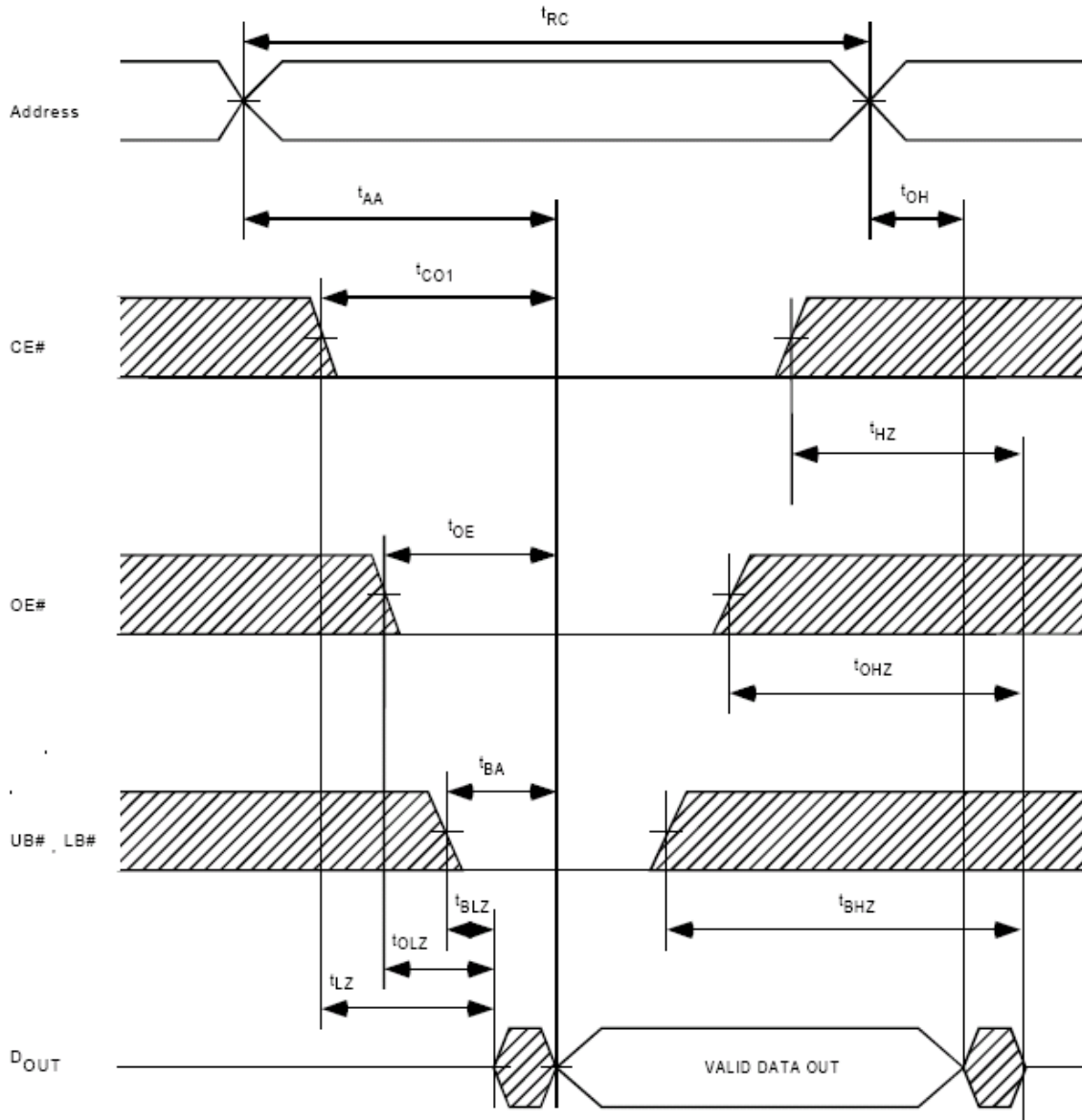
AC Characteristics and Operating Conditions (Ta = -40°C to 85°C, VDD = 2.7V to 3.6V)

Read Cycle								
Symbol	Parameter	EM564166						Unit
		-85		-70		-55		
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read cycle time	85	–	70	–	55	–	ns
t _{AA}	Address access time	–	85	–	70	–	55	
t _{CO1}	Chip Enable (CE#) Access Time	–	85	–	70	–	55	
t _{OE}	Output enable access time	–	45	–	35	–	25	
t _{BA}	Data Byte Control Access Time	–	85	–	70	–	55	
t _{LZ}	Chip Enable Low to Output in Low-Z	10	–	10	–	10	–	
t _{OLZ}	Output enable Low to Output in Low-Z	3	–	3	–	3	–	
t _{BLZ}	Data Byte Control Low to Output in Low-Z	5	–	5	–	5	–	
t _{HZ}	Chip Enable High to Output in High-Z	–	35	–	25	–	20	
t _{OHZ}	Output Enable High to Output in High-Z	–	35	–	25	–	20	
t _{BHZ}	Data Byte Control High to Output in High-Z	–	35	–	25	–	20	
t _{OH}	Output Data Hold Time	0	–	0	–	0	–	
Write Cycle								
Symbol	Parameter	EM564166						Unit
		-85		-70		-55		
		Min	Max	Min	Max	Min	Max	
t _{WC}	Write cycle time	85	–	70	–	55	–	ns
t _{WP}	Write pulse width	55	–	55	–	40	–	
t _{CW}	Chip Enable to end of write	70	–	60	–	45	–	
t _{BW}	Data Byte Control to end of Write	70	–	60	–	45	–	
t _{AS}	Address setup time	0	–	0	–	0	–	
t _{WR}	Write Recovery time	0	–	0	–	0	–	
t _{WHZ}	WE# Low to Output in High-Z	–	35	–	30	–	25	
t _{OW}	WE# High to Output in Low-Z	5	–	5	–	5	–	
t _{DS}	Data Setup Time	35	–	30	–	30	–	
t _{DH}	Data Hold Time	0	–	0	–	0	–	

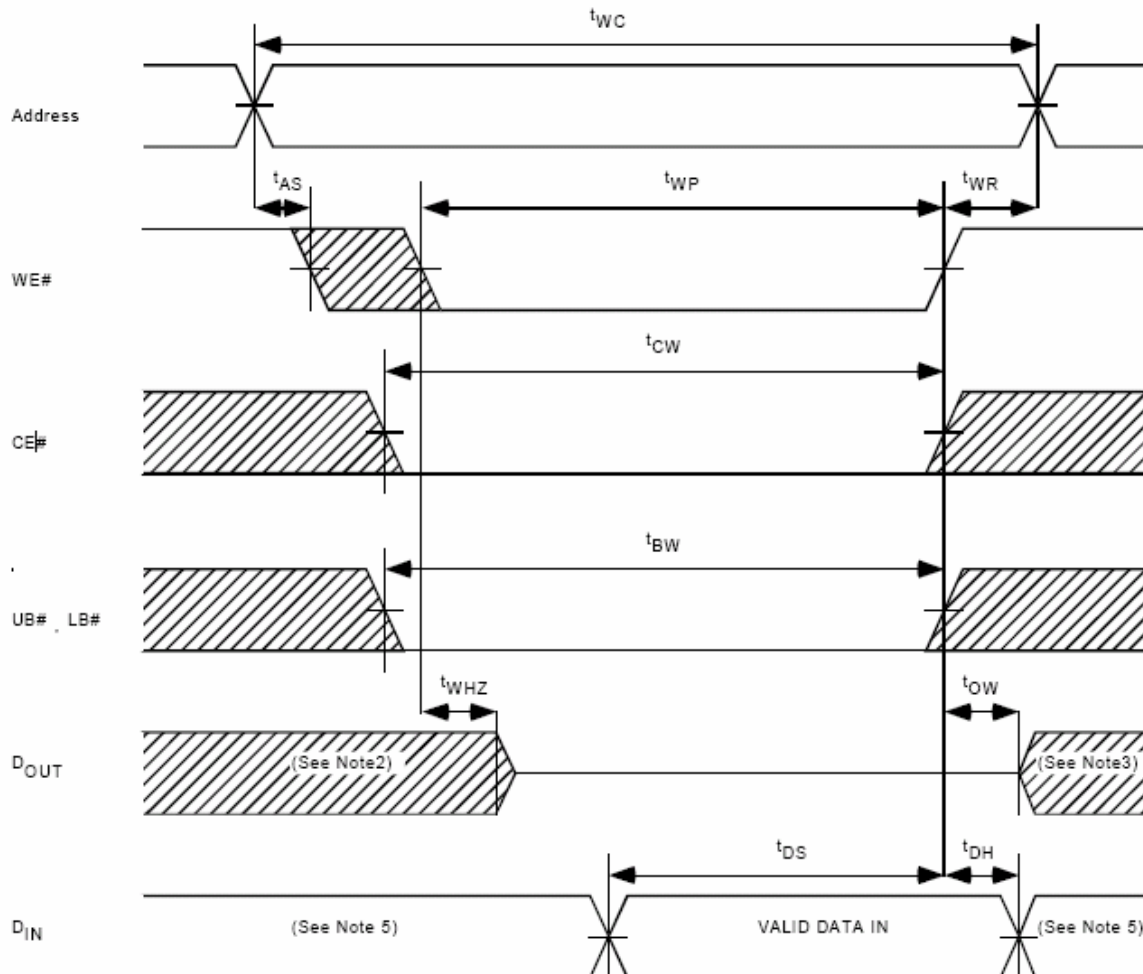
AC Test Condition

- Output load : 50pF + one TTL gate
- Input pulse level : 0.4V, 2.4V
- Timing measurements : 0.5 x VDD
- t_R, t_F : 5ns

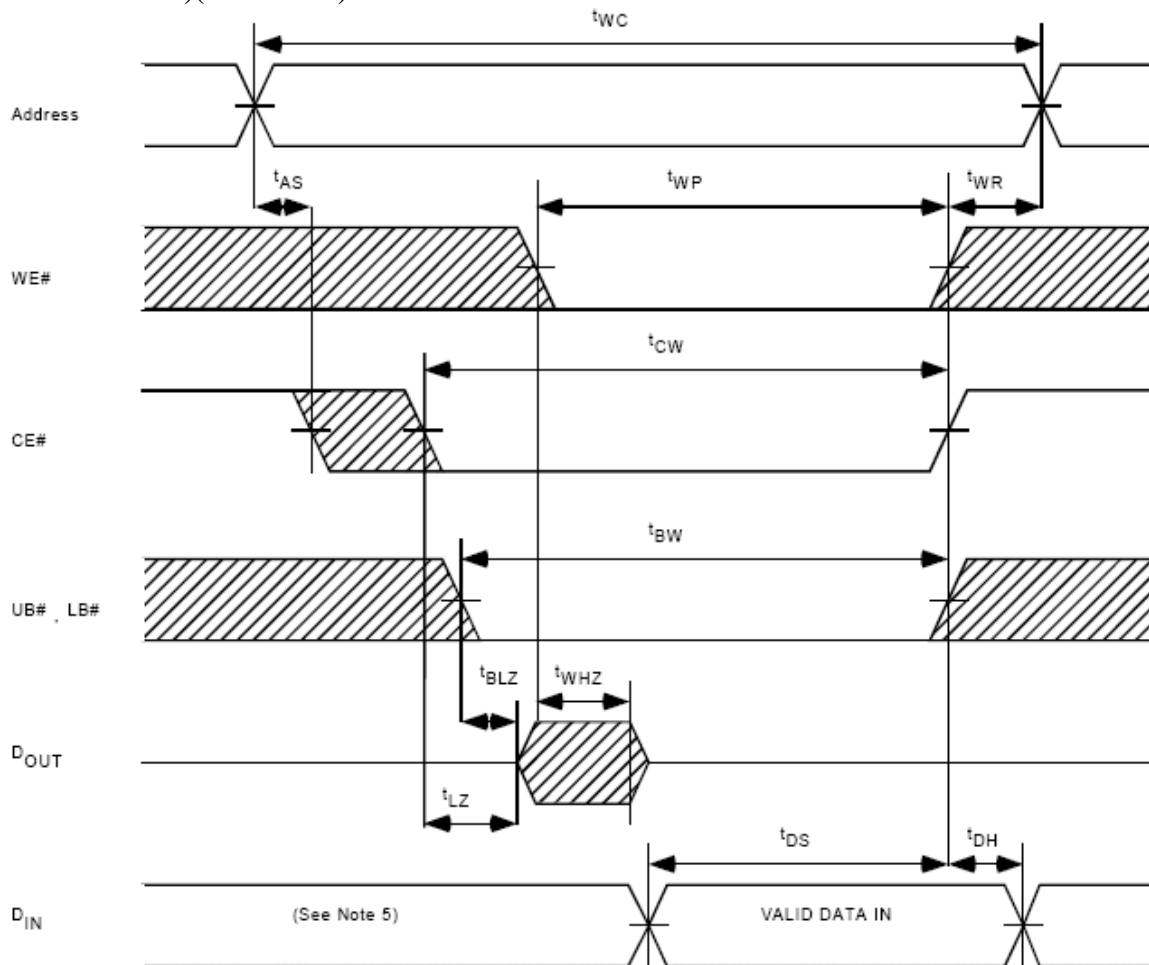
Read Cycle (See Note 1)



Write Cycle1 (WE# Controlled)(See Note 4)

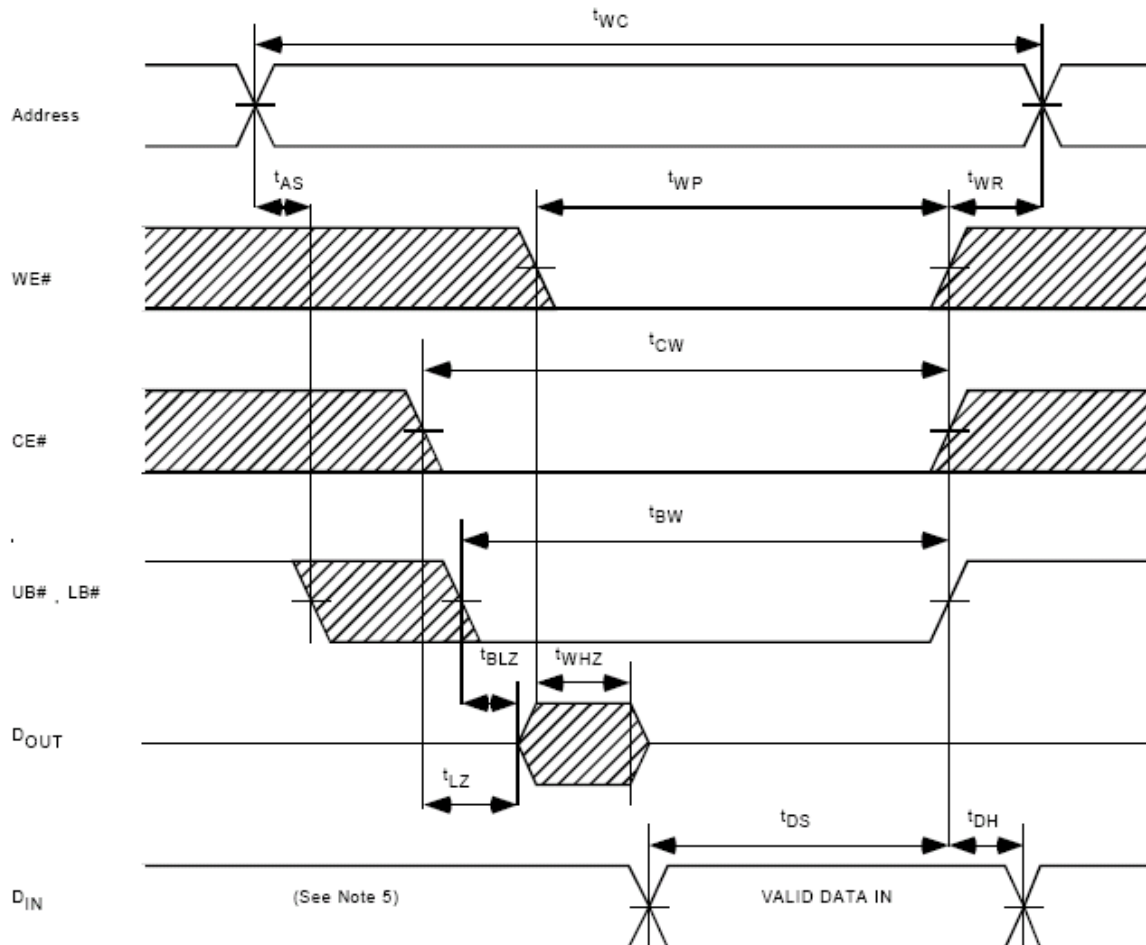


Write Cycle 2 (CE# Controlled)(See Note 4)



Write Cycle3

(UB#, LB# Controlled)(See Note 4)



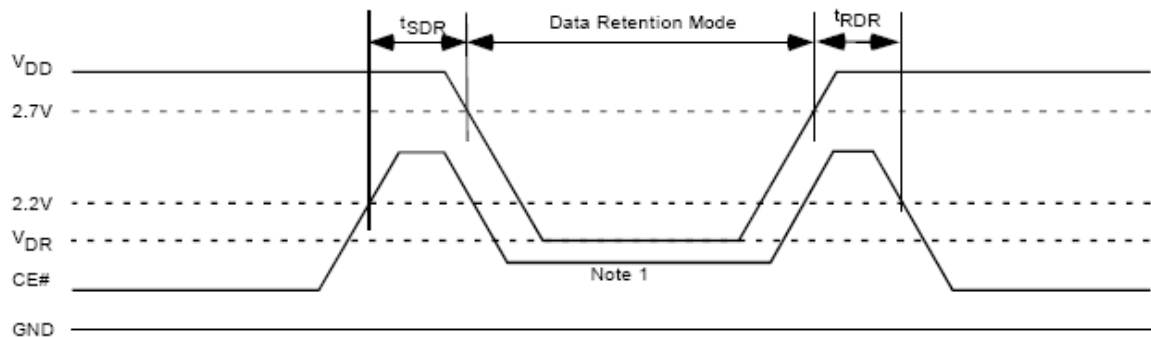
Note:

1. WE# remains HIGH for the read cycle.
2. If CE# goes LOW with or after WE# goes LOW, the outputs will remain at high impedance.
3. If CE# goes HIGH coincident with or before WE# goes HIGH, the outputs will remain at high impedance.
4. If OE# is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

Data Retention Characteristics (Ta = -40°C to 85°C)

Symbol	Parameter	Min	Max	Unit
V _{DR}	Data Retention Supply Voltage CE# ≥ V _{DD} - 0.2V, VIN ≥ V _{DD} - 0.2V or VIN ≤ 0.2V	1.5	3.6	V
I _{DR}	Data Retention Current V _{DD} = 1.5V, CE# ≥ V _{DD} - 0.2V, VIN ≥ V _{DD} - 0.2V or VIN ≤ 0.2V	–	35	μA
t _{SDR}	Chip Deselect to Data Retention Mode Time	0	–	ns
t _{RDR}	Recovery Time	t _{RC}	–	ns

CE# Controlled Data Retention Mode



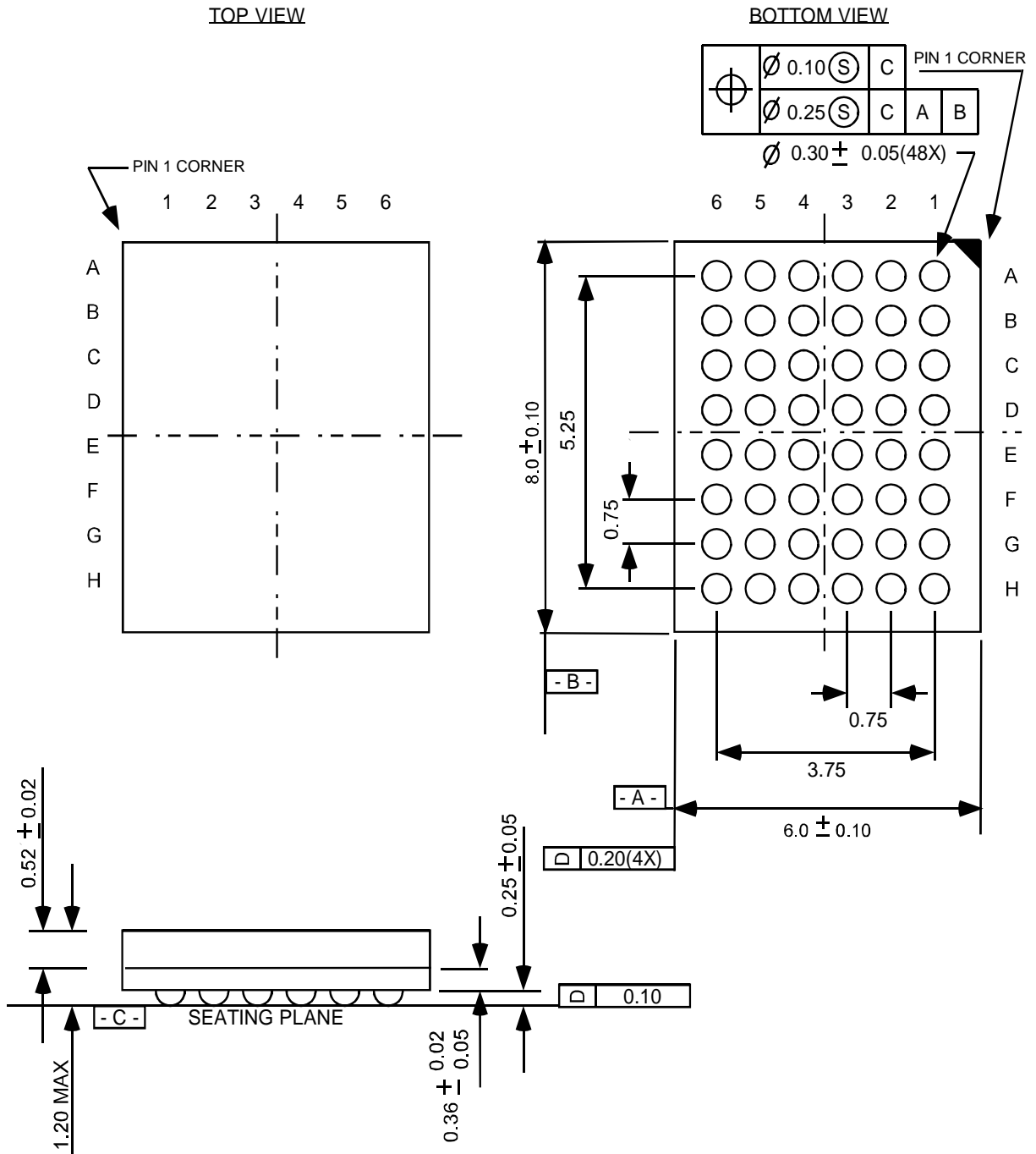
Note:

1. CE# ≥ V_{DD} - 0.2V or UB# = LB# ≥ V_{DD} - 0.2V

Package Diagrams

48-Ball (6mm x 8mm) BGA

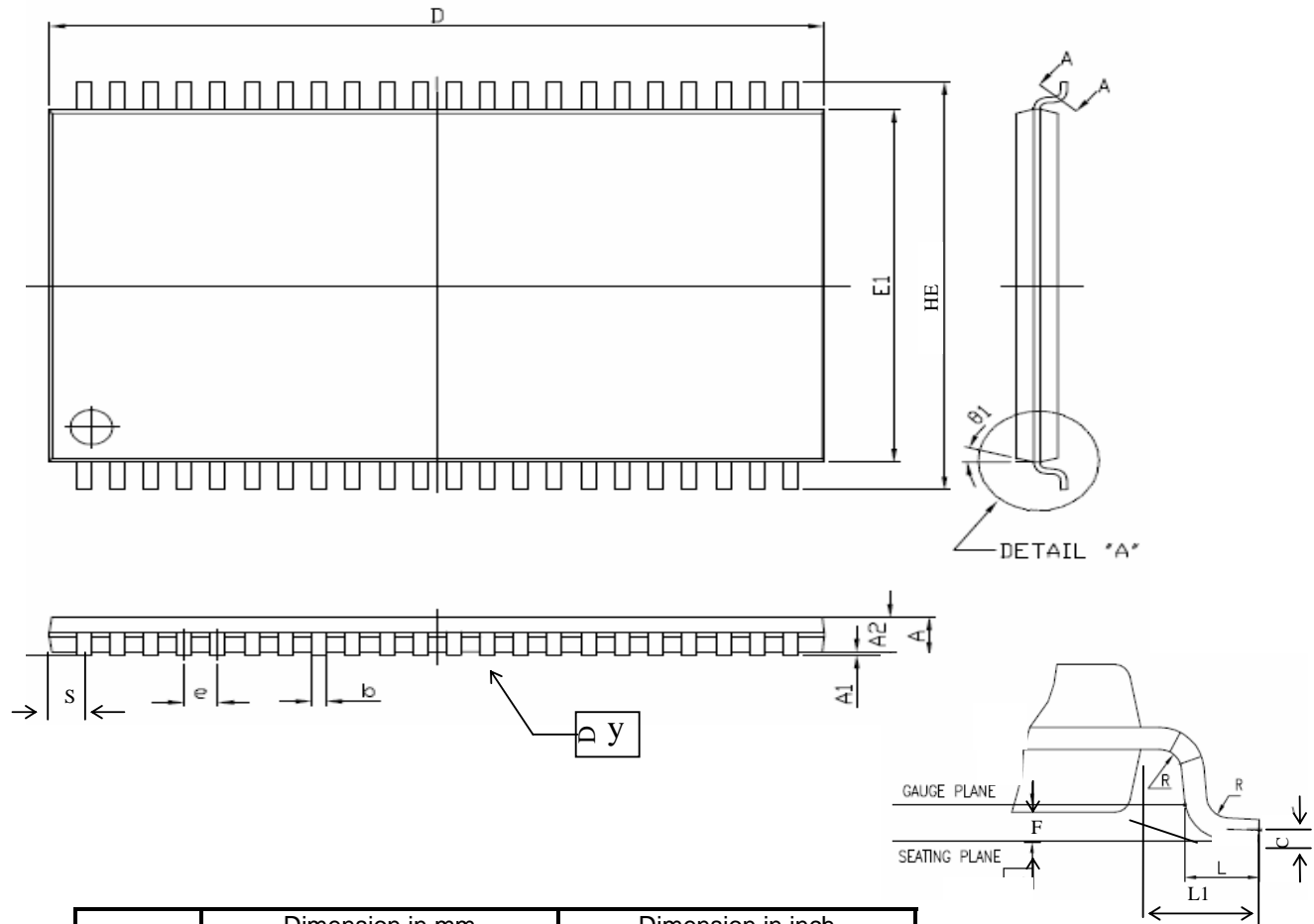
Units in mm



Package Diagrams

44-pin TSOP II

Units in mm



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.2	---	---	0.047
A1	0.05	---	0.2	0.002	---	0.008
A2	0.90	1.0	1.1	0.035	0.039	0.043
b	0.22	---	0.45	0.009	---	0.018
e	---	0.80	---	---	0.031	---
C	0.095	0.125	0.21	0.004	0.005	0.008
D	18.28	18.41	18.54	0.720	0.725	0.730
E	10.03	10.16	10.29	0.395	0.400	0.405
HE	11.56	11.76	11.96	0.455	0.463	0.471
L	0.40	---	0.75	0.016	---	0.03
L1	0.8 BASIC			0.032 BASIC		
F	---	0.25	---	---	0.01	---
	0°	---	10°	0°	---	10°
S	0.805 REF			0.03 REF		
Δ y	---	---	0.10	---	---	0.004