EM65571

130COM / 128SEG
65K Color STN
LCD Driver

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History		
Version	Revision Description	Date
0.1	Initial version	2004/09/02
0.2	Modified the bump size on page 6	2004/11/04
0.3	Modified the VBA pin description on page 17 Modified the voltage generation circuit on page 57~58	2004/12/24
0.4	Added V0 DC spec. on page 105	2005/1/07
0.5	Modified the pin configurations on page 5~14 Modified the write timing “tWRLW8” values of the AC characteristics on page 110 and page 112	2005/1/24
0.6	Modified the VBA application circuit	2005/02/16
1.0	Modified the DV Range 128→ 114 Removed the “Preliminary” water mark	2005/08/04

1 General Description

The EM65571 is one of the industry's most advanced wide-screen STN-LCD drivers for 65K-color displays. It has a built-in display RAM, a power supply circuit for LCD drive, an LCD controller circuit, and support for LCD cell tolerance compensation of V_{LCD} by external pin selection. It also supports the EEPROM function for programming information to tune V_{LCD} offset voltage to get the best contrast. Therefore, this contributes to a compact system design. In addition, its partial display function realizes low power consumption.

*Partial display function: A function that utilizes only part of the screen, thus reducing power consumption.

2 Feature

- 65K-color display
- LCD output: Segment 128RGB (384 outputs); Common 128 outputs
- Display RAM capacity: 128x130x16=266240 bits
- Built-in display RAM and power supply circuit
- Partial display function
- Bus connection with 80-family/68-family MPU/ELAN MPU
- Logic power supply voltage: 2.2V to 3.3V
- LCD driving voltage: 5.0V to 20V
- Booster: 2 to 7 times
- Fast burst-RAM write function
- EEPROM function for tuning LCD operating voltage Vop
- Write system cycle: 200 ns
- Package:

Part Number	Package	Description	Package Information
EM65571AGH	Gold bumped chip	NA	Page 5

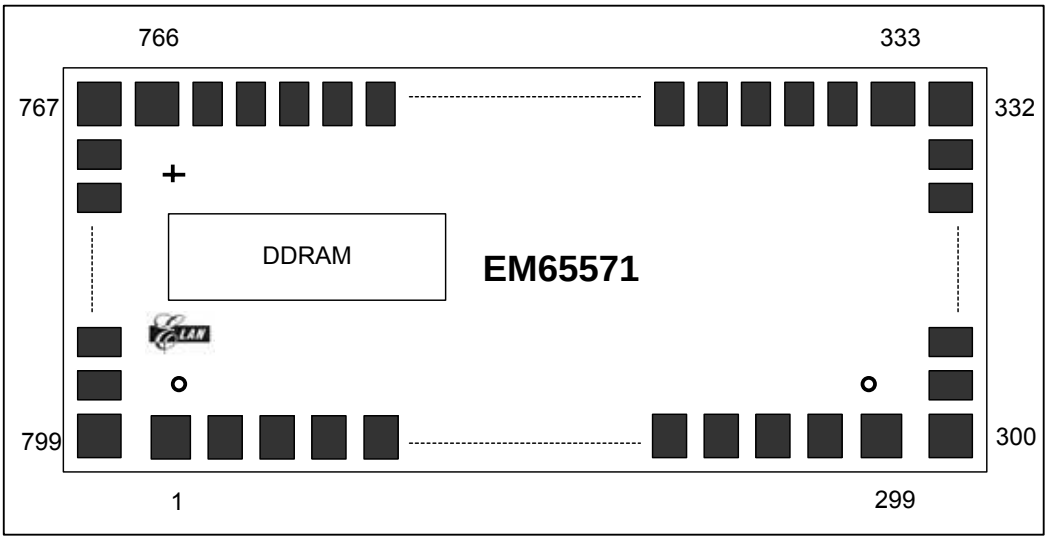
Note: The EM65571 series has the following sub-codes, depending on their shapes.
H: Bare chip (Aluminum pad without bump); **GH**: Gold bumped chip
F: COF package; **T**: TAB (TCP) package

Example:
EM65571AGH → EM65571: Elan number; A: Package Version; GH: Gold bumped chip

3 Applications

- Mobile phone
- Small PDA

3.1 Pin Configuration

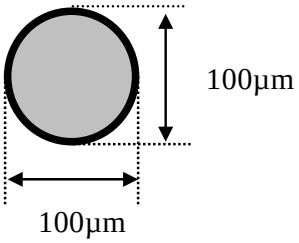


Note: *With the Elan logo at the left corner (as shown in the figure) and DDRAM (black color) on the left side, Pin 1 is at the bottom left corner.*

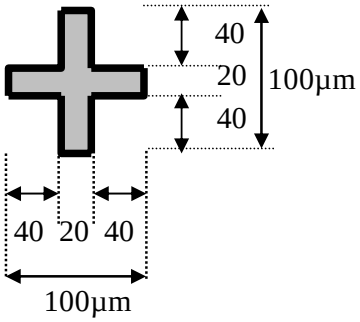
Figure 1. Pin Configuration

Mark	Coordinate (X, Y)	Mark	Coordinate (X, Y)
U-Left	-9836.85 , 376.85	U-Right	NA
D-Left	-9836.85 , -372.55	D-Right	9836.85 , -372.55

D-Left and D-Right:



U-Left and U-Right:



3.2 Pin Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	20580	1720	μm
Bump Size	1~28,272~299,333~766	30	70	
	300~332,767~799	70	30	
	30~270	42	59	
	29,271	48	70	
Pad Pitch	45 (min.)			
Die thickness (excluding bumps)	20+-1 mil (500+-25 μm)			
Bump Height	17+-3 μm			
Minimum Bump Gap	15			
Coordinate Origin	Chip center			

Recommended Cog Ito Traces Resistor

Interface	ITO Traces Resistances
V0~V4 CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP4+, CAP5+, CAP6+, Vout VDD, VEE VSSL, VSSH	Max = 50Ω
WRB, RDB, CSB,… D0~D7	Max = 3KΩ
RESB	Max = 5~10KΩ

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
1	NC1	-9846.8 , -729.0	51	RS	-7235.3 , -734.5
2	COM109	-9801.8 , -729.0	52	RS	-7175.3 , -734.5
3	COM111	-9756.8 , -729.0	53	RS	-7115.3 , -734.5
4	COM113	-9711.8 , -729.0	54	VSSL	-7055.3 , -734.5
5	COM115	-9666.8 , -729.0	55	VSSL	-6995.3 , -734.5
6	COM117	-9621.8 , -729.0	56	VSSL	-6935.3 , -734.5
7	COM119	-9576.8 , -729.0	57	VDD	-6647.3 , -734.5
8	COM121	-9531.8 , -729.0	58	VDD	-6587.3 , -734.5
9	COM123	-9486.8 , -729.0	59	VDD	-6527.3 , -734.5
10	COM125	-9441.8 , -729.0	60	P/S	-6467.3 , -734.5
11	COM127	-9396.8 , -729.0	61	P/S	-6407.3 , -734.5
12	DUMMY	-9351.8 , -729.0	62	P/S	-6347.3 , -734.5
13	DUMMY	-9306.8 , -729.0	63	M86	-6287.3 , -734.5
14	DUMMY	-9261.8 , -729.0	64	M86	-6227.3 , -734.5
15	DUMMY	-9216.8 , -729.0	65	M86	-6167.3 , -734.5
16	DUMMY	-9171.8 , -729.0	66	VSSL	-6107.3 , -734.5
17	DUMMY	-9126.8 , -729.0	67	VSSL	-6047.3 , -734.5
18	DUMMY	-9081.8 , -729.0	68	VSSL	-5987.3 , -734.5
19	DUMMY	-9036.8 , -729.0	69	VSSL	-5927.3 , -734.5
20	DUMMY	-8991.8 , -729.0	70	WRB	-5867.3 , -734.5
21	DUMMY	-8946.8 , -729.0	71	WRB	-5807.3 , -734.5
22	DUMMY	-8901.8 , -729.0	72	WRB	-5747.3 , -734.5
23	DUMMY	-8856.8 , -729.0	73	RDB	-5687.3 , -734.5
24	DUMMY	-8811.8 , -729.0	74	RDB	-5627.3 , -734.5
25	DUMMY	-8766.8 , -729.0	75	RDB	-5567.3 , -734.5
26	DUMMY	-8721.8 , -729.0	76	VDD	-5279.3 , -734.5
27	DUMMY	-8676.8 , -729.0	77	VDD	-5219.3 , -734.5
28	COMB	-8631.8 , -729.0	78	VDD	-5159.3 , -734.5
29	NC2	-8576.3 , -729.0	79	VPP	-4859.3 , -734.5
30	VSSL	-8495.3 , -734.5	80	VPP	-4799.3 , -734.5
31	VSSL	-8435.3 , -734.5	81	VPP	-4739.3 , -734.5
32	VSSL	-8375.3 , -734.5	82	NC14	-4439.3 , -734.5
33	VSSL	-8315.3 , -734.5	83	D0	-4379.3 , -734.5
34	VSSL	-8255.3 , -734.5	84	D0	-4319.3 , -734.5
35	VSSL	-8195.3 , -734.5	85	D0	-4259.3 , -734.5
36	VSSL	-8135.3 , -734.5	86	D1	-4199.3 , -734.5
37	VSSL	-8075.3 , -734.5	87	D1	-4139.3 , -734.5
38	VSSL	-8015.3 , -734.5	88	D1	-4079.3 , -734.5
39	VSSL	-7955.3 , -734.5	89	D2	-4019.3 , -734.5
40	VSSL	-7895.3 , -734.5	90	D2	-3959.3 , -734.5
41	VSSL	-7835.3 , -734.5	91	D2	-3899.3 , -734.5
42	TEST	-7775.3 , -734.5	92	D3	-3839.3 , -734.5
43	TEST	-7715.3 , -734.5	93	D3	-3779.3 , -734.5
44	TEST	-7655.3 , -734.5	94	D3	-3719.3 , -734.5
45	RESB	-7595.3 , -734.5	95	D4	-3431.3 , -734.5
46	RESB	-7535.3 , -734.5	96	D4	-3371.3 , -734.5
47	RESB	-7475.3 , -734.5	97	D4	-3311.3 , -734.5
48	CSB	-7415.3 , -734.5	98	D5	-3251.3 , -734.5
49	CSB	-7355.3 , -734.5	99	D5	-3191.3 , -734.5
50	CSB	-7295.3 , -734.5	100	D5	-3131.3 , -734.5

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
101	D6	-3071.3 , -734.5	151	VDD	386.8 , -734.5
102	D6	-3011.3 , -734.5	152	V0	485.45 , -734.5
103	D6	-2951.3 , -734.5	153	V0	545.45 , -734.5
104	D7	-2891.3 , -734.5	154	V0	605.45 , -734.5
105	D7	-2831.3 , -734.5	155	V0	665.45 , -734.5
106	D7	-2771.3 , -734.5	156	V0	725.45 , -734.5
107	D8	-2711.3 , -734.5	157	V0	785.45 , -734.5
108	D8	-2651.3 , -734.5	158	V1	845.45 , -734.5
109	D8	-2591.3 , -734.5	159	V1	905.45 , -734.5
110	D9	-2531.3 , -734.5	160	V1	965.45 , -734.5
111	D9	-2471.3 , -734.5	161	V1	1025.45 , -734.5
112	D9	-2411.3 , -734.5	162	V1	1085.45 , -734.5
113	D10	-2351.3 , -734.5	163	V1	1145.45 , -734.5
114	D10	-2291.3 , -734.5	164	V2	1205.45 , -734.5
115	D10	-2231.3 , -734.5	165	V2	1265.45 , -734.5
116	D11	-2171.3 , -734.5	166	V2	1325.45 , -734.5
117	D11	-2111.3 , -734.5	167	V2	1385.45 , -734.5
118	D11	-2051.3 , -734.5	168	V2	1445.45 , -734.5
119	D12	-1761.2 , -734.5	169	V2	1505.45 , -734.5
120	D12	-1701.2 , -734.5	170	V3	1783.55 , -734.5
121	D12	-1641.2 , -734.5	171	V3	1843.55 , -734.5
122	D13	-1581.2 , -734.5	172	V3	1903.55 , -734.5
123	D13	-1521.2 , -734.5	173	V3	1963.55 , -734.5
124	D13	-1461.2 , -734.5	174	V3	2023.55 , -734.5
125	D14	-1401.2 , -734.5	175	V3	2083.55 , -734.5
126	D14	-1341.2 , -734.5	176	V4	2143.55 , -734.5
127	D14	-1281.2 , -734.5	177	V4	2203.55 , -734.5
128	D15	-1221.2 , -734.5	178	V4	2263.55 , -734.5
129	D15	-1161.2 , -734.5	179	V4	2323.55 , -734.5
130	D15	-1101.2 , -734.5	180	V4	2383.55 , -734.5
131	VSSL	-1041.2 , -734.5	181	V4	2443.55 , -734.5
132	VSSL	-981.2 , -734.5	182	VSSH	2503.55 , -734.5
133	VSSL	-921.2 , -734.5	183	VSSH	2563.55 , -734.5
134	CK	-861.2 , -734.5	184	VSSH	2623.55 , -734.5
135	CK	-801.2 , -734.5	185	VSSH	2683.55 , -734.5
136	CK	-741.2 , -734.5	186	VSSH	2743.55 , -734.5
137	CKS	-681.2 , -734.5	187	VSSH	2803.55 , -734.5
138	CKS	-621.2 , -734.5	188	VSSH	2863.55 , -734.5
139	CKS	-561.2 , -734.5	189	VSSH	2923.55 , -734.5
140	VDD	-273.2 , -734.5	190	NC3	2986.55 , -734.5
141	VDD	-213.2 , -734.5	191	VBA	3267.9 , -734.5
142	VDD	-153.2 , -734.5	192	VBA	3327.9 , -734.5
143	VDD	-93.2 , -734.5	193	VBA	3387.9 , -734.5
144	VDD	-33.2 , -734.5	194	VBA	3447.9 , -734.5
145	VDD	26.8 , -734.5	195	VBA	3507.9 , -734.5
146	VDD	86.8 , -734.5	196	VBA	3567.9 , -734.5
147	VDD	146.8 , -734.5	197	VREF	3627.9 , -734.5
148	VDD	206.8 , -734.5	198	VREF	3687.9 , -734.5
149	VDD	266.8 , -734.5	199	VREF	3747.9 , -734.5
150	VDD	326.8 , -734.5	200	VREF	3807.9 , -734.5

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
201	VREF	3867.9 , -734.5	251	CAP3+	7111.9 , -734.5
202	VREF	3927.9 , -734.5	252	CAP3+	7171.9 , -734.5
203	VEE	3987.9 , -734.5	253	CAP4+	7231.9 , -734.5
204	VEE	4047.9 , -734.5	254	CAP4+	7291.9 , -734.5
205	VEE	4107.9 , -734.5	255	CAP4+	7351.9 , -734.5
206	VEE	4167.9 , -734.5	256	CAP4+	7411.9 , -734.5
207	VEE	4227.9 , -734.5	257	CAP4+	7471.9 , -734.5
208	VEE	4287.9 , -734.5	258	CAP4+	7531.9 , -734.5
209	VSSH	4347.9 , -734.5	259	CAP5+	7835.3 , -734.5
210	VSSH	4407.9 , -734.5	260	CAP5+	7895.3 , -734.5
211	VSSH	4467.9 , -734.5	261	CAP5+	7955.3 , -734.5
212	VSSH	4527.9 , -734.5	262	CAP5+	8015.3 , -734.5
213	VSSH	4587.9 , -734.5	263	CAP5+	8075.3 , -734.5
214	VSSH	4647.9 , -734.5	264	CAP5+	8135.3 , -734.5
215	VSSH	4707.9 , -734.5	265	CAP6+	8195.3 , -734.5
216	VSSH	4767.9 , -734.5	266	CAP6+	8255.3 , -734.5
217	VOUT	4827.9 , -734.5	267	CAP6+	8315.3 , -734.5
218	VOUT	4887.9 , -734.5	268	CAP6+	8375.3 , -734.5
219	VOUT	4947.9 , -734.5	269	CAP6+	8435.3 , -734.5
220	VOUT	5007.9 , -734.5	270	CAP6+	8495.3 , -734.5
221	VOUT	5067.9 , -734.5	271	NC4	8576.3 , -729.0
222	VOUT	5127.9 , -734.5	272	DUMMY	8631.8 , -729.0
223	CAP1-	5187.9 , -734.5	273	DUMMY	8676.8 , -729.0
224	CAP1-	5247.9 , -734.5	274	DUMMY	8721.8 , -729.0
225	CAP1-	5307.9 , -734.5	275	DUMMY	8766.8 , -729.0
226	CAP1-	5367.9 , -734.5	276	DUMMY	8811.8 , -729.0
227	CAP1-	5427.9 , -734.5	277	DUMMY	8856.8 , -729.0
228	CAP1-	5487.9 , -734.5	278	DUMMY	8901.8 , -729.0
229	CAP1+	5791.9 , -734.5	279	DUMMY	8946.8 , -729.0
230	CAP1+	5851.9 , -734.5	280	DUMMY	8991.8 , -729.0
231	CAP1+	5911.9 , -734.5	281	DUMMY	9036.8 , -729.0
232	CAP1+	5971.9 , -734.5	282	DUMMY	9081.8 , -729.0
233	CAP1+	6031.9 , -734.5	283	DUMMY	9126.8 , -729.0
234	CAP1+	6091.9 , -734.5	284	DUMMY	9171.8 , -729.0
235	CAP2-	6151.9 , -734.5	285	DUMMY	9216.8 , -729.0
236	CAP2-	6211.9 , -734.5	286	DUMMY	9261.8 , -729.0
237	CAP2-	6271.9 , -734.5	287	DUMMY	9306.8 , -729.0
238	CAP2-	6331.9 , -734.5	288	COM126	9351.8 , -729.0
239	CAP2-	6391.9 , -734.5	289	COM124	9396.8 , -729.0
240	CAP2-	6451.9 , -734.5	290	COM122	9441.8 , -729.0
241	CAP2+	6511.9 , -734.5	291	COM120	9486.8 , -729.0
242	CAP2+	6571.9 , -734.5	292	COM118	9531.8 , -729.0
243	CAP2+	6631.9 , -734.5	293	COM116	9576.8 , -729.0
244	CAP2+	6691.9 , -734.5	294	COM114	9621.8 , -729.0
245	CAP2+	6751.9 , -734.5	295	COM112	9666.8 , -729.0
246	CAP2+	6811.9 , -734.5	296	COM110	9711.8 , -729.0
247	CAP3+	6871.9 , -734.5	297	COM108	9756.8 , -729.0
248	CAP3+	6931.9 , -734.5	298	COM106	9801.8 , -729.0
249	CAP3+	6991.9 , -734.5	299	NC5	9846.8 , -729.0
250	CAP3+	7051.9 , -734.5	300	NC6	10159.0 , -720.0

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
301	COM104	10159.0 , -675.0	351	COM8	9036.8 , 729.0
302	COM102	10159.0 , -630.0	352	COM6	8991.8 , 729.0
303	COM100	10159.0 , -585.0	353	COM4	8946.8 , 729.0
304	COM98	10159.0 , -540.0	354	COM2	8901.8 , 729.0
305	COM96	10159.0 , -495.0	355	COM0	8856.8 , 729.0
306	COM94	10159.0 , -450.0	356	COMA	8811.8 , 729.0
307	COM92	10159.0 , -405.0	357	NC9	8766.8 , 729.0
308	COM90	10159.0 , -360.0	358	SEGA0	8721.8 , 729.0
309	COM88	10159.0 , -315.0	359	SEGB0	8676.8 , 729.0
310	COM86	10159.0 , -270.0	360	SEGC0	8631.8 , 729.0
311	COM84	10159.0 , -225.0	361	SEGA1	8586.8 , 729.0
312	COM82	10159.0 , -180.0	362	SEGB1	8541.8 , 729.0
313	COM80	10159.0 , -135.0	363	SEGC1	8496.8 , 729.0
314	COM78	10159.0 , -90.0	364	SEGA2	8451.8 , 729.0
315	COM76	10159.0 , -45.0	365	SEGB2	8406.8 , 729.0
316	COM74	10159. 0, 0.0	366	SEGC2	8361.8 , 729.0
317	COM72	10159.0 , 45.0	367	SEGA3	8316.8 , 729.0
318	COM70	10159.0 , 90.0	368	SEGB3	8271.8 , 729.0
319	COM68	10159.0 , 135.0	369	SEGC3	8226.8 , 729.0
320	COM66	10159.0 , 180.0	370	SEGA4	8181.8 , 729.0
321	COM64	10159.0 , 225.0	371	SEGB4	8136.8 , 729.0
322	COM62	10159.0 , 270.0	372	SEGC4	8091.8 , 729.0
323	COM60	10159.0 , 315.0	373	SEGA5	8046.8 , 729.0
324	COM58	10159.0 , 360.0	374	SEGB5	8001.8 , 729.0
325	COM56	10159.0 , 405.0	375	SEGC5	7956.8 , 729.0
326	COM54	10159.0 , 450.0	376	SEGA6	7911.8 , 729.0
327	COM52	10159.0 , 495.0	377	SEGB6	7866.8 , 729.0
328	COM50	10159.0 , 540.0	378	SEGC6	7821.8 , 729.0
329	COM48	10159.0 , 585.0	379	SEGA7	7776.8 , 729.0
330	COM46	10159.0 , 630.0	380	SEGB7	7731.8 , 729.0
331	COM44	10159.0 , 675.0	381	SEGC7	7686.8 , 729.0
332	NC7	10159.0 , 720.0	382	SEGA8	7641.8 , 729.0
333	NC8	9846.8 , 729.0	383	SEGB8	7596.8 , 729.0
334	COM42	9801.8 , 729.0	384	SEGC8	7551.8 , 729.0
335	COM40	9756.8 , 729.0	385	SEGA9	7506.8 , 729.0
336	COM38	9711.8 , 729.0	386	SEGB9	7461.8 , 729.0
337	COM36	9666.8 , 729.0	387	SEGC9	7416.8 , 729.0
338	COM34	9621.8 , 729.0	388	SEGA10	7371.8 , 729.0
339	COM32	9576.8 , 729.0	389	SEGB10	7326.8 , 729.0
340	COM30	9531.8 , 729.0	390	SEGC10	7281.8 , 729.0
341	COM28	9486.8 , 729.0	391	SEGA11	7236.8 , 729.0
342	COM26	9441.8 , 729.0	392	SEGB11	7191.8 , 729.0
343	COM24	9396.8 , 729.0	393	SEGC11	7146.8 , 729.0
344	COM22	9351.8 , 729.0	394	SEGA12	7101.8 , 729.0
345	COM20	9306.8 , 729.0	395	SEGB12	7056.8 , 729.0
346	COM18	9261.8 , 729.0	396	SEGC12	7011.8 , 729.0
347	COM16	9216.8 , 729.0	397	SEGA13	6966.8 , 729.0
348	COM14	9171.8 , 729.0	398	SEGB13	6921.8 , 729.0
349	COM12	9126.8 , 729.0	399	SEGC13	6876.8 , 729.0
350	COM10	9081.8 , 729.0	400	SEGA14	6831.8 , 729.0

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
401	SEGB14	6786.8 , 729.0	451	SEGA31	4536.8 , 729.0
402	SEGC14	6741.8 , 729.0	452	SEGB31	4491.8 , 729.0
403	SEGA15	6696.8 , 729.0	453	SEGC31	4446.8 , 729.0
404	SEGB15	6651.8 , 729.0	454	SEGA32	4401.8 , 729.0
405	SEGC15	6606.8 , 729.0	455	SEGB32	4356.8 , 729.0
406	SEGA16	6561.8 , 729.0	456	SEGC32	4311.8 , 729.0
407	SEGB16	6516.8 , 729.0	457	SEGA33	4266.8 , 729.0
408	SEGC16	6471.8 , 729.0	458	SEGB33	4221.8 , 729.0
409	SEGA17	6426.8 , 729.0	459	SEGC33	4176.8 , 729.0
410	SEGB17	6381.8 , 729.0	460	SEGA34	4131.8 , 729.0
411	SEGC17	6336.8 , 729.0	461	SEGB34	4086.8 , 729.0
412	SEGA18	6291.8 , 729.0	462	SEGC34	4041.8 , 729.0
413	SEGB18	6246.8 , 729.0	463	SEGA35	3996.8 , 729.0
414	SEGC18	6201.8 , 729.0	464	SEGB35	3951.8 , 729.0
415	SEGA19	6156.8 , 729.0	465	SEGC35	3906.8 , 729.0
416	SEGB19	6111.8 , 729.0	466	SEGA36	3861.8 , 729.0
417	SEGC19	6066.8 , 729.0	467	SEGB36	3816.8 , 729.0
418	SEGA20	6021.8 , 729.0	468	SEGC36	3771.8 , 729.0
419	SEGB20	5976.8 , 729.0	469	SEGA37	3726.8 , 729.0
420	SEGC20	5931.8 , 729.0	470	SEGB37	3681.8 , 729.0
421	SEGA21	5886.8 , 729.0	471	SEGC37	3636.8 , 729.0
422	SEGB21	5841.8 , 729.0	472	SEGA38	3591.8 , 729.0
423	SEGC21	5796.8 , 729.0	473	SEGB38	3546.8 , 729.0
424	SEGA22	5751.8 , 729.0	474	SEGC38	3501.8 , 729.0
425	SEGB22	5706.8 , 729.0	475	SEGA39	3456.8 , 729.0
426	SEGC22	5661.8 , 729.0	476	SEGB39	3411.8 , 729.0
427	SEGA23	5616.8 , 729.0	477	SEGC39	3366.8 , 729.0
428	SEGB23	5571.8 , 729.0	478	SEGA40	3321.8 , 729.0
429	SEGC23	5526.8 , 729.0	479	SEGB40	3276.8 , 729.0
430	SEGA24	5481.8 , 729.0	480	SEGC40	3231.8 , 729.0
431	SEGB24	5436.8 , 729.0	481	SEGA41	3186.8 , 729.0
432	SEGC24	5391.8 , 729.0	482	SEGB41	3141.8 , 729.0
433	SEGA25	5346.8 , 729.0	483	SEGC41	3096.8 , 729.0
434	SEGB25	5301.8 , 729.0	484	SEGA42	3051.8 , 729.0
435	SEGC25	5256.8 , 729.0	485	SEGB42	3006.8 , 729.0
436	SEGA26	5211.8 , 729.0	486	SEGC42	2961.8 , 729.0
437	SEGB26	5166.8 , 729.0	487	SEGA43	2916.8 , 729.0
438	SEGC26	5121.8 , 729.0	488	SEGB43	2871.8 , 729.0
439	SEGA27	5076.8 , 729.0	489	SEGC43	2826.8 , 729.0
440	SEGB27	5031.8 , 729.0	490	SEGA44	2781.8 , 729.0
441	SEGC27	4986.8 , 729.0	491	SEGB44	2736.8 , 729.0
442	SEGA28	4941.8 , 729.0	492	SEGC44	2691.8 , 729.0
443	SEGB28	4896.8 , 729.0	493	SEGA45	2646.8 , 729.0
444	SEGC28	4851.8 , 729.0	494	SEGB45	2601.8 , 729.0
445	SEGA29	4806.8 , 729.0	495	SEGC45	2556.8 , 729.0
446	SEGB29	4761.8 , 729.0	496	SEGA46	2511.8 , 729.0
447	SEGC29	4716.8 , 729.0	497	SEGB46	2466.8 , 729.0
448	SEGA30	4671.8 , 729.0	498	SEGC46	2421.8 , 729.0
449	SEGB30	4626.8 , 729.0	499	SEGA47	2376.8 , 729.0
450	SEGC30	4581.8 , 729.0	500	SEGB47	2331.8 , 729.0

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
501	SEGC47	2286.8 , 729.0	551	SEGB64	-171.8 , 729.0
502	SEGA48	2241.8 , 729.0	552	SEGC64	-216.8 , 729.0
503	SEGB48	2196.8 , 729.0	553	SEGA65	-261.8 , 729.0
504	SEGC48	2151.8 , 729.0	554	SEGB65	-306.8 , 729.0
505	SEGA49	2106.8 , 729.0	555	SEGC65	-351.8 , 729.0
506	SEGB49	2061.8 , 729.0	556	SEGA66	-396.8 , 729.0
507	SEGC49	2016.8 , 729.0	557	SEGB66	-441.8 , 729.0
508	SEGA50	1971.8 , 729.0	558	SEGC66	-486.8 , 729.0
509	SEGB50	1926.8 , 729.0	559	SEGA67	-531.8 , 729.0
510	SEGC50	1881.8 , 729.0	560	SEGB67	-576.8 , 729.0
511	SEGA51	1836.8 , 729.0	561	SEGC67	-621.8 , 729.0
512	SEGB51	1791.8 , 729.0	562	SEGA68	-666.8 , 729.0
513	SEGC51	1746.8 , 729.0	563	SEGB68	-711.8 , 729.0
514	SEGA52	1701.8 , 729.0	564	SEGC68	-756.8 , 729.0
515	SEGB52	1656.8 , 729.0	565	SEGA69	-801.8 , 729.0
516	SEGC52	1611.8 , 729.0	566	SEGB69	-846.8 , 729.0
517	SEGA53	1566.8 , 729.0	567	SEGC69	-891.8 , 729.0
518	SEGB53	1521.8 , 729.0	568	SEGA70	-936.8 , 729.0
519	SEGC53	1476.8 , 729.0	569	SEGB70	-981.8 , 729.0
520	SEGA54	1431.8 , 729.0	570	SEGC70	-1026.8 , 729.0
521	SEGB54	1386.8 , 729.0	571	SEGA71	-1071.8 , 729.0
522	SEGC54	1341.8 , 729.0	572	SEGB71	-1116.8 , 729.0
523	SEGA55	1296.8 , 729.0	573	SEGC71	-1161.8 , 729.0
524	SEGB55	1251.8 , 729.0	574	SEGA72	-1206.8 , 729.0
525	SEGC55	1206.8 , 729.0	575	SEGB72	-1251.8 , 729.0
526	SEGA56	1161.8 , 729.0	576	SEGC72	-1296.8 , 729.0
527	SEGB56	1116.8 , 729.0	577	SEGA73	-1341.8 , 729.0
528	SEGC56	1071.8 , 729.0	578	SEGB73	-1386.8 , 729.0
529	SEGA57	1026.8 , 729.0	579	SEGC73	-1431.8 , 729.0
530	SEGB57	981.8 , 729.0	580	SEGA74	-1476.8 , 729.0
531	SEGC57	936.8 , 729.0	581	SEGB74	-1521.8 , 729.0
532	SEGA58	891.8 , 729.0	582	SEGC74	-1566.8 , 729.0
533	SEGB58	846.8 , 729.0	583	SEGA75	-1611.8 , 729.0
534	SEGC58	801.8 , 729.0	584	SEGB75	-1656.8 , 729.0
535	SEGA59	756.8 , 729.0	585	SEGC75	-1701.8 , 729.0
536	SEGB59	711.8 , 729.0	586	SEGA76	-1746.8 , 729.0
537	SEGC59	666.8 , 729.0	587	SEGB76	-1791.8 , 729.0
538	SEGA60	621.8 , 729.0	588	SEGC76	-1836.8 , 729.0
539	SEGB60	576.8 , 729.0	589	SEGA77	-1881.8 , 729.0
540	SEGC60	531.8 , 729.0	590	SEGB77	-1926.8 , 729.0
541	SEGA61	486.8 , 729.0	591	SEGC77	-1971.8 , 729.0
542	SEGB61	441.8 , 729.0	592	SEGA78	-2016.8 , 729.0
543	SEGC61	396.8 , 729.0	593	SEGB78	-2061.8 , 729.0
544	SEGA62	351.8 , 729.0	594	SEGC78	-2106.8 , 729.0
545	SEGB62	306.8 , 729.0	595	SEGA79	-2151.8 , 729.0
546	SEGC62	261.8 , 729.0	596	SEGB79	-2196.8 , 729.0
547	SEGA63	216.8 , 729.0	597	SEGC79	-2241.8 , 729.0
548	SEGB63	171.8 , 729.0	598	SEGA80	-2286.8 , 729.0
549	SEGC63	126.8 , 729.0	599	SEGB80	-2331.8 , 729.0
550	SEGA64	-126.8 , 729.0	600	SEGC80	-2376.8 , 729.0

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
601	SEGA81	-2421.8 , 729.0	651	SEGC97	-4671.8 , 729.0
602	SEGB81	-2466.8 , 729.0	652	SEGA98	-4716.8 , 729.0
603	SEGC81	-2511.8 , 729.0	653	SEGB98	-4761.8 , 729.0
604	SEGA82	-2556.8 , 729.0	654	SEGC98	-4806.8 , 729.0
605	SEGB82	-2601.8 , 729.0	655	SEGA99	-4851.8 , 729.0
606	SEGC82	-2646.8 , 729.0	656	SEGB99	-4896.8 , 729.0
607	SEGA83	-2691.8 , 729.0	657	SEGC99	-4941.8 , 729.0
608	SEGB83	-2736.8 , 729.0	658	SEGA100	-4986.8 , 729.0
609	SEGC83	-2781.8 , 729.0	659	SEGB100	-5031.8 , 729.0
610	SEGA84	-2826.8 , 729.0	660	SEGC100	-5076.8 , 729.0
611	SEGB84	-2871.8 , 729.0	661	SEGA101	-5121.8 , 729.0
612	SEGC84	-2916.8 , 729.0	662	SEGB101	-5166.8 , 729.0
613	SEGA85	-2961.8 , 729.0	663	SEGC101	-5211.8 , 729.0
614	SEGB85	-3006.8 , 729.0	664	SEGA102	-5256.8 , 729.0
615	SEGC85	-3051.8 , 729.0	665	SEGB102	-5301.8 , 729.0
616	SEGA86	-3096.8 , 729.0	666	SEGC102	-5346.8 , 729.0
617	SEGB86	-3141.8 , 729.0	667	SEGA103	-5391.8 , 729.0
618	SEGC86	-3186.8 , 729.0	668	SEGB103	-5436.8 , 729.0
619	SEGA87	-3231.8 , 729.0	669	SEGC103	-5481.8 , 729.0
620	SEGB87	-3276.8 , 729.0	670	SEGA104	-5526.8 , 729.0
621	SEGC87	-3321.8 , 729.0	671	SEGB104	-5571.8 , 729.0
622	SEGA88	-3366.8 , 729.0	672	SEGC104	-5616.8 , 729.0
623	SEGB88	-3411.8 , 729.0	673	SEGA105	-5661.8 , 729.0
624	SEGC88	-3456.8 , 729.0	674	SEGB105	-5706.8 , 729.0
625	SEGA89	-3501.8 , 729.0	675	SEGC105	-5751.8 , 729.0
626	SEGB89	-3546.8 , 729.0	676	SEGA106	-5796.8 , 729.0
627	SEGC89	-3591.8 , 729.0	677	SEGB106	-5841.8 , 729.0
628	SEGA90	-3636.8 , 729.0	678	SEGC106	-5886.8 , 729.0
629	SEGB90	-3681.8 , 729.0	679	SEGA107	-5931.8 , 729.0
630	SEGC90	-3726.8 , 729.0	680	SEGB107	-5976.8 , 729.0
631	SEGA91	-3771.8 , 729.0	681	SEGC107	-6021.8 , 729.0
632	SEGB91	-3816.8 , 729.0	682	SEGA108	-6066.8 , 729.0
633	SEGC91	-3861.8 , 729.0	683	SEGB108	-6111.8 , 729.0
634	SEGA92	-3906.8 , 729.0	684	SEGC108	-6156.8 , 729.0
635	SEGB92	-3951.8 , 729.0	685	SEGA109	-6201.8 , 729.0
636	SEGC92	-3996.8 , 729.0	686	SEGB109	-6246.8 , 729.0
637	SEGA93	-4041.8 , 729.0	687	SEGC109	-6291.8 , 729.0
638	SEGB93	-4086.8 , 729.0	688	SEGA110	-6336.8 , 729.0
639	SEGC93	-4131.8 , 729.0	689	SEGB110	-6381.8 , 729.0
640	SEGA94	-4176.8 , 729.0	690	SEGC110	-6426.8 , 729.0
641	SEGB94	-4221.8 , 729.0	691	SEGA111	-6471.8 , 729.0
642	SEGC94	-4266.8 , 729.0	692	SEGB111	-6516.8 , 729.0
643	SEGA95	-4311.8 , 729.0	693	SEGC111	-6561.8 , 729.0
644	SEGB95	-4356.8 , 729.0	694	SEGA112	-6606.8 , 729.0
645	SEGC95	-4401.8 , 729.0	695	SEGB112	-6651.8 , 729.0
646	SEGA96	-4446.8 , 729.0	696	SEGC112	-6696.8 , 729.0
647	SEGB96	-4491.8 , 729.0	697	SEGA113	-6741.8 , 729.0
648	SEGC96	-4536.8 , 729.0	698	SEGB113	-6786.8 , 729.0
649	SEGA97	-4581.8 , 729.0	699	SEGC113	-6831.8 , 729.0
650	SEGB97	-4626.8 , 729.0	700	SEGA114	-6876.8 , 729.0

Pin No.	Pad Name	Coordinate (X, Y)	Pin No.	Pad Name	Coordinate (X, Y)
701	SEGB114	-6921.8 , 729.0	751	COM17	-9171.8 , 729.0
702	SEGC114	-6966.8 , 729.0	752	COM19	-9216.8 , 729.0
703	SEGA115	-7011.8 , 729.0	753	COM21	-9261.8 , 729.0
704	SEGB115	-7056.8 , 729.0	754	COM23	-9306.8 , 729.0
705	SEGC115	-7101.8 , 729.0	755	COM25	-9351.8 , 729.0
706	SEGA116	-7146.8 , 729.0	756	COM27	-9396.8 , 729.0
707	SEGB116	-7191.8 , 729.0	757	COM29	-9441.8 , 729.0
708	SEGC116	-7236.8 , 729.0	758	COM31	-9486.8 , 729.0
709	SEGA117	-7281.8 , 729.0	759	COM33	-9531.8 , 729.0
710	SEGB117	-7326.8 , 729.0	760	COM35	-9576.8 , 729.0
711	SEGC117	-7371.8 , 729.0	761	COM37	-9621.8 , 729.0
712	SEGA118	-7416.8 , 729.0	762	COM39	-9666.8 , 729.0
713	SEGB118	-7461.8 , 729.0	763	COM41	-9711.8 , 729.0
714	SEGC118	-7506.8 , 729.0	764	COM43	-9756.8 , 729.0
715	SEGA119	-7551.8 , 729.0	765	COM45	-9801.8 , 729.0
716	SEGB119	-7596.8 , 729.0	766	NC11	-9846.8 , 729.0
717	SEGC119	-7641.8 , 729.0	767	NC12	-10159.0 , 720.0
718	SEGA120	-7686.8 , 729.0	768	COM47	-10159.0 , 675.0
719	SEGB120	-7731.8 , 729.0	769	COM49	-10159.0 , 630.0
720	SEGC120	-7776.8 , 729.0	770	COM51	-10159.0 , 585.0
721	SEGA121	-7821.8 , 729.0	771	COM53	-10159.0 , 540.0
722	SEGB121	-7866.8 , 729.0	772	COM55	-10159.0 , 495.0
723	SEGC121	-7911.8 , 729.0	773	COM57	-10159.0 , 450.0
724	SEGA122	-7956.8 , 729.0	774	COM59	-10159.0 , 405.0
725	SEGB122	-8001.8 , 729.0	775	COM61	-10159.0 , 360.0
726	SEGC122	-8046.8 , 729.0	776	COM63	-10159.0 , 315.0
727	SEGA123	-8091.8 , 729.0	777	COM65	-10159.0 , 270.0
728	SEGB123	-8136.8 , 729.0	778	COM67	-10159.0 , 225.0
729	SEGC123	-8181.8 , 729.0	779	COM69	-10159.0 , 180.0
730	SEGA124	-8226.8 , 729.0	780	COM71	-10159.0 , 135.0
731	SEGB124	-8271.8 , 729.0	781	COM73	-10159.0 , 90.0
732	SEGC124	-8316.8 , 729.0	782	COM75	-10159.0 , 45.0
733	SEGA125	-8361.8 , 729.0	783	COM77	-10159.0 , 0.0
734	SEGB125	-8406.8 , 729.0	784	COM79	-10159.0 , -45.0
735	SEGC125	-8451.8 , 729.0	785	COM81	-10159.0 , -90.0
736	SEGA126	-8496.8 , 729.0	786	COM83	-10159.0 , - 135.0
737	SEGB126	-8541.8 , 729.0	787	COM85	-10159.0 , -180.0
738	SEGC126	-8586.8 , 729.0	788	COM87	-10159.0 , -225.0
739	SEGA127	-8631.8 , 729.0	789	COM89	-10159.0 , -270.0
740	SEGB127	-8676.8 , 729.0	790	COM91	-10159.0 , -315.0
741	SEGC127	-8721.8 , 729.0	791	COM93	-10159.0 , -360.0
742	NC10	-8766.8 , 729.0	792	COM95	-10159.0 , -405.0
743	COM1	-8811.8 , 729.0	793	COM97	-10159.0 , -450.0
744	COM3	-8856.8 , 729.0	794	COM99	-10159.0 , -495.0
745	COM5	-8901.8 , 729.0	795	COM101	-10159.0 , -540.0
746	COM7	-8946.8 , 729.0	796	COM103	-10159.0 , -585.0
747	COM9	-8991.8 , 729.0	797	COM105	-10159.0 , -630.0
748	COM11	-9036.8 , 729.0	798	COM107	-10159.0 , -675.0
749	COM13	-9081.8 , 729.0	799	NC13	-10159.0 , -720.0
750	COM15	-9126.8 , 729.0			

4 Functional Block Diagram

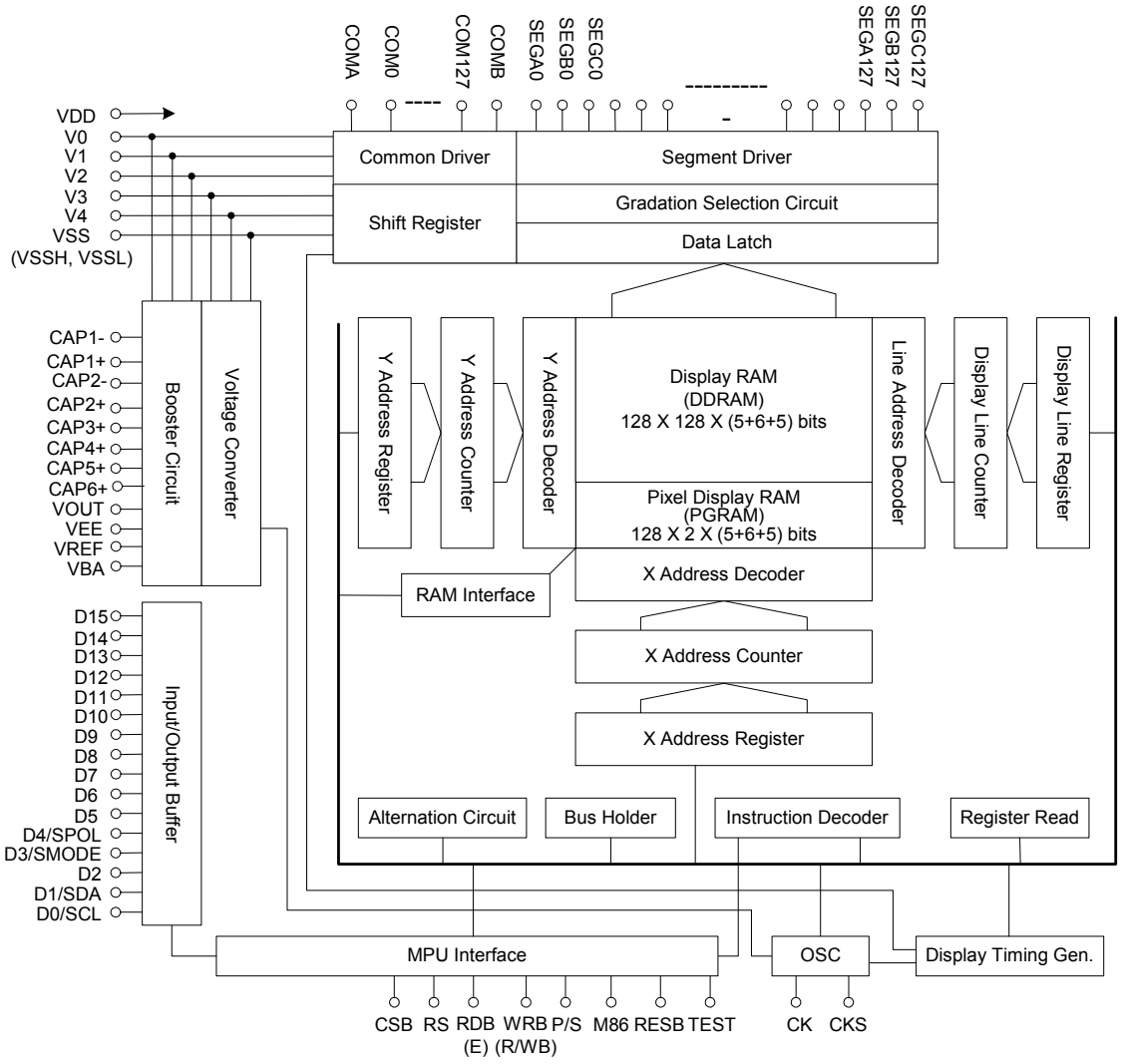


Figure 2. System Block Diagram

5 Power Circuit Block Diagram

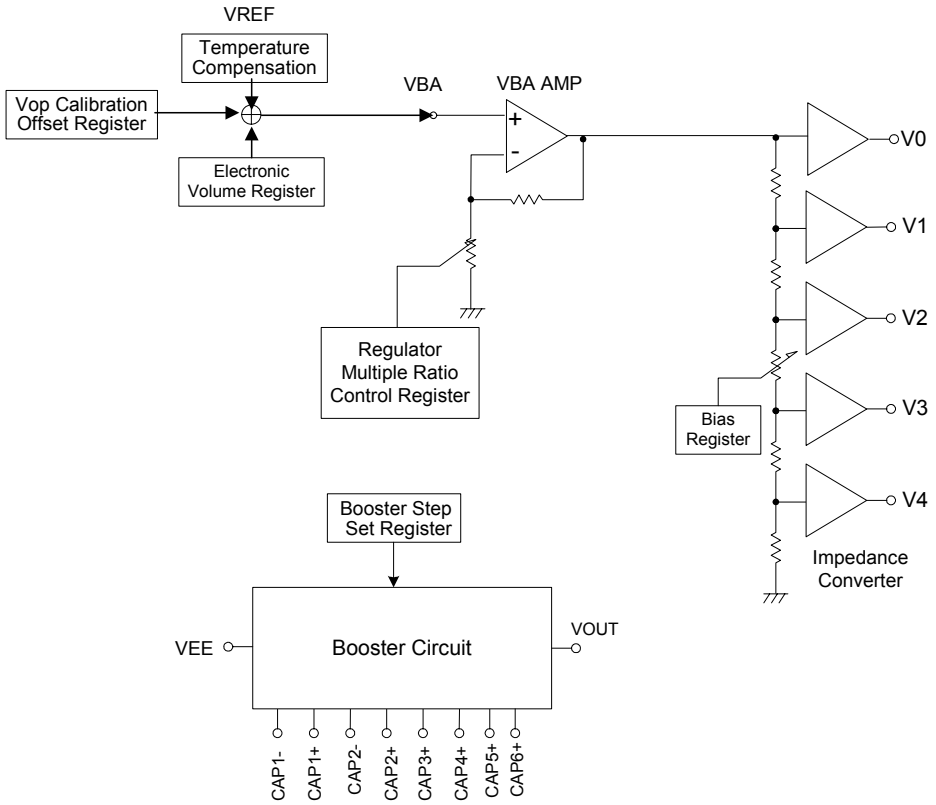


Figure 3. Power Circuit Block Diagram

6 Pin Description

6.1 Power Supply Pins

Symbol	I/O	Description
VDD	–	Power supply pin for logic circuit, +2.2V to 3.3V
VSSL	–	Ground pin for logic circuit, connected to 0V
VSSH	–	Ground pin for high voltage circuit, connected to 0V
V0 V1 V2 V3 V4	–	Bias power supply pin for LCD drive voltage When using an external power supply, convert the impedance by using resistance-division of the LCD drive power supply or operation amplifier before adding voltage to the pins. These voltages should have the following relationship: VSS<V4<V3<V2<V1<V0 When the internal power supply circuit is active, these voltages are generated by the built-in booster and voltage converter. Then, you must connect each capacitor to VSS.

6.2 LCD Power Supply Circuit Pins

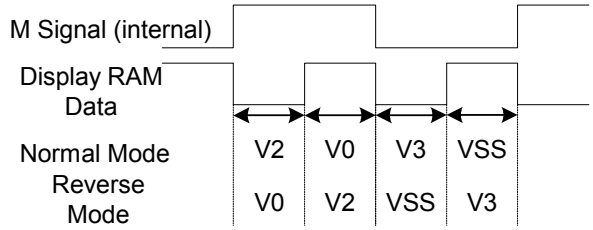
Symbol	I/O	Description
CAP1+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP1- and CAP1+.
CAP1-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP1- and CAP1+.
CAP2+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP2- and CAP2+.
CAP2-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP2- and CAP2+.
CAP3+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP1- and CAP3+.
CAP4+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP2- and CAP4+.
CAP5+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP1- and CAP5+.
CAP6+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP2- and CAP6+.
VEE	–	Voltage supply pin for the booster circuit. Usually the same voltage level as VDD. In the case of TCP, draw it at a separate terminal.
VOUT	O	Output pin of boosted voltage in the built-in booster. The capacitor must be connected between this pin and the VSS.
VBA	O	Output pin for regulator voltage of VBA AMP.
VREF	O	Output pin for temperature compensation output voltage.

6.3 System Bus Pins

Symbol	I/O	Description
RESB	I	Reset input pin. When RESB is “L”, initialization is executed.
D0/SCL D1/SDA D2 D3/SMODE D4.SPOL D5-D7	I/O	Data bus / Signal interface related pins. When parallel interface is selected (P/S = “H”), the D7-D0 are 8-bit bi-directional data busses, connected to the MPU data bus. *When serial interface is selected (P/S = “L”), D0 and D1 (SCL, SDA) are used as serial interface pins. SCL: Input pin for data transfer clock SDA: Serial data input pin SMODE: Serial transfer mode select pin SPOL: RS pole select pin when 3-wires serial interface is selected. SDA data is latched at the rising edge of SCL. Internal serial/parallel conversion into 8-bit data occurs at the rising edge of the 8th clock of SCL. After completing data transfer, or when making no access, be sure to set SCL to “L”.
D8-D15	I/O	8-bit bi-directional bus. Connected to MPU data bus. Used as a data bus for the upper 8 pins in the 16-bit access mode.
CSB	I	Chip Select input pin. CSB = “L”: accepts access from the MPU CSB = “H”: denies access from the MPU
RS	I	RAM/Register select input pin. RS = “0”: D7-D0 are display RAM data RS = “1”: D7-D0 are control register data
RDB (E)	I	Read/Write control pin. Select 80-family MPU type (M86 = “L”) The RDB is a data read signal. When RDB is “L”, D7-D0 are in an output status. Select 68-family MPU type (M86 = “H”) R/WB = “H”: When E is “H”, D7-D0 are in an output status. R/WB = “L”: The data on D7-D0 are latched at the falling edge of the E signal.
WRB (R/WB)	I	Read/Write control pin. Select 80-family MPU type (M86 = “L”) The WRB is a data write signal. The data on D7-D0 are latched at the rising edge of the WRB signal. Select 68-family MPU type (M86 = “H”) Read/Write control input pin. R/W = “H”: Read R/W = “L”: Write
M86	I	MPU interface type selecting input pin. M86 = “H”: 68-family interface M86 = “L”: 80-family interface Fixed at either “H” or “L”

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>TEST</td><td>I</td><td>For testing. Fix to “L”</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel/Serial interface select pin.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data Identification</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>CSB</td><td>RS</td><td>D0-D7</td><td>RDB, WRB</td><td>-</td></tr>
<tr><td>L</td><td>CSB</td><td>RS</td><td>SDA</td><td>Write only</td><td>SCL</td></tr>
</table>
P/S = “H”: For parallel interface
P/S = “L”: For serial interface. Fix D15-D5 pins to Hi-Z, and fix RDB and WRB pins to either “H” or “L”</td></tr>
</table>

6.4 LCD Drive Circuit Signals

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEGA0-A127
SEGB0-B127
SEGC0-C127</td><td>O</td><td>Segment output pins for the LCD driver.
Basing on the Display RAM data, non-lighted at “0”, lighted at “1” (Normal Mode), non-lighted at “1”, lighted at “0” (Reverse Mode) and by a combination of M signal and display data, one signal level among V0, V2, V3 and VSS signal level is selected.
(For Monochrome Display)
 
</td></tr>
<tr><td>COM0-
COM127</td><td>O</td><td>Common output pins for the LCD drivers. By a combination of the scanning data and M signal, one signal level among V0, V1, V4 and VSS signal level is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output Level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>COMA</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
<tr><td>COMB</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
</table>

6.5 Oscillating Circuit Pin

Symbol	I/O	Description
CKS	I	Display timing clock source select input pin. CKS = "H": Use external clock from the CK pin. CKS = "L": Use internal oscillator clock. In the case of TCP, draw it as a separate terminal.
CK	I	External clock input pin for display timing (CKS=1). When using internal oscillator clock, connect CK to VSS (CKS=0).

6.6 EEPROM Power Pin

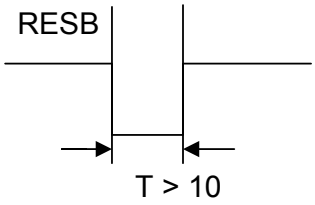
Symbol	I/O	Description
VPP	I	External power supply pin for EEPROM programming or erasing. When using external power for EEPROM programming or erasing, the power supply is 16V~18V.

7 Functional Description

7.1 MPU Interface

7.1.1 Reset Pin Description (RESB)

Hold the RESB low for at least 10μs, then the EM65571 accepts this reset command.



7.1.2 Selection of Interface Type

The EM65571 transfers data through an 8-bit parallel I/O (D7-D0), 16-bit parallel I/O (D15-D0) or serial data input (SDA, SCL). The parallel interface or serial interface can be selected by the state of the P/S pin. When selecting serial interface, data reading cannot be performed, only data writing can operate.

P/S	I/F Type	CSB	RS	RDB	WRB	M86	SDA	SCL	Data
H	Parallel	CSB	RS	RDB	WRB	M86	-	-	D7~D0 (D15~D0)
L	Serial	CSB	RS	-	-	-	SDA	SCL	-

7.1.3 Parallel Input

When parallel interface is selected with the P/S pin, the EM65571 allows data to be transferred in parallel to an 8-bit/16-bit MPU through the data bus. For the 8-bit/16-bit MPU, either the 80-family MPU interface or the 68-family MPU interface can be selected with the M86 pin.

M86	MPU Type	CSB	RS	RDB	WRB	Data
H	68-family MPU	CSB	RS	E	R/WB	D7~D0 (D15~D0)
L	80-family MPU	CSB	RS	RDB	WRB	D0~D7 (D15~D0)

7.1.4 Read/Write Functions of the Registers and Display RAM

The EM65571 has four read/write functions during parallel interface mode. Each read/write function is selected by combinations of RS, RDB and WRB signals.

RS	68-family R/WB	80-family		Function
		RDB	WRB	
1	1	0	1	Read internal Register
1	0	1	0	Write internal Register
0	1	0	1	Read display data
0	0	1	0	Write display data

7.1.5 Serial Interface

The EM65571 has two types of serial interface. One is a 3-wire type serial interface; the other one is a 4-wire type serial interface. The choice whether 3-wire or 4-wire is determined by the SMODE pin.

SMODE = “L”: 4-wires serial interface

SMODE = “H”: 3-wires serial interface

7.1.6 4-wire Serial Interface

When chip select is active (CSB = “L”), 4-wire type serial interface can work through the SDA and SCL input pins. When chip select is inactive (CSB = “H”), the internal shift register and counter are reset to the initial condition. Serial data SDA is input sequentially in the order from D7 to D0 at the rising edge of the serial clock (SCL) and is converted into 8-bit parallel data (by serial to parallel conversion) at the rising edge of the 8th serial clock, processed in accordance with the data. The identification whether serial data input (SDA), display data or control register data is determined by input to the RS pin.

RS = “L” : display RAM data

RS = “H” : control register data

After completion of an 8-bit data transfer, or when making no access, be sure to set the serial clock input (SCL) to “L”. Care of the SDA and SCL signals against external noise should be taken into consideration during board wiring. To prevent transfer error due to external noise, release the chip select (CSB = “H”) after every completion of an 8-bit data transfer.

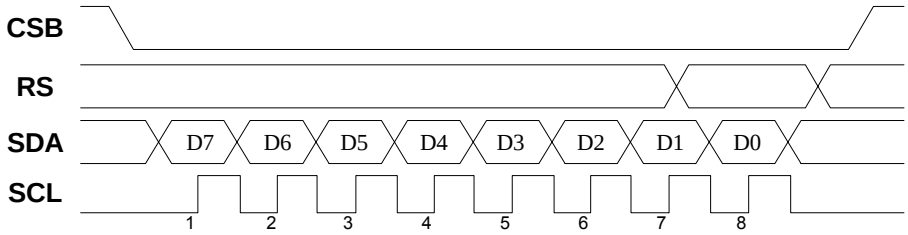


Figure 4. 4-wire Type Serial Interface

7.1.7 3-Wire Type Serial Interface

When chip select is active (CSB = “L”), 3-wire type serial interface can work through the SDA and SCL input pins. When chip select is inactive (CSB = “H”), the internal shift register and counter are reset to the initial condition. Serial data SDA is input sequentially in the order from RS, D7 to D0 at the rising edge of the serial clock (SCL) and is converted into 9-bit parallel data (by serial to parallel conversion) at the rising edge of the 9th serial clock. The identification whether serial data input (SDA), display data or control register data is determined by the first serial input data (RS) and SPOL pin as follows.

SPOL = “0”		SPOL = “1”	
RS	Display RAM/Register	RS	Display RAM/Register
0	Display RAM Data	0	Control Register Data
1	Control Register Data	1	Display RAM Data

After completion of a 9-bit data transfer, or when making no access, be sure to set the serial clock input (SCL) to “L”. Care of the SDA and SCL signals against external noise should be taken into consideration during board wiring. To prevent transfer error due to external noise, release the chip select (CSB = “H”) after every completion of 9-bit data transfer.

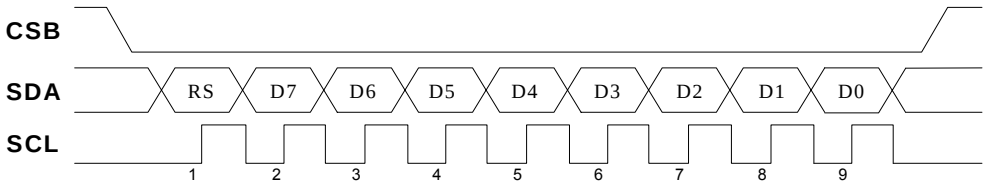


Figure 5. 3-wire Type Serial Interface

7.2 Data Write to Display RAM and Control Register

The data write to display RAM and Control Register use almost the same procedure, only different settings of RS that select access to the object.

RS = “L”: Display RAM data

RS = “H”: Control register data

In the case of the 80-family MPU, the data is written at the rising edge of WRB. In the case of the 68-family MPU, the data is written at the falling edge of signal E.

Data Write Operation

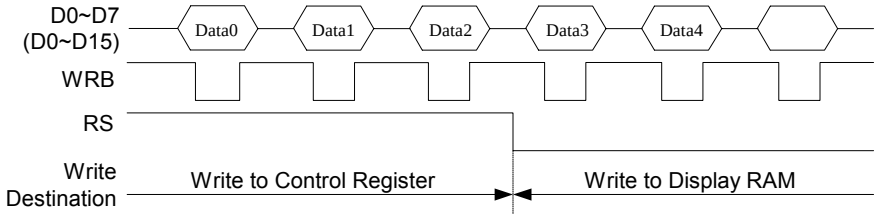


Figure 6. Data Write Operation

7.3 Internal Register Read

In the case of display RAM read operation, you need to perform a dummy read one time. The designated address data is not output to read operation immediately after the address is set to AX or AY register, but is output when the second data is read. Dummy read is always required one time after an address set and write cycle.

Read Display RAM Operation

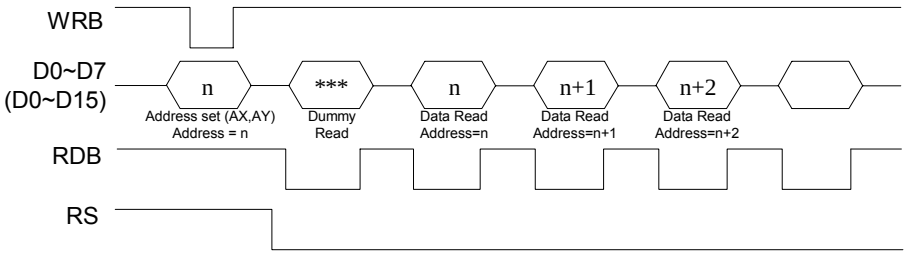


Figure 7. Read Display RAM Operation

The EM65571 can read the control registers, in case of control register read operation, the data bus upper nibble (D7-D4) is used for register address (0 to FH). A maximum of 16 registers can be accessed directly. Since there are more than 16 registers, the EM65571 has a register bank control. The RE register sets the bank number to be accessed. And the RE address is 0FH, in any bank that can access RE register, 4-steps are needed to read a specific register.

1. Write 04H to the RE register to access the RA register.
2. Write the specific register address to the RA register.
3. Write specific register bank to RE register.
4. Read specific register contents.

Register Read Operation

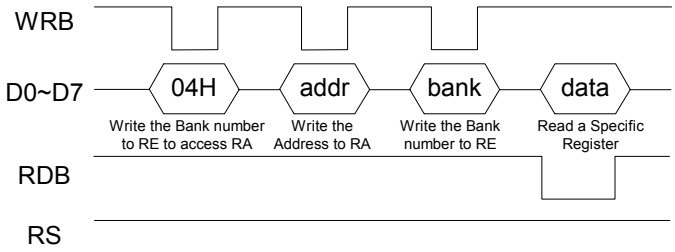


Figure 8. Register Read Operation

7.4 16-Bit Data Access to Display RAM

The EM65571 corresponds to 8-bit and 16-bit bus size access.

The data bus size can be selected by the WLS register.

WLS = “0”: 8-bit bus size

WLS = “1”: 16-bit bus size

In the 16-bit access mode, in accessing the control register, use the low-byte data bus (D7~D0). High byte data bus (D15~D8) are not used in internal circuits when reading the control register using 16-bit bus. Register values are output to D3-D0 and D15-D4 output “H”.

7.5 Fast Burst RAM Write Function

The EM65571 has a built-in fast burst RAM write function. The burst mode transfers 32 bits of data in a block at once, so it can decrease half the access time needed for common standard RAM write functions (16 bits data bus). The burst RAM write function is suitable for frequently rewriting data such as displaying color animation.

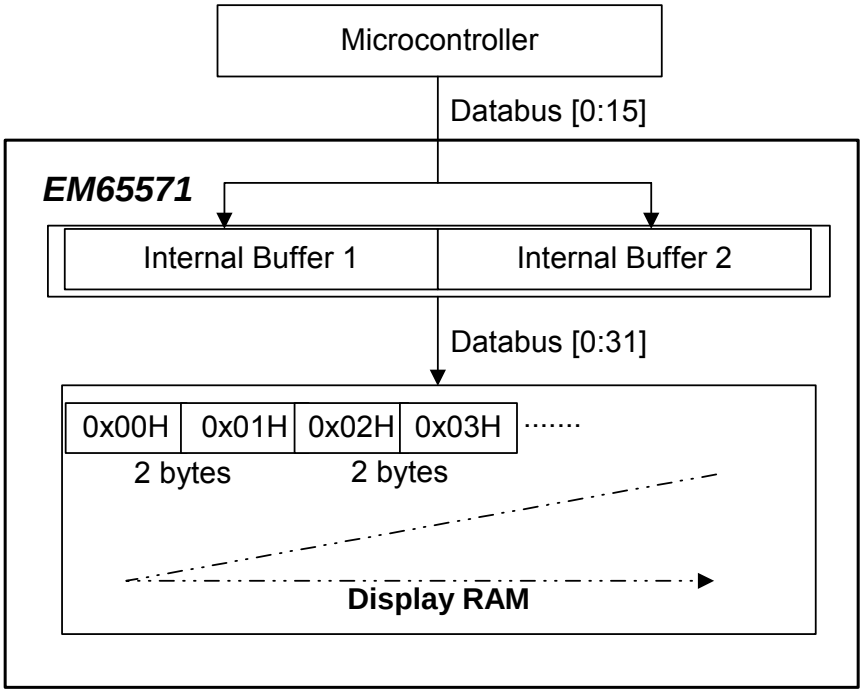


Figure 9. Burst RAM Write Operation

7.6 Display Start Address Register

This register determines the Y-address of the display RAM corresponding to the display start line. The display RAM data addressed by the Display Start Address register is output to the common driver start line. The actual common start line of the LCD panel depends on the Display Start Common register and the SHIFT bit of the Display Control register. The registers are preset every time the FLM signal varies in the display line counter. The line counter counts up when synchronized with the LP input and generates line addresses which are read out sequentially as 384 bits of data from display RAM to the LCD driver circuit.

7.7 Display RAM Addressing

The EM65571 has a built-in bit mapped display RAM. The display RAM consists of 2048 bits (16 bits*128) in the X-direction and 128 bits in the Y-direction. In the gradation display mode, the EM65571 provides segment driver output for 48-gradation display using 6 bits. The three outputs of the segment driver can be used for one pixel of RGB. When connected to an STN color LCD panel, the EM65571 can display 128*128 pixels with 65K colors (48 gradation * 48 gradation * 48 gradation). The address area in the X-direction depends on the access bus size. In the X-direction, the X Address register is used to access; and in the Y-direction, the Y Address register is

used to access. Do not specify any address outside of the effective address area in each access mode because it is not permitted.

In Gradation Display Mode (C256="0", 65K="0", 4096 colors)

■ 8-bit Bus Size Access

● WLS="0", ABS="X",HSW="0"

X-address

Y-address	0H	1H	----------	FEH	FFH
0H	4-bit	8-bit		4-bit	8-bit
7FH	4-bit	8-bit		4-bit	8-bit

● WLS="0", ABS="X", HSW="1"

X-address

Y-address	0H	1H	----------	BEH	BFH
0H	8-bit	8-bit		8-bit	8-bit
7FH	8-bit	8-bit		8-bit	8-bit

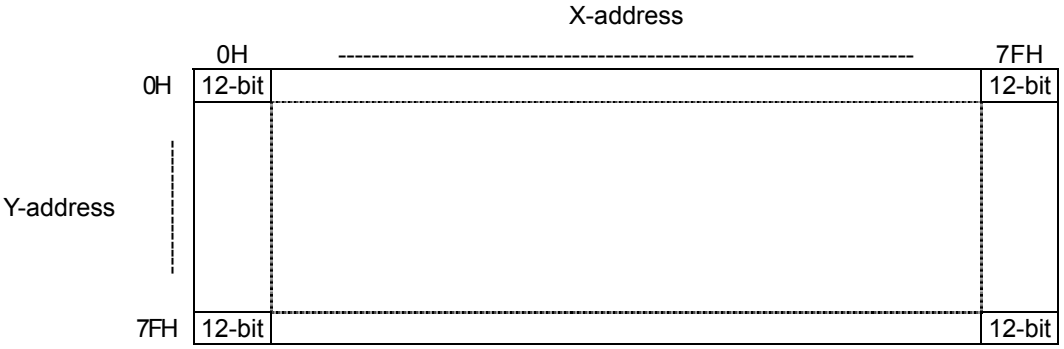
■ 16-bit Bus Size Access

● WLS="1" ABS="0" HSW="X"

X-address

Y-address	0H	----------	7FH
0H	12-bit		12-bit
7FH	12-bit		12-bit

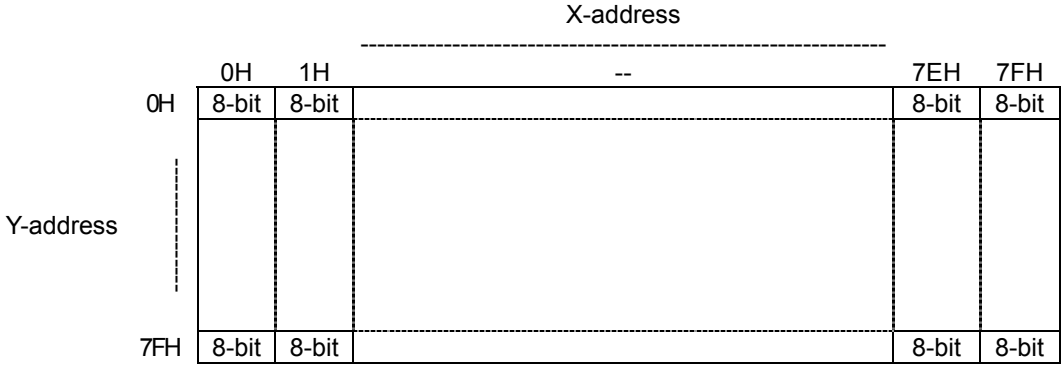
- WLS=”1” ABS=”1” HSW=”X”



In Gradation Display Mode (C256=”1”, 65K=”0”, 256 colors)

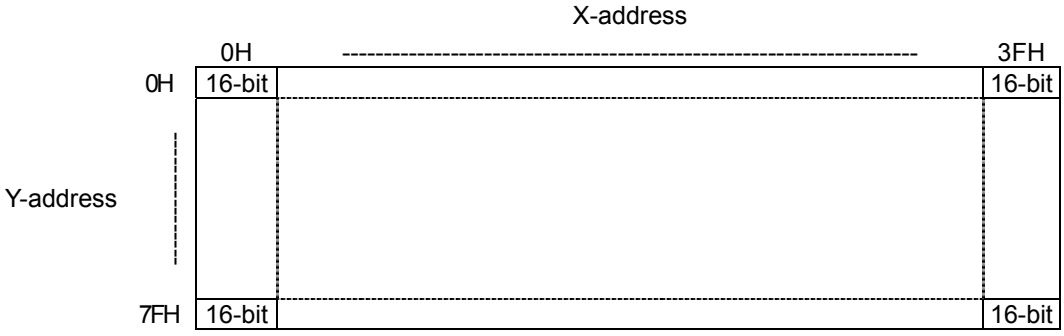
■ 8-bit Bus Size Access

- WLS=”0” ABS=”X” HSW=”X”



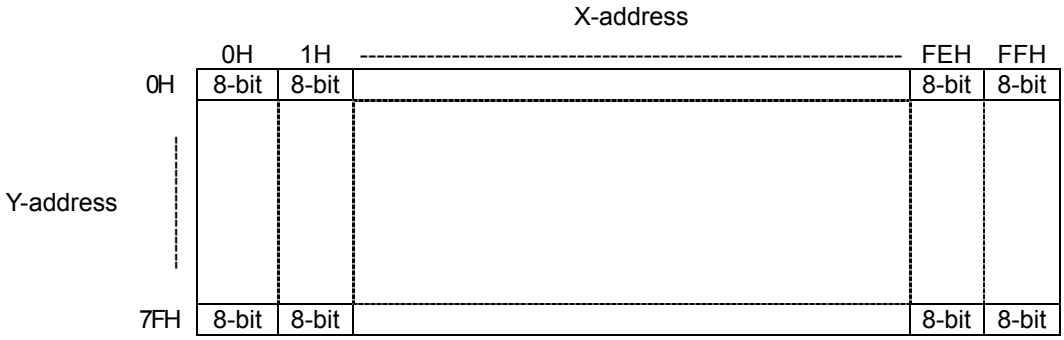
■ 16-bit Bus Size Access

- WLS=”1” ABS=”X” HSW=”X”

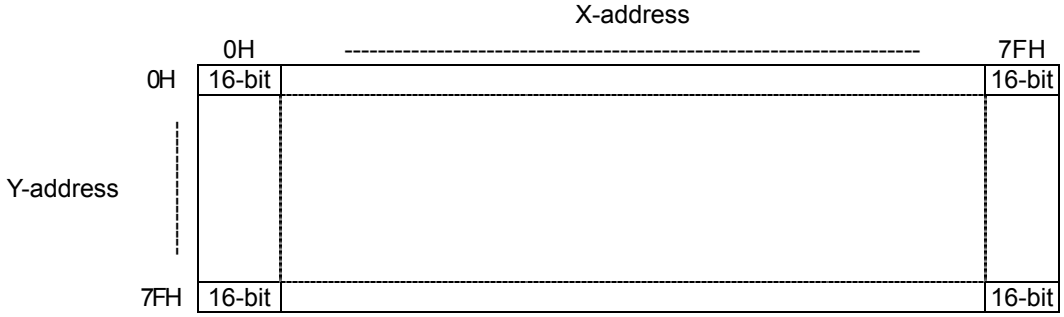


In Gradation Display Mode (C256="0", 65K="1", 65K colors)

- 8-bit Bus Size Access
  - WLS="0"



- 16-bit Bus Size Access
  - WLS="1"



The addresses, X-address and Y-address can be set up so that they can increment automatically with the address control register. The increment is made every time the display RAM is read from or written to in the MPU. In the Y-direction, 384 bits of data are read out to the display data latch circuit by internal operation when the LP rises in a one-line cycle. They are output from the display data latch circuit when the internal signal LP fails. When internal FLM signals output in one frame cycle are at "H", the values in the display start line register are preset in the line counter and the line counter counts up at the falling edge of the internal signal LP. The display line address counter is synchronized with each timing signal of the LCD system to operate and is independent of the address counters X and Y.

7.8 Display RAM Access Using Windows Function

The EM65571 has a window area setting command for specified display RAM area access. To use the window function, you need to set up two positions X and Y addresses. You also need to set up the auto increment mode (AXI="1", AYI="1"). Two position means window start position and window end position. The window start position's X and Y-address set to normal the X-address (AX) and Y-address (AY)

registers. The window end position's X and Y address set to Window the X-end Address (EX) and Window Y-end Address (EY) register. In window function access, you can modify the write access and set to AIM="1". In the case of using window function access, it should be set to the following registers before accessing the RAM.

WIN = "1", AXI="1", AYI="1"

X-Address, Y-Address, Window X-end Address, Window Y-end Address

Moreover, you should keep the following address conditions:

Window end X-address (EX) Window start X-address (AX)

Window end Y-address (EY) Window start Y-address (AY)

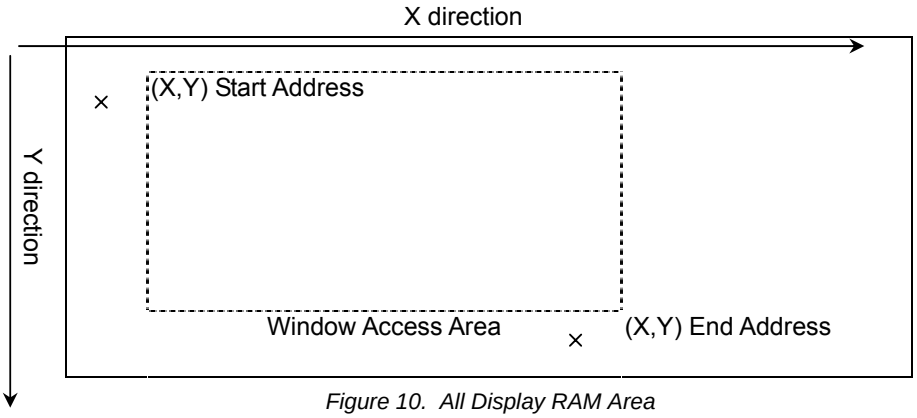


Figure 10. All Display RAM Area

7.9 Display RAM Data and LCD

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are setup as follows.

Normal display (REV=0): RAM data = "0" not lighted

RAM data = "1" lighted

Reverse display (REV=1): RAM data = "0" lighted

RAM data = "1" not lighted

7.10 Segment Display Output Order/Reverse Set up

The order of display output, SEGA0, SEGB0, SEGC0 to SEGA127, SEGB127, and SEGC127 can be reversed. If REF control bit is set to "1", display by reversing access to display the RAM from the MPU by using REF register. This reduces the limitation in placing IC when assembling an LCD panel module.

7.11 Relationship between Display RAM and Address

The Display RAM Block Diagram is shown in the figure below:

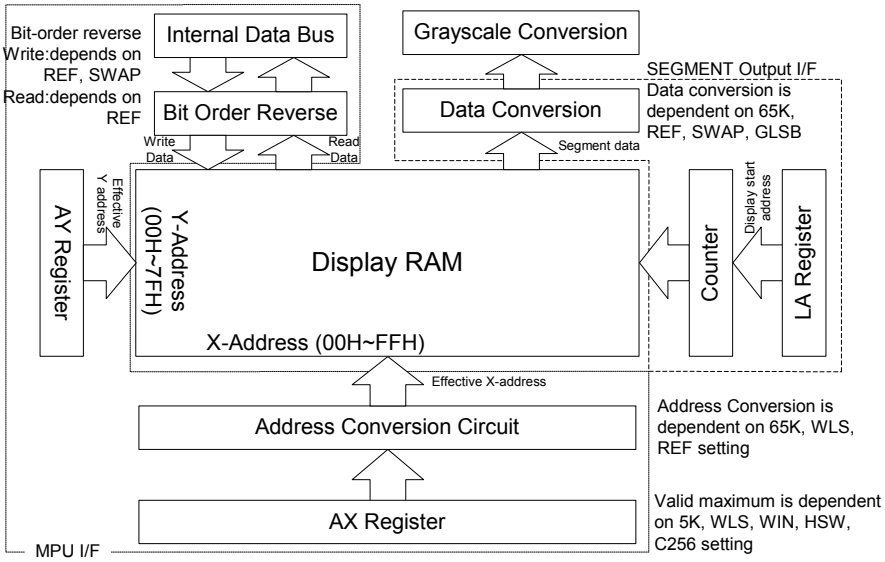


Figure 11. Display RAM Block Diagram

The EM65571 executes address conversion that depends on the control register setting. In case of auto increment mode, usually the AX register is incremented by one. For instance when REF and AXI are both "1", the AX register is incremented by one, but the effective X-address seems to decrement because of address conversion. The effective Y-address use AY register values as it is.

Gradation Mode (256 Color), (C256=1, 65K=0)

(1). 8-bit Mode (WLS=0)

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Palette Bit / Segment Assigned															
*	*	0	0	X=00H								X=7FH							
*	*	1	1	X=7FH								X=00H							
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A		Palette B			Palette C			Palette A		Palette B			Palette C		
				A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3
				SEG A0		SEG B0			SEG C0			SEG A127		SEG B127			SEG C127		

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Palette Bit / Segment Assigned															
*	*	0	1	X=00H								X=7FH							
*	*	1	0	X=7FH								X=00H							
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A		Palette B			Palette C			Palette A		Palette B			Palette C		
				A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3
				SEG C0		SEG B0			SEG A0			SEG C127		SEG B127			SEG A127		

(2). 16-bit Mode (WLS=1)

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Palette Bit / Segment Assigned	
*	*	0	0	X=00H	X=3FH
*	*	1	1	X=3FH	X=00H

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Palette A		Palette B		Palette C			Palette A		Palette B		Palette C					Palette A		Palette B		Palette C			Palette A		Palette B		Palette C			
A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3
SEG A0		SEG B0		SEG C0			SEG A1		SEG B1		SEG C1					SEG A126		SEG B126		SEG C126			SEG A127		SEG B127		SEG C127			

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Palette Bit / Segment Assigned	
*	*	0	1	X=00H	X=3FH
*	*	1	0	X=3FH	X=00H

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Palette A		Palette B		Palette C			Palette A		Palette B		Palette C					Palette A		Palette B		Palette C			Palette A		Palette B		Palette C			
A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3
SEG A1		SEG B1		SEG C1			SEG A0		SEG B0		SEG C0					SEG A127		SEG B127		SEG C127			SEG A126		SEG B126		SEG C126			

Gradation Mode (4096 Color), (C256=0, 65K=0)

(1). 8-bit Mode (WLS="0")

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																					
0	*	0	0	X=00H							X=01H							X=FEH							X=FFH						
0	*	1	1	X=FEH							X=FFH							X=00H							X=01H						
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B			Palette C					Palette A				Palette B			Palette C				
				SEG A0				SEG B0			SEG C0					SEG A127				SEG B127			SEG C127				

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																					
0	*	0	1	X=00H							X=01H							X=FEH							X=FFH						
0	*	1	0	X=FEH							X=FFH							X=00H							X=01H						
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B			Palette C					Palette A				Palette B			Palette C				
				SEG C0				SEG B0			SEG A0					SEG C127				SEG B127			SEG A127				

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																					
1	*	0	0	X=00H							X=01H							X=BEH							X=BFH						
1	*	1	1	X=BEH							X=BFH							X=00H							X=01H						
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3
				Palette A				Palette B			Palette C					Palette A				Palette B			Palette C				
				SEG A0				SEG B0			SEG C0					SEG A127				SEG B127			SEG C127				

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																					
1	*	0	1	X=00H							X=01H					X=BEH							X=BFH			
1	*	1	0	X=BEH							X=BFH					X=00H							X=01H			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3
				Palette A					Palette B			Palette C				Palette A					Palette B			Palette C			
				SEG C0					SEG B0			SEG A0				SEG C127					SEG B127			SEG A127			

(2). 16-bit Mode (WLS="1")

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																					
*	0	0	0	X=00H												X=7FH									
*	0	1	1	X=7FH												X=00H									
				D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15	D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				SEG A0				SEG B0				SEG C0				SEG A127				SEG B127				SEG C127			

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																					
*	0	0	1	X=00H												X=7FH									
*	0	1	0	X=7FH												X=00H									
				D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15	D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				SEG C0				SEG B0				SEG A0				SEG C127				SEG B127				SEG A127			

(3). 16-bit Mode (WLS="1")

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																			
*	1	0	0	X=00H											X=7FH								
*	1	1	1	X=7FH											X=00H								
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				SEG A0				SEG B0				SEG C0				SEG A127				SEG B127				SEG C127			

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																			
*	1	0	1	X=00H											X=7FH								
*	1	1	0	X=7FH											X=00H								
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				SEG C0				SEG B0				SEG A0				SEG C127				SEG B127				SEG A127			

Gradation Mode (65K Color), (C256=0, 65K=1)

(1). 8-bit Mode (WLS=0)

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned																			
*	*	0	0	X=00H								X=01H				X=FEH								X=FFH			
*	*	1	1	X=FEH								X=FFH				X=00H								X=01H			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				SEG A0				SEG B0				SEG C0				SEG A127				SEG B127				SEG C127			

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned															
*	*	0	1	X=00H				X=01H				X=FEH				X=FFH			
*	*	1	0	X=FEH				X=FFH				X=00H				X=01H			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B				Palette C				Palette A			
				SEG C0				SEG B0				SEG A0				SEG C127			

				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				Palette B				Palette C				Palette A				Palette B			
				SEG B127				SEG A127											

(2). 16-bit Mode (WLS=1)

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned															
*	*	0	0	X=00H								X=7FH							
*	*	1	1	X=7FH								X=00H							
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				Palette A				Palette B				Palette C				Palette A			
				SEG A0				SEG B0				SEG C0				SEG A127			

				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				Palette B				Palette C											
				SEG B127				SEG C127											

HSW	ABS	REF	SWAP	X-address / Data Bus / Palette / Segment Assigned															
*	*	0	1	X=00H								X=7FH							
*	*	1	0	X=7FH								X=00H							
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				Palette A				Palette B				Palette C				Palette A			
				SEG C0				SEG B0				SEG A0				SEG C127			

				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				Palette B				Palette C											
				SEG B127				SEG A127											

Data Read and Write Bit Assignment

(1). In 16-bit Data Bus Mode

ABS=0	65K=1	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

ABS=0	65K=0	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D15	D14	D13	D12	1	D10	D9	D8	D7	1	D5	D4	D3	D2	D1	1

ABS=1	65K=0	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	1	1	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

ABS=	65K=0	C256=1	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(2). In 8-bit Data Bus Mode

ABS=*	HSW=*	65K=1	C256=0	Address	00, 02, 04…….FC, FEH								01, 03, 05…….FD, FFH							
				Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
				Read	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

ABS=*	HSW=0	65K=0	C256=0	Address	00, 02, 04…….FC, FEH								01, 03,05…….FD, FFH							
				Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
				Read	1	1	1	1	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

ABS=*	HSW=1	65K=0	C256=0	Address	00, 02, 04…….FC, FEH								01, 03, 05…….FD, FFH							
				Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
				Read	D7	D6	D5	D4	D3	D2	D1	D0	1	1	1	1	D3	D2	D1	D0

ABS=*	HSW=*	65K=0	C256=1	Address	00, 01, 02…….FD, FE, FFH							
				Write	D7	D6	D5	D4	D3	D2	D1	D0
				Read	D7	D6	D5	D4	D3	D2	D1	D0

7.12 Display Data Structure and Gradation Control

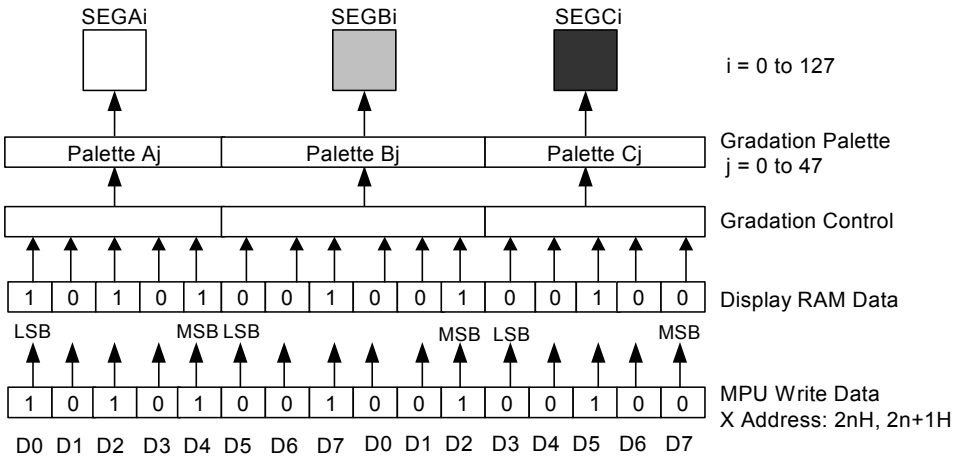
For the purpose of gradation control, one pixel requires multiple bits of display RAM. The EM65571 has 5-bit of data per output to achieve the gradation display.

The three outputs of the segment driver are used for one pixel of RGB, and the EM65571 is connected to an STN color LCD panel. It can display 128*128 pixels with 65K colors (5 bits * 6 bits [5+FRC] * 5 bits). In this case, since the gradation display data is processed by a single access to the memory, the data can be rewritten fast and naturally.

The weighting for each data bit is dependent on the status of the SWAP bit and the REF bit that is selected when data is written to the display RAM.

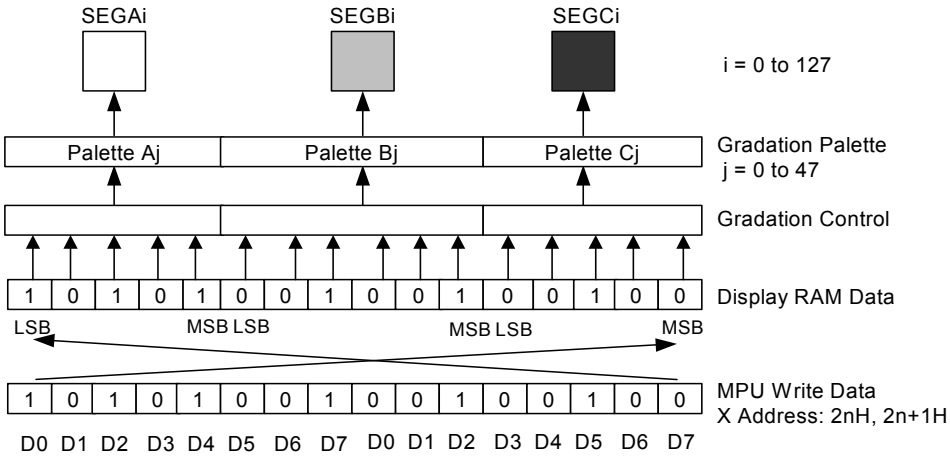
Gradation Mode (65K Color)

- 8-bit Mode
  - (REF, SWAP) = (0, 0) or (1, 1)



Note: Internal X-address

- (REF, SWAP) = (0, 1) or (1, 0)

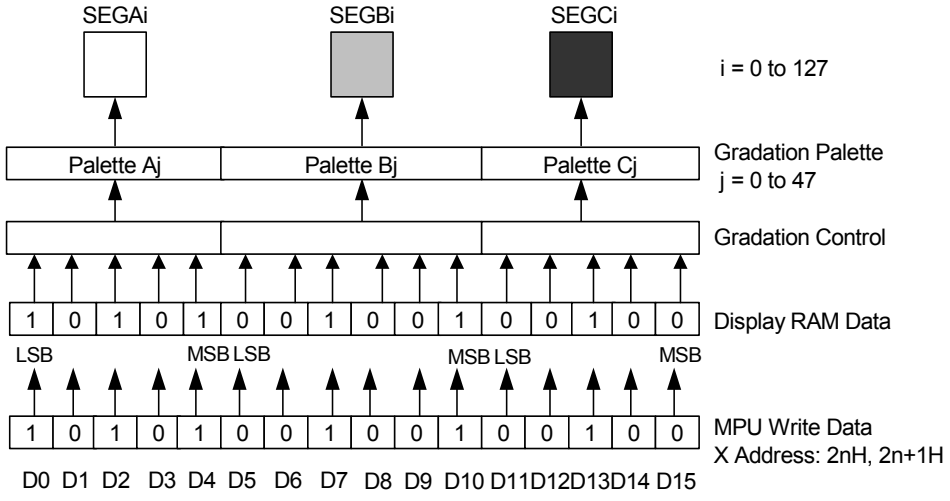


Note: Internal X-address

■ 16-bit Mode

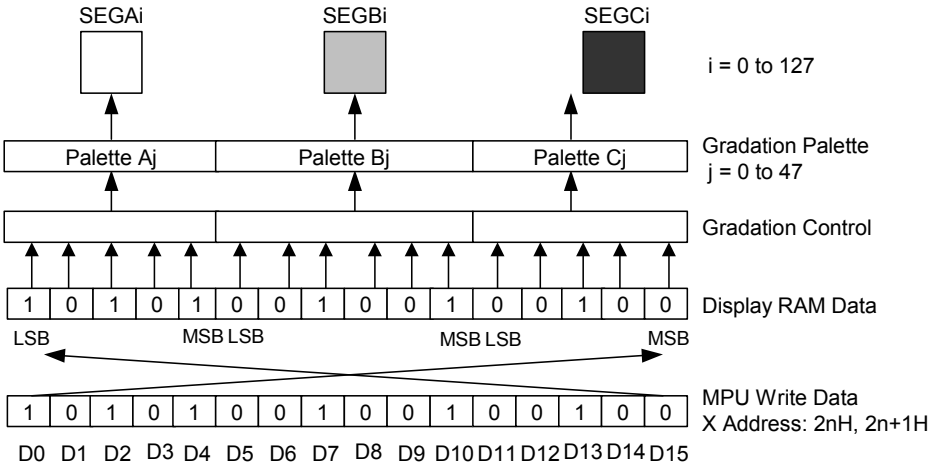
In 16-bits access, the weighting for each data bit is dependent on the status of the SWAP bit and the REF bit that is selected when data is written to the display RAM, as in the case with 8-bits access.

- (REF, SWAP) = (0, 0) or (1, 1)



Note: Internal X-address

- (REF, SWAP) = (0, 1) or (1, 0)

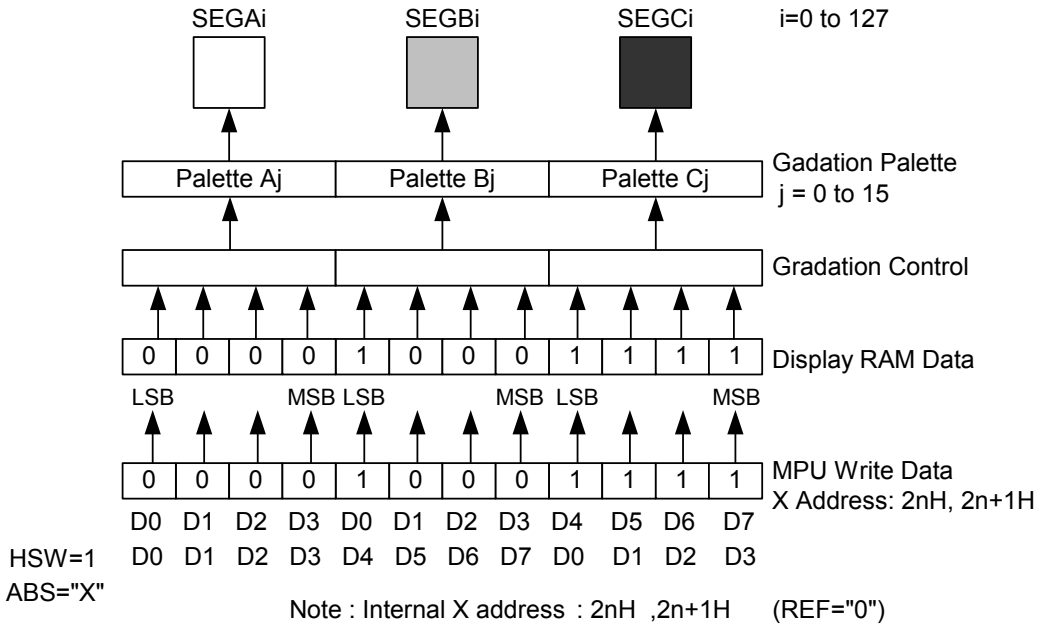


Note: Internal X-address

Gradation Mode (4096 Color)

■ 8-bit mode

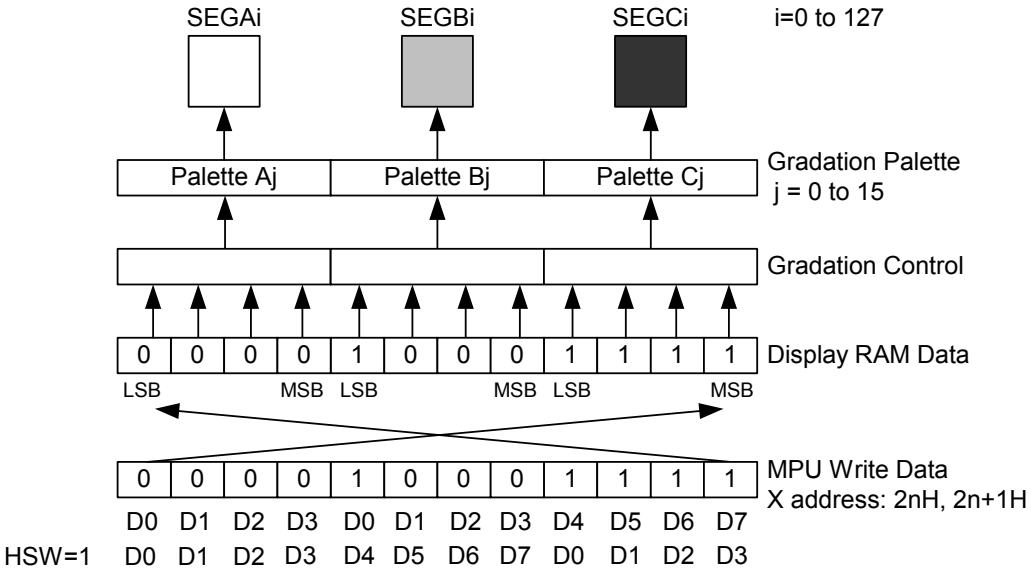
- (REF, SWAP)=(0,0) or (1,1)



Note : Internal X address : 2nH ,2n+1H (REF="0")
: (FE-2n)H , [FF-(2n+1)]H (REF="1")

In HSW=1, Address=00H~BFH

- (REF, SWAP) = (0, 1) or (1, 0)



ABS="X"

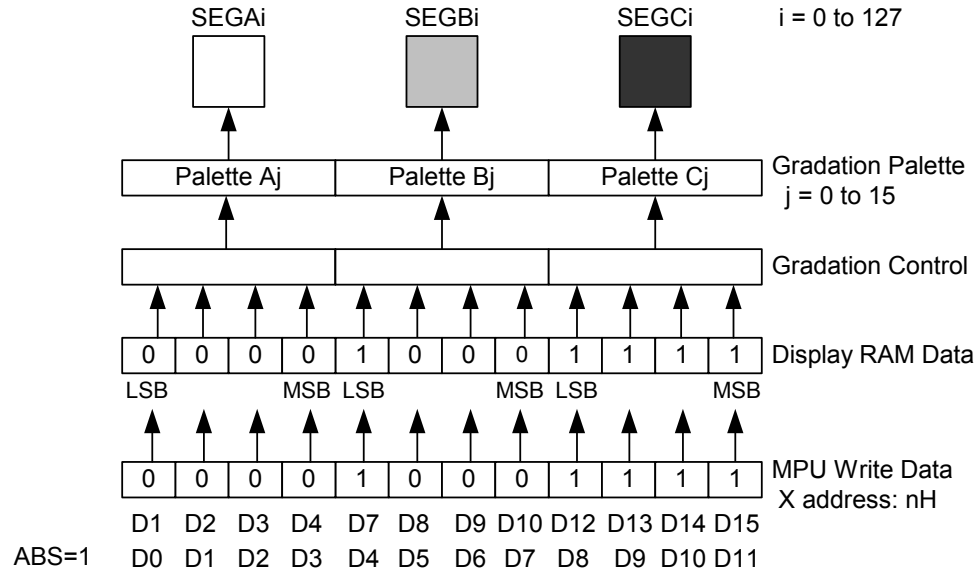
Note : Internal X address : 2nH ,2n+1H (REF="0")
: (FE-2n)H , [FF-(2n+1)] H (REF="1")

In HSW=1, Address=00H~BFH

- 16-bit mode

In 16-bits access, the weighting for each data bit is dependent on the status of the SWAP bit and the REF bit that is selected when data is written to the display RAM, as in the case with 8-bits access.

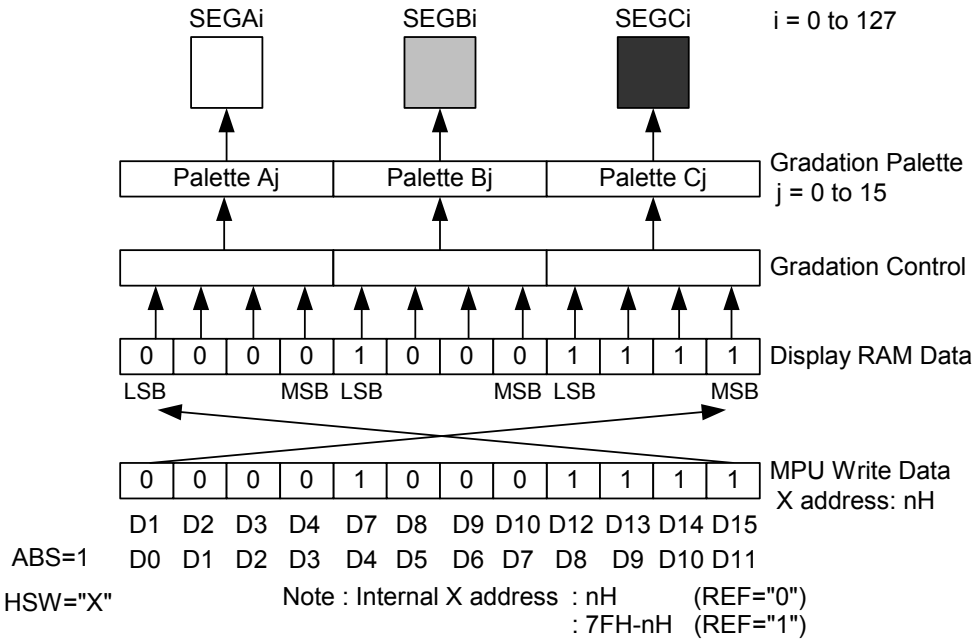
- (REF, SWAP)=(0, 0) or (1, 1)



HSW="X"

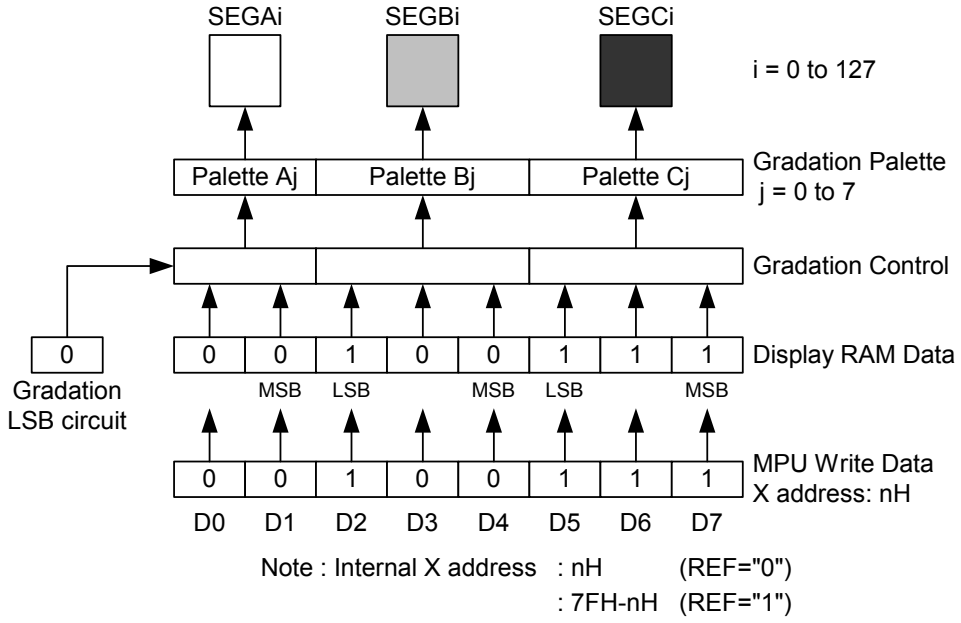
Note : Internal X address : nH (REF="0")
: 7FH-nH (REF="1")

- (REF, SWAP)=(0, 1) or (1, 0)

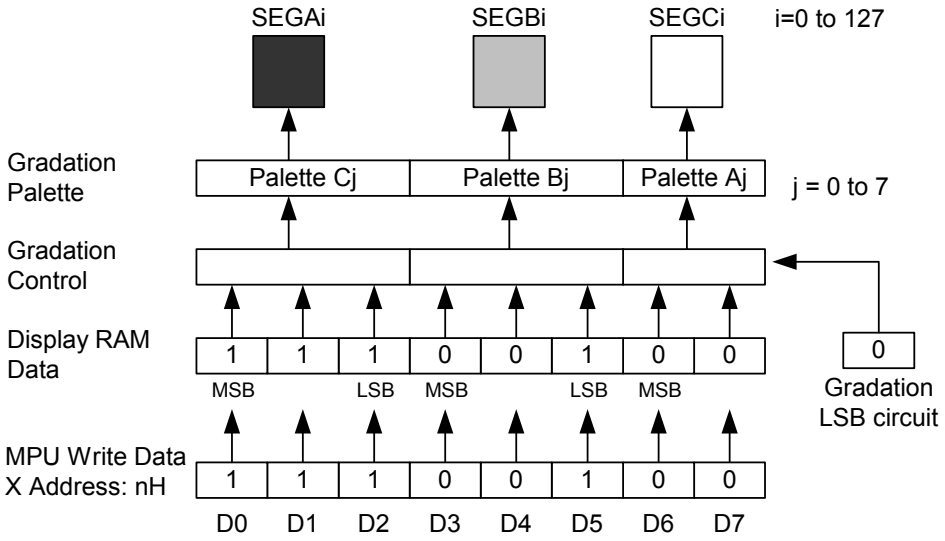


Gradation Mode (256 color)

- 8-bit mode
  - (REF, SWAP) = (0, 0) or (1, 1)



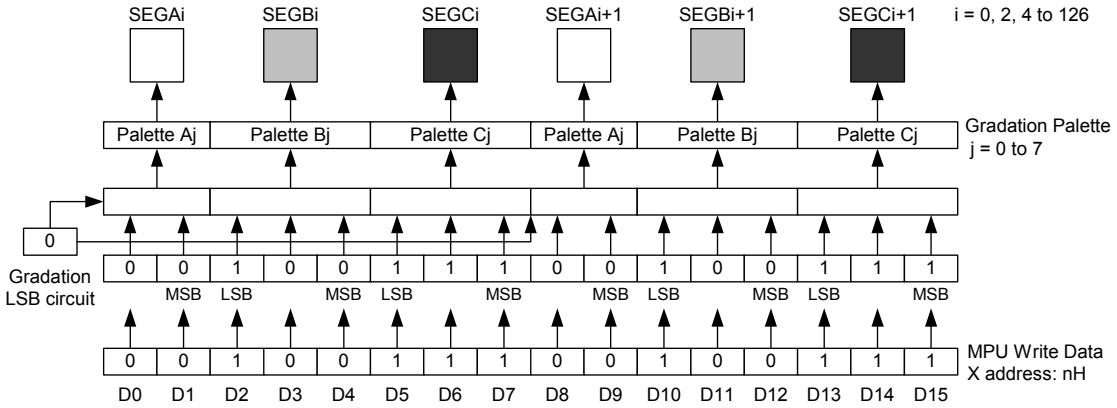
- (REF, SWAP) = (0, 1) or (1, 0)



Note : Internal X address : nH (REF="0")
: 7FH-nH (REF="1")

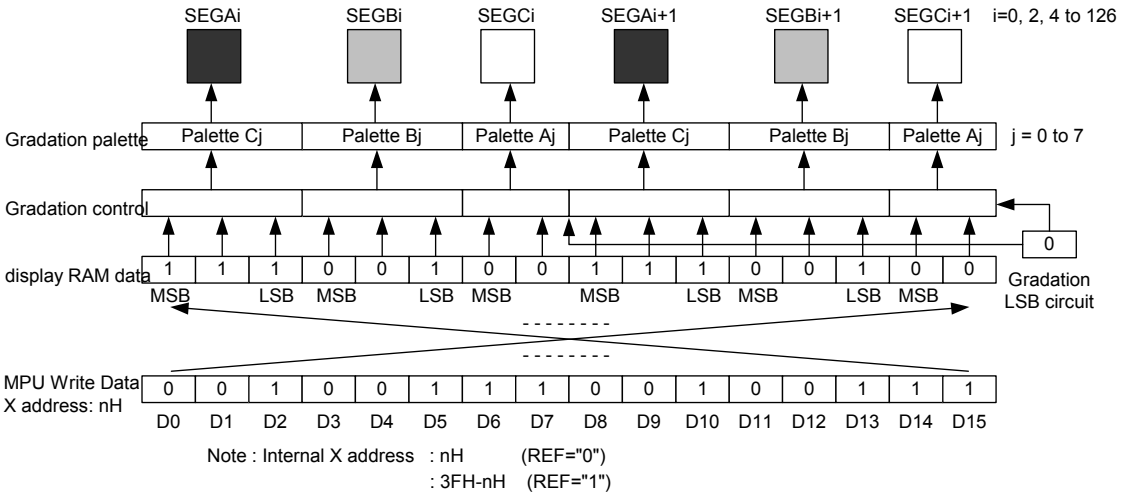
■ 16-bit mode (WLS=1)

- (REF, SWAP) = (0, 0) or (1, 1)



Note : Internal X address : nH (REF="0")
: 3FH-nH (REF="1")

- (REF, SWAP)=(0,1) or (1,0)



7.13 Gradation LSB Control

In 256 color mode (C256=1), the EM65571 provides segment driver output for 8-gradation display using 3 bits and for 4-gradation display using 2 bits.

The segment driver output for the 4-gradation display uses 2 bits written to the corresponding RAM area and 1 bit supplemented by the gradation LSB circuit, and then selects 4-gradation from 8-gradation.

In 256 color mode (C256=1), the segment driver output for the 4-gradation display results in a gradation level of 0 regardless of the gradation LSB when 2 bits of data on the display RAM are “00”. When 2-bits of data on the display RAM are “11”, a gradation level of 7/7 is selected regardless of the bit information of the gradation LSB. The other gradation levels are selected depending on the 2 bits of data on the display RAM and the gradation LSB bits.

One bit of data is supplemented by setting the gradation LSB register (GLSB).

The Gradation LSB control bit is applied to all 4-gradation segment drivers.

Gradation LSB = “0”: Select 0 as the LSB information on the RAM for 4-gradation segment drivers.

Gradation LSB = “1”: Select 1 as the LSB information on the RAM for 4-gradation segment drivers.

7.14 Gradation Palette

The EM65571 has two gradation display modes, the gradation fixed display mode and the gradation variable display mode. Select either of the two modes using the gradation display mode register.

PWM = "0": Select the variable display mode using 32 gradations selected from 48 gradations (65K=1, C256=0).

Select the variable display mode using 16 gradations selected from 48 gradations (65K=0, C256=0).

Select the variable display mode using 8 gradations selected from 48 gradations (65K=0, C256=1).

PWM = "1": Select the fixed display mode using specific 32 gradations (65K=1, C256=0)

Select the fixed display mode using specific 16 gradations (65K=0,C256=0)

Select the fixed display mode using specific 8 gradations (65K=0,C256=1)

To select the best gradation level suited for the LCD panel, use the gradation palette register among the 48-level gradation palettes in the gradation variable display mode. The segment driver output is set up by the selected 32-levels of gradation palettes.

The gradation palette register provides three registers for the SEGAi (0-127) group, SEGBi (0-127) group, and SEGCi (0-127) group of segment driver outputs [palettes Aj, Bj, and Cj (j = 0-31)]. Each register consists of a 6-bit register, selecting 32 gradations from the pattern for 48 gradations.

Initial values on the gradation palette register

65K Color Gradation Mode 65K=1, C256="*"

[Three groups of palettes Aj, Bj, and Cj (j = 0-31) are available]

(MSB) RAM Data (LSB)					Register Name	Initial Value
0	0	0	0	0	Palette0	000000
0	0	0	0	1	Palette1	000010
0	0	0	1	0	Palette2	000011
0	0	0	1	1	Palette3	000101
0	0	1	0	0	Palette4	000110
0	0	1	0	1	Palette5	001000
0	0	1	1	0	Palette6	001001
0	0	1	1	1	Palette7	001011
0	1	0	0	0	Palette8	001100
0	1	0	0	1	Palette9	001110
0	1	0	1	0	Palette10	001111
0	1	0	1	1	Palette11	010001
0	1	1	0	0	Palette12	010010
0	1	1	0	1	Palette13	010100
0	1	1	1	0	Palette14	010101
0	1	1	1	1	Palette15	010111
1	0	0	0	0	Palette16	011000
1	0	0	0	1	Palette17	011010
1	0	0	1	0	Palette18	011011
1	0	0	1	1	Palette19	011101
1	0	1	0	0	Palette20	011110
1	0	1	0	1	Palette21	100000
1	0	1	1	0	Palette22	100001
1	0	1	1	1	Palette23	100011
1	1	0	0	0	Palette24	100100
1	1	0	0	1	Palette25	100110
1	1	0	1	0	Palette26	100111
1	1	0	1	1	Palette27	101001
1	1	1	0	0	Palette28	101010
1	1	1	0	1	Palette29	101100
1	1	1	1	0	Palette30	101101
1	1	1	1	1	Palette31	101111

4096 Color Gradation Mode 65K=0, C256=0
[Three groups of palettes Aj, Bj, and Cj (j = 0-15) are available]

(MSB) RAM Data (LSB)				Register Name	Initial Value
0	0	0	0	Palette0	000000
0	0	0	1	Palette1	000011
0	0	1	0	Palette2	000110
0	0	1	1	Palette3	001001
0	1	0	0	Palette4	001100
0	1	0	1	Palette5	001111
0	1	1	0	Palette6	010010
0	1	1	1	Palette7	010101
1	0	0	0	Palette8	011000
1	0	0	1	Palette9	011011
1	0	1	0	Palette10	011110
1	0	1	1	Palette11	100001
1	1	0	0	Palette12	100100
1	1	0	1	Palette13	100111
1	1	1	0	Palette14	101010
1	1	1	1	Palette15	101110

256 Color Mode 65K=0, C256=1
[Three groups of palettes Aj, Bj, and Cj (j = 0-7) are available]

(MSB) RAM Data (LSB)			Register Name	Initial Value
0	0	0	Palette0	000000
0	0	1	Palette1	000100
0	1	0	Palette2	001011
0	1	1	Palette3	010011
1	0	0	Palette4	011010
1	0	1	Palette5	100001
1	1	0	Palette6	101000
1	1	1	Palette7	101111

Gradation level table (PWM = “0”, variable mode, 65K= “1”, C256=”*”)
[Three groups of palettes Aj, Bj, and Cj (j = 0-31) are available

Palette	Gradation Level	Remarks	Palette	Gradation Level	Remarks
0 0 0 0 0 0	0	gradation palette0 initial value	0 1 1 0 0 0	24/48	gradation palette16 initial value
0 0 0 0 0 1	1/48		0 1 1 0 0 1	25/48	
0 0 0 0 1 0	2/48	gradation palette1 initial value	0 1 1 0 1 0	26/48	gradation palette17 initial value
0 0 0 0 1 1	3/48	gradation palette2 initial value	0 1 1 0 1 1	27/48	gradation palette18 initial value
0 0 0 1 0 0	4/48		0 1 1 1 0 0	28/48	
0 0 0 1 0 1	5/48	gradation palette3 initial value	0 1 1 1 0 1	29/48	gradation palette19 initial value
0 0 0 1 1 0	6/48	gradation palette4 initial value	0 1 1 1 1 0	30/48	gradation palette20 initial value
0 0 0 1 1 1	7//48		0 1 1 1 1 1	31/48	
0 0 1 0 0 0	8/48	gradation palette5 initial value	1 0 0 0 0	32/48	gradation palette21 initial value
0 0 1 0 0 1	9/48	gradation palette6 initial value	1 0 0 0 0 1	33/48	gradation palette22 initial value
0 0 1 0 1 0	10/48		1 0 0 0 1 0	34/48	
0 0 1 0 1 1	11/48	gradation palette7 initial value	1 0 0 0 1 1	35/48	gradation palette23 initial value
0 0 1 1 0 0	12/48	gradation palette8 initial value	1 0 0 1 0 0	36/48	gradation palette24 initial value
0 0 1 1 0 1	13/48		1 0 0 1 0 1	37/48	
0 0 1 1 1 0	14/48	gradation palette9 initial value	1 0 0 1 1 0	38/48	gradation palette25 initial value
0 0 1 1 1 1	15/48	gradation palette10 initial value	1 0 0 1 1 1	39/48	gradation palette26 initial value
0 1 0 0 0 0	16/48		1 0 1 0 0 0	40/48	
0 1 0 0 0 1	17/48	gradation palette11 initial value	1 0 1 0 0 1	41/48	gradation palette27 initial value
0 1 0 0 1 0	18/48	gradation palette12 initial value	1 0 1 0 1 0	42/48	gradation palette28 initial value
0 1 0 0 1 1	19/48		1 0 1 0 1 1	43/48	
0 1 0 1 0 0	20/48	gradation palette13 initial value	1 0 1 1 0 0	44/48	gradation palette29 initial value
0 1 0 1 0 1	21/48	gradation palette14 initial value	1 0 1 1 0 1	45/48	gradation palette30 initial value
0 1 0 1 1 0	22/48		1 0 1 1 1 0	46/48	
0 1 0 1 1 1	23/48	gradation palette15 initial value	1 0 1 1 1 1	47/48	gradation palette31 initial value

Gradation level table (PWM = “0”, variable mode, 65K= “0”, C256=”0”)
[Three groups of palettes Aj, Bj, and Cj (j = 0-15) are available

Palette	Gradation level	Remarks	Palette	Gradation level	Remarks
0 0 0 0 0 0	0	gradation palette0 initial value	0 1 1 0 0 0	24/48	
0 0 0 0 0 1	1/48		0 1 1 0 0 1	25/48	gradation palette8 initial value
0 0 0 0 1 0	2/48		0 1 1 0 1 0	26/48	
0 0 0 0 1 1	3/48	gradation palette1 initial value	0 1 1 0 1 1	27/48	
0 0 0 1 0 0	4/48		0 1 1 1 0 0	28/48	gradation palette9 initial value
0 0 0 1 0 1	5/48		0 1 1 1 0 1	29/48	
0 0 0 1 1 0	6/48	gradation palette2 initial value	0 1 1 1 1 0	30/48	
0 0 0 1 1 1	7//48		0 1 1 1 1 1	31/48	gradation palette10 initial value
0 0 1 0 0 0	8/48		1 0 0 0 0	32/48	
0 0 1 0 0 1	9/48	gradation palette3 initial value	1 0 0 0 0 1	33/48	
0 0 1 0 1 0	10/48		1 0 0 0 1 0	34/48	gradation palette11 initial value
0 0 1 0 1 1	11/48		1 0 0 0 1 1	35/48	
0 0 1 1 0 0	12/48	gradation palette4 initial value	1 0 0 1 0 0	36/48	
0 0 1 1 0 1	13/48		1 0 0 1 0 1	37/48	gradation palette12 initial value
0 0 1 1 1 0	14/48		1 0 0 1 1 0	38/48	
0 0 1 1 1 1	15/48	gradation palette5 initial value	1 0 0 1 1 1	39/48	
0 1 0 0 0 0	16/48		1 0 1 0 0 0	40/48	gradation palette13 initial value
0 1 0 0 0 1	17/48		1 0 1 0 0 1	41/48	
0 1 0 0 1 0	18/48	gradation palette6 initial value	1 0 1 0 1 0	42/48	
0 1 0 0 1 1	19/48		1 0 1 0 1 1	43/48	gradation palette14 initial value

0 1 0 1 0 0	20/48		1 0 1 1 0 0	44/48	
0 1 0 1 0 1	21/48	gradation palette7 initial value	1 0 1 1 0 1	45/48	
0 1 0 1 1 0	22/48		1 0 1 1 1 0	46/48	gradation palette15 initial value
0 1 0 1 1 1	23/48		1 0 1 1 1 1	47/48	

Gradation level table (PWM = “0”, variable mode, 65K= “0”, C256=”1”)
[Three groups of palettes Aj, Bj, and Cj (j = 0-7) are available

Palette	Gradation level	Remarks	Palette	Gradation level	Remarks
0 0 0 0 0 0	0	gradation palette0 initial value	0 1 1 0 0 0	24/48	
0 0 0 0 0 1	1/48		0 1 1 0 0 1	25/48	
0 0 0 0 1 0	2/48		0 1 1 0 1 0	26/48	gradation palette4 initial value
0 0 0 0 1 1	3/48		0 1 1 0 1 1	27/48	
0 0 0 1 0 0	4/48	gradation palette1 initial value	0 1 1 1 0 0	28/48	
0 0 0 1 0 1	5/48		0 1 1 1 0 1	29/48	
0 0 0 1 1 0	6/48		0 1 1 1 1 0	30/48	
0 0 0 1 1 1	7//48		0 1 1 1 1 1	31/48	
0 0 1 0 0 0	8/48		1 0 0 0 0	32/48	
0 0 1 0 0 1	9/48		1 0 0 0 0 1	33/48	gradation palette5 initial value
0 0 1 0 1 0	10/48		1 0 0 0 1 0	34/48	
0 0 1 0 1 1	11/48	gradation palette2 initial value	1 0 0 0 1 1	35/48	
0 0 1 1 0 0	12/48		1 0 0 1 0 0	36/48	
0 0 1 1 0 1	13/48		1 0 0 1 0 1	37/48	
0 0 1 1 1 0	14/48		1 0 0 1 1 0	38/48	
0 0 1 1 1 1	15/48		1 0 0 1 1 1	39/48	
0 1 0 0 0 0	16/48		1 0 1 0 0 0	40/48	gradation palette6 initial value
0 1 0 0 0 1	17/48		1 0 1 0 0 1	41/48	
0 1 0 0 1 0	18/48		1 0 1 0 1 0	42/48	
0 1 0 0 1 1	19/48	gradation palette3 initial value	1 0 1 0 1 1	43/48	
0 1 0 1 0 0	20/48		1 0 1 1 0 0	44/48	
0 1 0 1 0 1	21/48		1 0 1 1 0 1	45/48	
0 1 0 1 1 0	22/48		1 0 1 1 1 0	46/48	
0 1 0 1 1 1	23/48		1 0 1 1 1 1	47/48	gradation palette7 initial value

7.15 Color Display (PWM+FRC)

Display color on the LCD, using gradation level to control th4e RGB color filter. The EM65571 uses 16 bits display data for 65K color. In 16 bits, D0-D4 means 32-gradation levels from 48 gradation levels R (or B), D5-D10 means 32-gradation levels from 48 gradation levels + FRC control bit G, D11-D15 means selecting 32-gradation levels B (or G) from 48 gradation levels.

Display RAM data RED, BLUE and Gradation level relationship

R, B Pixel Data	Output Level	R, B Pixel Data	Output Level
00000	GP0	10000	GP16
00001	GP1	10001	GP17
00010	GP2	10010	GP18
00011	GP3	10011	GP19
00100	GP4	10100	GP20
00101	GP5	10101	GP21
00110	GP6	10110	GP22
00111	GP7	10111	GP23
01000	GP8	11000	GP24
01001	GP9	11001	GP25
01010	GP10	11010	GP26
01011	GP11	11011	GP27
01100	GP12	11100	GP28
01101	GP13	11101	GP29
01110	GP14	11110	GP30
01111	GP15	11111	GP31

GP: Abbreviation of Gradation Palette

Display Ram Data Green and Gradation Level Relationship

When LSB=1, FRC enable, tThe FRC control bit is located at the G pixel data LSB

G Pixel Data	Output Level	G Pixel Data	Output Level
000000	GP0	100000	GP16
000001	(GP0+GP1)/2	100001	(GP16+GP17)/2
000010	GP1	100010	GP17
000011	(GP1+GP2)/2	100011	(GP17+GP18)
000100	GP2	100100	GP18
000101	(GP2+GP3)/2	100101	(GP18+GP19)
000110	GP3	100110	GP19
000111	(GP3+GP4)/2	100111	(GP19+GP20)
001000	GP4	101000	GP20
001001	(GP4+GP5)/2	101001	(GP20+21)
001010	GP5	101010	GP21
001011	(GP5+GP6)/2	101011	(GP21+GP22)
001100	GP6	101100	GP22
001101	(GP6+GP7)/2	101101	(GP22+GP23)
001110	GP7	101110	GP23
001111	(GP7+GP8)/2	101111	(GP23+GP24)
010000	GP8	110000	GP24
010001	(GP8+GP9)/2	110001	(GP24+GP25)
010010	GP9	110010	GP25
010011	(GP9+GP10)/2	110011	(GP25+GP26)
010100	GP10	110100	GP26
010101	(GP10+GP11)/2	110101	(GP26+GP27)
010110	GP11	110110	GP27
010111	(GP11+GP12)/2	110111	(GP27+GP28)
011000	GP12	111000	GP28
011001	(GP12+GP13)/2	111001	(GP28+GP29)
011010	GP13	111010	GP29
011011	(GP13+GP14)/2	111011	(GP29+GP30)
011100	GP14	111100	GP30
011101	(GP14+GP15)/2	111101	(GP30+GP31)
011110	GP15	111110	GP31
011111	(GP15+GP16)/2	111111	GP31

GP: Abbreviation of Gradation Palette

7.16 Display Timing Circuit

The display timing circuit generates internal signals and timing pulses (internal LP, FLM, M) by clock. It can select external input (CK) or internal oscillation.

Symbol	Description
LP (internal)	LP or latched clock signal. At the rising edge, count the display line counter. At the falling edge, output the LCD drive signal.
FLM (internal)	FLM or First Line Maker, signal for LCD display synchronous signals. When FLM is set to "H", the display start-line address is present.
M (internal)	Signal for LCD drive output alternated signals.

7.17 Signal Generation to Display Line Counter and Display Data Latching Circuit

Both the clock for the line counter and the clock to display the data latching circuit from the display clock (internal LP) are generated. Synchronized with the display clock (internal LP), the line addresses of the Display RAM are generated and 384-bit display data are latched to display the data latching circuit and output to the LCD drive circuit (segment output). Read-out of the display data to the LCD drive circuit is completely independent of the MPU.

7.18 Generation of the Alternated Signal (internal M) and the Synchronous Signal (internal FLM)

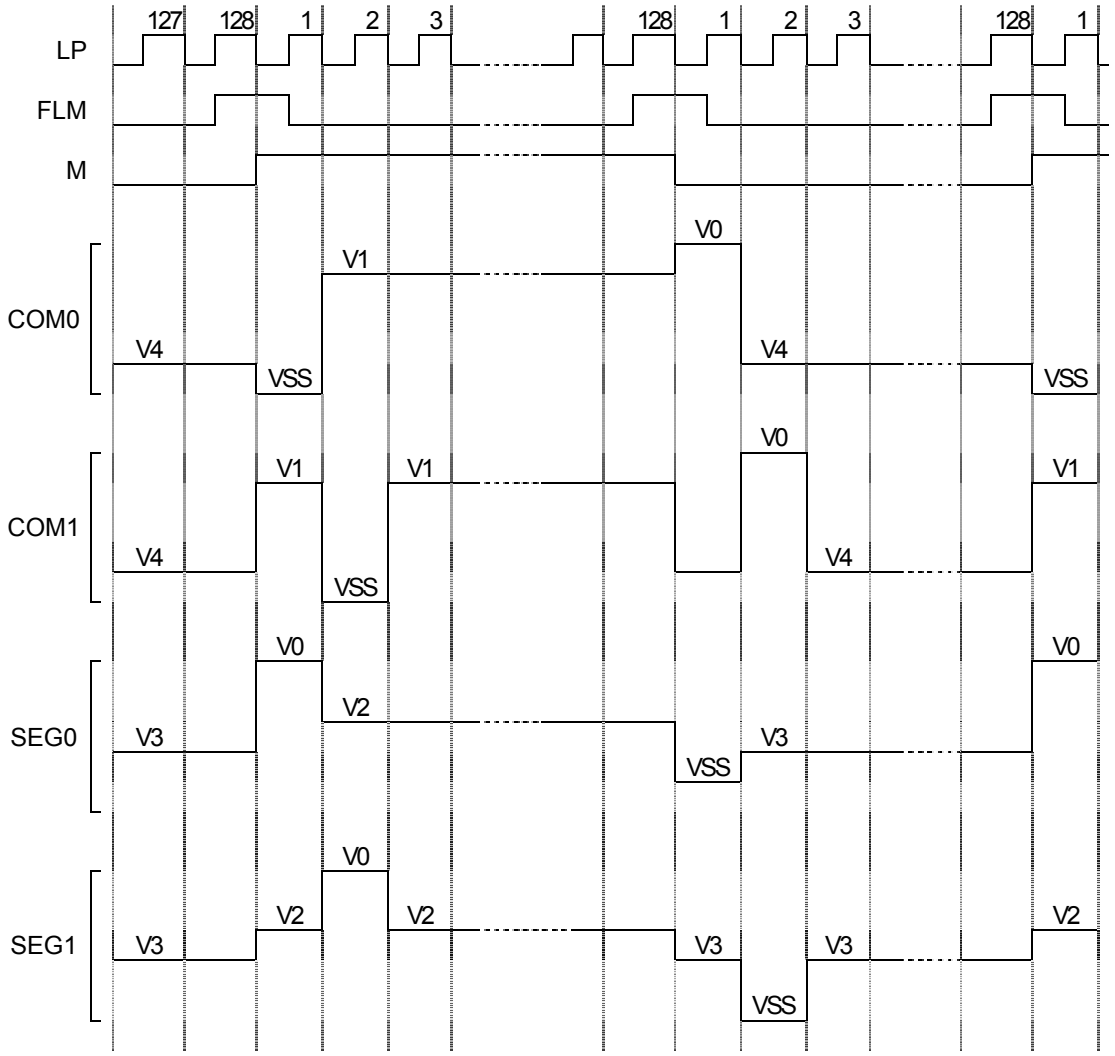
The LCD alternated signal (internal M) and synchronous signal (internal FLM) are generated by the display clock (internal LP). The FLM generates an alternated drive waveform to the LCD drive circuit. Normally, the FLM generates alternated drive waveform every frame (M-signal level is reversed every one frame). However, by setting up data (n-1) in an n-line reverse register and n-line alternated control bit (NLIN) at "1", an n-line reverse waveform is generated.

7.19 Display Data Latching Circuit

The display data latching circuit temporally latches the display data that is output to the LCD driver circuit from the display RAM, once every one common period. Normal display/reverse display, display ON/OFF, and display all on functions are operated by controlling the data in the display data latch, therefore, no data within the display RAM changes.

7.20 Output Timing of the LCD Driver

Display Timing at Normal mode (not reverse mode), 1/128 DUTY.



7.21 LCD Driver Circuit

This driver circuit generates four levels of LCD driver voltage. The circuit has 384-segment output and 130-common output and outputs a combined display data and internal signal M. Two of the common outputs, COMA and COMB, are special outputs. The COMA and COMB outputs are not influenced by partial setting, they are mainly used for display. The common driver circuit that has shift register sequentially outputs common scan signals.

7.22 Oscillator Circuit

The EM65571 has a CR oscillator. The output from this oscillator is used as the timing signal source of the display and the boosting clock for the booster.

When external clock is used, feed the clock to CK pin.

The duty cycle of the external clock must be 50%.

The resistance ratio of the CR oscillator is programmable. If you change this ratio, also change the frame frequency for display.

7.23 Power Supply Circuit

This circuit supplies voltages necessary to drive an LCD. The circuit consists of a booster and a voltage converter.

Boosted voltage from the booster is fed to the voltage converter that converts this input voltage into V0, V1, V2, V3 and V4 that are used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many pixels. Otherwise, the display quality will degrade considerably. Instead, use an external power supply. When using an external power supply, turn off the internal power supply (AMPON, DCON="00"), disconnect pins CAP1-, CAP1+, CAP2+, CAP2-, CAP3+, CAP4+, CAP5+, CAP6+, VOUT and VEE. Then, feed the external LCD drive voltages to pins V0, V1, V2, V3 and V4. The power circuit can be controlled by a power circuit related register. So, partial function of the built-in power circuit can be used with external power supply.

DCON	AMPON	Booster Circuit	Voltage Conversion Circuit	External Voltage Input
0	0	Disable	Disable	V0, V1, V2, V3 and V4 are supplied [1]
0	1	Disable	Enable	VOUT is supplied [2]
1	1	Enable	Enable	-

Note:

[1] When the booster and voltage converter are not operating, disconnect pins CAP+, CAP-, CAP2+, CAP2-, CAP3+, CAP4+, CAP5+, CAP6+, VOUT and VEE.
Apply external LCD driver voltages to the corresponding pins.

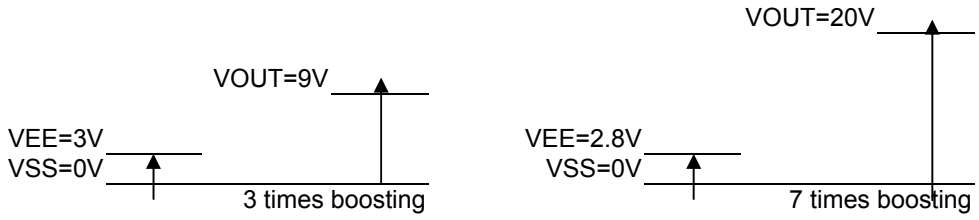
[2] Since the booster is not operating, disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP4+, CAP5+, CAP6+ and VEE.
Derive the voltage source to be supplied to the voltage converter from the VOUT pin.

7.24 Booster Circuit

Placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-, across CAP4+ and CAP2-, across CAP5+ and CAP1-, across CAP6+ and CAP2-, and across VOUT and VSS will boost the voltage coming from VEE and VSS nth times and outputs the boosted voltage to the VOUT pin. The boosted voltage, either twice, three times, four times or five times the supply voltage and which is output to the VOUT pin is determined by the boost step register, and set by a command instruction.

- ✧ In case the required voltage is twice the voltage supply, this is achieve by placing capacitor C1 only across CAP1+ and CAP1-, and opening CAP2+, CAP2-, CAP3+, CAP1-, CAP4+, CAP2-, CAP5+, CAP1-, CAP6+ and CAP2-.
- ✧ In case the required voltage is three times the voltage supply, this is achieve by placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, and opening CAP3+, CAP1-, CAP4+, CAP2-, CAP5+, CAP1-, CAP6+ and CAP2-.
- ✧ In case the required voltage is four times the voltage supply, this is achieve by placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-, and opening CAP4+, CAP2-, CAP5+, CAP1-, CAP6+ and CAP2-.
- ✧ In case the required voltage is five times the voltage supply, this is achieve by placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-, across CAP4+ and CAP2-, and opening CAP5+, CAP1-, CAP6+ and CAP2-.
- ✧ In case the required voltage is six times the voltage supply, this is achieve by placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-, across CAP4+ and CAP2-, across CAP5+ and CAP1-, and opening CAP6+ and CAP2-.
- ✧ In case the required voltage is seven times the voltage supply, this is achieve by placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-, across CAP4+ and CAP2-, across CAP5+ and CAP1-, across CAP6+ and CAP2-.

When using a built-in booster circuit, the output voltage (VOUT) must be less than the recommended operating voltage (20V). If the output voltage (VOUT) is over the recommended operating voltage, the proper and full functionality of the chip cannot be guaranteed.



When using 7x boosting ratio, the VEE operating voltage should not exceed 2.8V. For a guaranteed result, the VOUT should be less than the recommended operating voltage of 20V.

7.25 Electronic Volume

The voltage conversion circuit has a built-in electronic volume, which allows the VBA to be controlled with DV register setting. The DV registers are 7 bits, so it's advisable to select 113 voltage values for the VBA voltage. The relationship between VBA and DV is shown in the following equation:

$$VBA = \left[1 + \frac{M + Offset}{381}\right] \times VREF$$

where M: DV register value (8~20)

Offset: CV1~CV4 setting

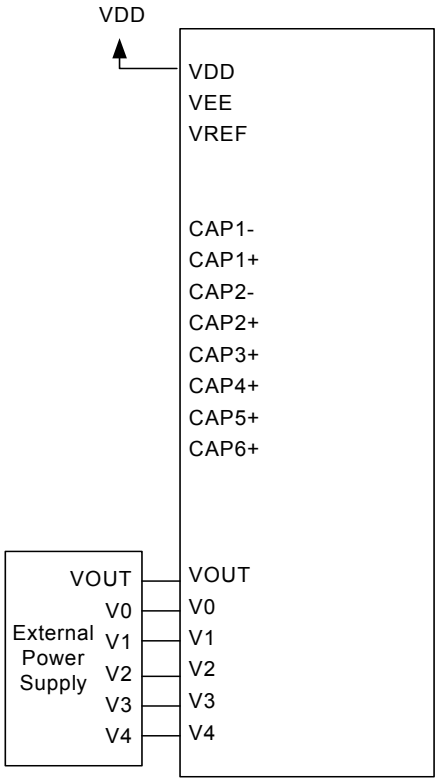
VREF: Internal temperature compensation output voltage

7.26 Voltage Regulator

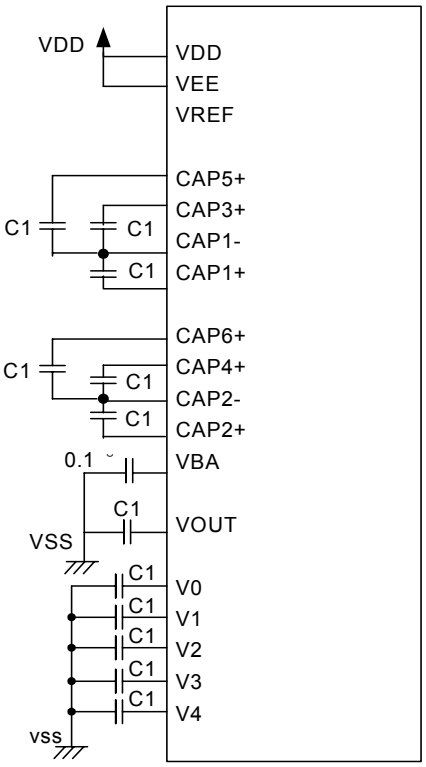
The EM65571 has a built-in reference voltage regulator, which generates the voltage amplified by the input voltage from the internal temperature compensation output voltage VREF pin. The generated voltage is output at the V0 pin. Even if the boosted voltage level fluctuates, V0 remains stable as long as VOUT is higher than V0. Stable power supply can be obtained using this constant voltage, even if the load fluctuates. The EM65571 uses the generated V0 level for the reference level of the electronic volume to generate an LCD driver voltage.

7.27 Voltage Generator Circuit

The voltage converter contains the voltage generator circuit. The LCD driver voltages other than V0, which is, V1, V2, V3 and V4 are obtained by dividing V0 through a resistor network. The LCD driver voltage from EM65571 is biased at 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11, 1/12 or 1/13. When using the internal power supply, connect a stabilizing capacitor C2 to each of the pins V0 to V4. The capacitance of C2 should be determined while observing the LCD panel to be used. When using an external power supply, apply external LCD driver voltages to V0, V1, V2, V3, V4, and disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP4+, CAP5+, CAP6+, VOUT, VEE. When using only the voltage conversion circuit, turn off the internal booster circuit, disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP4+, CAP5+, CAP6+ and VEE. Derive the voltage source to be supplied to the voltage converter from the VOUT pin.



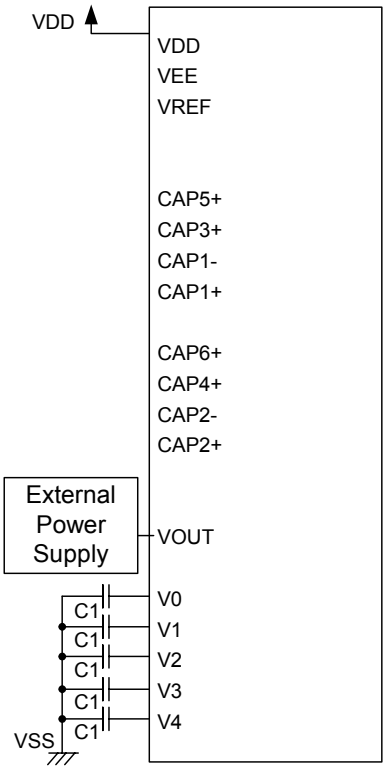
When using external power supply.



When using internal power circuit.
(7 times boosting)

Recommended value: C1 = 1 µF

Note: External Capacitance must use B characteristic.



When using an internal power circuit and internal reference voltage.

(VOUT supplied externally, and not using booster circuit)

Recommended value: C1 = 1µF

Note: External Capacitance must use B characteristic.

7.28 EEPROM Function

For the EM65571 to support EEPROM function to tune to the LCD operating voltage Vop, first, select EEPROM operating mode, EEPROM power from internal or external, and initial oscillator frequency or faster oscillator frequency (+50%). Select the register (Bank5 [AH]), using (M1, M0) to select the operating mode for the EEPROM, (M1, M0) = 00 → Read information from the EEPROM; (M1, M0) = 01 → Program information to the EEPROM; (M1, M0) = 10 → Erase information on the EEPROM; (M1, M0) = 11 → Reserved.

(M1, M0)	EEPROM Operating Mode
00	Read
01	Program
10	Erase
11	Reserve

Secondly, the power supply for the EEPROM is selective. By setting the VPP_EXT control bit of the register, you can select internal power (from V0) or external power to support the EEPROM. VPP_EXT=0 → internal power; VPP_EXT=1 → force 16~18V from the VPP pin externally.

Thirdly, you can select the oscillator frequency by setting the OSC control bit of register. OSC=0 → initial oscillator frequency setting; OSC=1 → oscillator frequency + 50%.

You can get Vop calibration offset voltage by setting the Vop calibration offset register.

CV4-CV1	Calibration Offset
0111	+7
0110	+6
…	…
0000	0
1000	-8
1001	-7
…	…
1111	-1

$$VBA = \left[1 + \frac{M + Offset}{381}\right] \times VREF$$

where M: DV register value

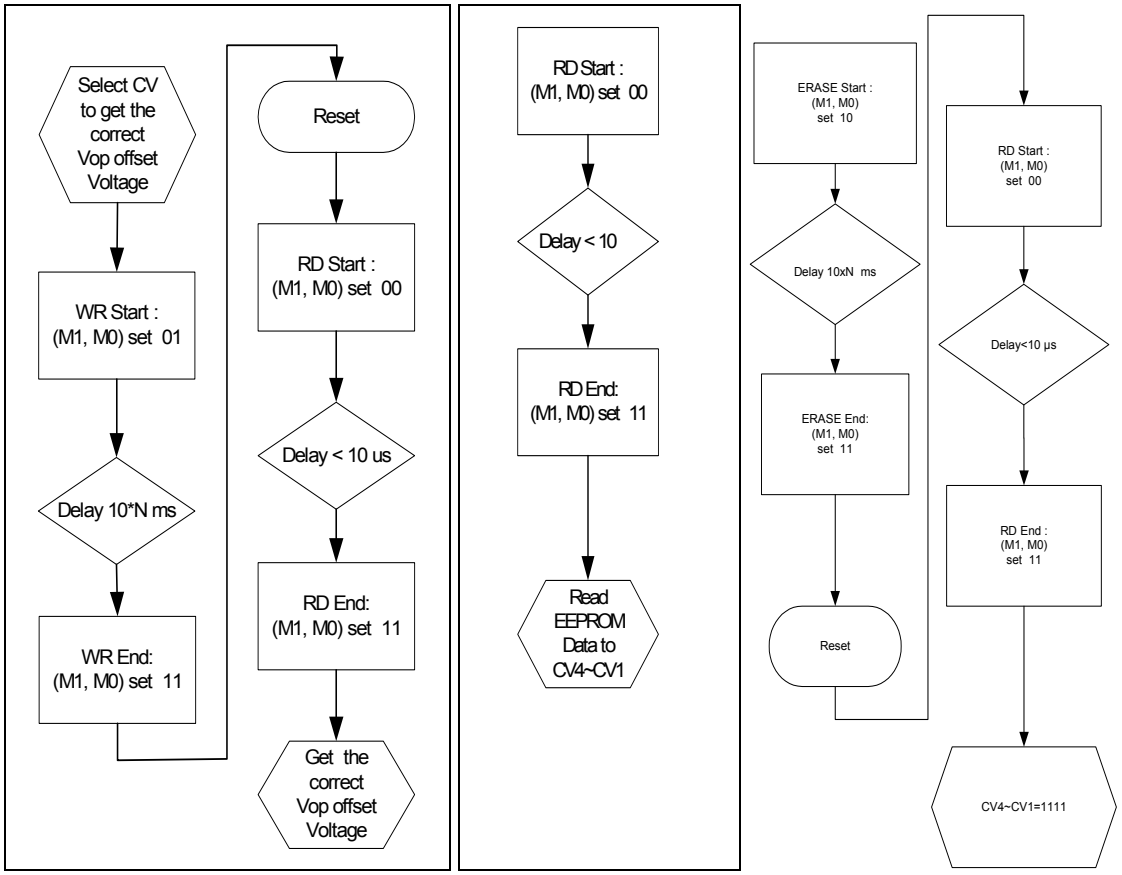
Offset: CV1~CV4 setting

VREF: internal temperature compensation output voltage

$$V0 = VBA \times N$$

where N : RM register setting

The flow charts for the program, read, and erase EEPROM to get correct Vop offset voltage are shown as follows:



Program **Read** **Erase**

■ Program

For example, the desired Vop calibration offset is +7, CV4~CV1 is set to 0111, the example code is shown below:

```
WRITE  #F5H    // set RE FLAG 101 → INSTRUCTION Bank 5

WRITE  #B7H    // set CV4~CV1=0111

WRITE  #A4H    // set EEPROM operating mode → programming ; EEPROM power is from
                  the internal V0 ; oscillator frequency is the initially set value

DELAY  10*N MS  // wait for 10*N ms to finish programming

WRITE  #ACH    // set EEPROM mode → reserve (finish programming)

WRITE  #F0H    // set RE FLAG 000 → INSTRUCTION Bank 0

WRITE  #B1H    // EM65571 reset

WRITE  #F5H    // set RE FLAG 101 → INSTRUCTION Bank 5
```

WRITE #A0H // set EEPROM operating mode → reading ; read data from EEPROM to CV4~CV1 register

DELAY <10 μS // wait <10 μS to finish reading

WRITE #ACH // set EEPROM mode → reserve (finish reading data from EEPROM to CV4~CV1 register)

■ Read

WRITE #F5H // set RE FLAG 101 → INSTRUCTION Bank 5

WRITE #D1H // EXTENSION COMMAND

WRITE #A0H // set EEPROM operating mode → reading

DELAY >10 μS // wait <10 μs to finish reading

WRITE #ACH // set EEPROM mode → reserve (finish reading)

WRITE #D0H // EXTENSION COMMAND

WRITE #A0H // set EEPROM operating mode → reading ; read data from EEPROM to CV4~CV1 register.

DELAY >10 μS // wait <10 μs to finish reading

WRITE #ACH // set EEPROM mode → reserve (finish reading)

■ Erase

WRITE #F5H // set RE FLAG 101 → INSTRUCTION Bank 5

WRITE #A8H // set EEPROM operating mode → erasing ; erase EEPROM data to 1

DELAY 10*N MS // wait 10*N ms to finish erasing

WRITE #ACH // set EEPROM mode → reserve (finish erasing)

WRITE #F0H // set RE FLAG 000 → INSTRUCTION Bank 0

WRITE #B1H // EM65571 reset

WRITE #F5H // set RE FLAG 101 → INSTRUCTION Bank 5

WRITE #A0H // set EEPROM operating mode → reading ; read data from EEPROM to CV4~CV1 register

DELAY <10 μS // wait <10 μS to finish reading

WRITE #ACH // set EEPROM mode → reserve (finish reading data from EEPROM to CV4~CV1 register)

(CV4~CV1 should be equal to 1111 after erasing)

7.29 Partial Display Function

The EM65571 has a partial display function, which can display a part of the graphic display area. This function is used to set the lower bias ratio, lower boost step, and lower LCD drive voltage. In setting the partial display function, the EM65571 provides low power consumption, hence, it is most suitable for clock indication or calendar indication of portable devices.

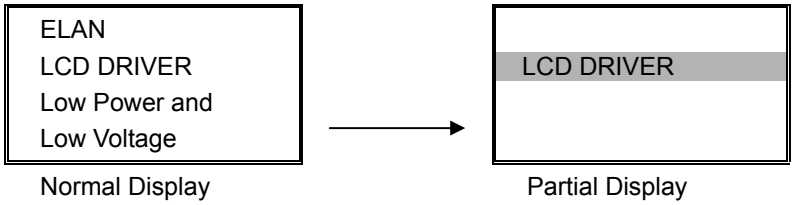
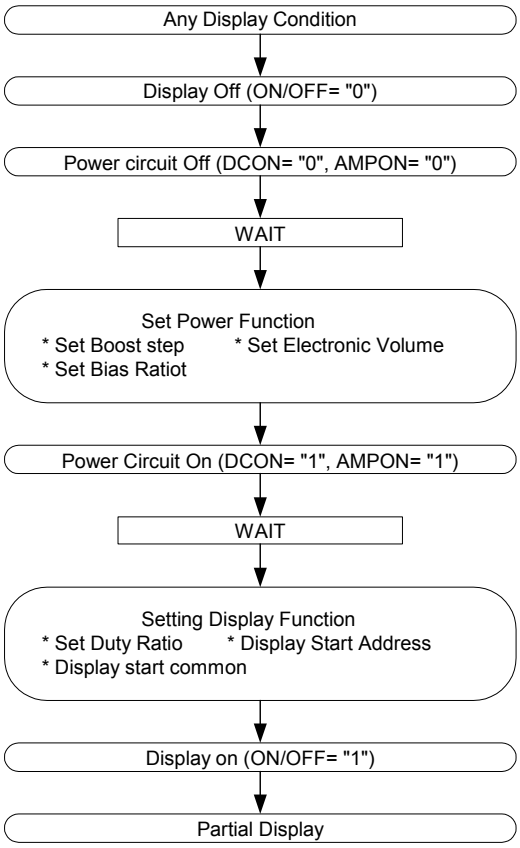


Figure 12. Partial Display Image

When using the partial display function, it is necessary to keep the following sequence.



Select a display duty ratio for the partial display from 1/10 to 1/128 using the DS (LCD duty ratio) register.

Set the most suitable values for LCD drive bias ratio, LCD drive voltage, electronic volume, the number of boosting steps, and other details according to the actual LCD panel used and the selected duty ratio.

7.30 Discharge Circuit

The EM65571 has a built-in discharge circuit, which discharges electricity from capacitors for stability of power sources (V0~V4).

The discharge circuit is valid, while the DIS register is set to “1”. When the built-in power supply is used, it should be set DIS=”1” after the power source is turned off (DCON, AMPON) = (0, 0). Both the built-in power source and the external power source (V0~V4, VOUT) should not be turned off while DIS= ”1”.

7.31 Initialization

Setting RESB pin to “L” initializes the EM65571. Normally, the RESB pin is initialized together with the MPU by connecting to the reset pin of the MPU. When power is ON, be sure to make RESB=”L”.

ITEM	Initial Value
Display RAM	Not fixed
X Address	00H set
Y Address	00H set
Display starting line	Set at the first line (0H)
Display ON/OFF	Display OFF
Display Normal/Reverse	Normal
Display duty	1/10
n-line alternate	Every frame unit
(BF1, BF0)	(0, 0)
Common shift direction	COM0 COM127, COMA, COMB
Increment mode	Increment OFF
REF mode	Normal
Data SWAP Mode	OFF
Register in electronic volume	(0, 0, 0, 0, 0, 0, 0)
Power Supply	OFF
Display mode	Gradation display mode
Bias ratio	1/13 bias
Gradation Palette 0	(0, 0, 0, 0, 0, 0)
Gradation Palette 1	(0, 0, 0, 0, 1, 0)
Gradation Palette 2	(0, 0, 0, 0, 1, 1)
Gradation Palette 3	(0, 0, 0, 1, 0, 1)
Gradation Palette 4	(0, 0, 0, 1, 1, 0)
Gradation Palette 5	(0, 0, 1, 0, 0, 0)
Gradation Palette 6	(0, 0, 1, 0, 0, 1)
Gradation Palette 7	(0, 0, 1, 0, 1, 1)
Gradation Palette 8	(0, 0, 1, 1, 0, 0)

ITEM	Initial Value
Gradation Palette 9	(0, 0, 1, 1, 1, 0)
Gradation Palette 10	(0, 0, 1, 1, 1, 1)
Gradation Palette 11	(0, 1, 0, 0, 0, 1)
Gradation Palette 12	(0, 1, 0, 0, 1, 0)
Gradation Palette 13	(0, 1, 0, 1, 0, 0)
Gradation Palette 14	(0, 1, 0, 1, 0, 1)
Gradation Palette 15	(0, 1, 0, 1, 1, 1)
Gradation Palette 16	(0, 1, 1, 0, 0, 0)
Gradation Palette 17	(0, 1, 1, 0, 0, 1)
Gradation Palette 18	(0, 1, 1, 0, 1, 1)
Gradation Palette 19	(0, 1, 1, 1, 0, 1)
Gradation Palette 20	(0, 1, 1, 1, 1, 0)
Gradation Palette 21	(1, 0, 0, 0, 0, 0)
Gradation Palette 22	(1, 0, 0, 0, 0, 1)
Gradation Palette 23	(1, 0, 0, 0, 1, 1)
Gradation Palette 24	(1, 0, 0, 1, 0, 0)
Gradation Palette 25	(1, 0, 0, 1, 1, 0)
Gradation Palette 26	(1, 0, 0, 1, 1, 1)
Gradation Palette 27	(1, 0, 1, 0, 0, 1)
Gradation Palette 28	(1, 0, 1, 0, 1, 0)
Gradation Palette 29	(1, 0, 1, 1, 0, 0)
Gradation Palette 30	(1, 0, 1, 1, 0, 1)
Gradation Palette 31	(1, 0, 1, 1, 1, 1)
Gradation display mode	Variable mode
Gradation LSB	0
RAM access data length	8-bit mode
Discharge Register	0

7.32 Precautionary Measures during Power ON and Power OFF

High current that may flow if a voltage is supplied to the LCD driver power supply while the system power supply is floating may permanently damage this LSI. The details are as follows.

7.32.1 When Using an External Power Supply

- ✧ Procedure for Power ON
  - o Logic system (VDD) power ON, make reset operation.
  - o Supply external LCD driver voltage to corresponding pins (V0, V1, V2, V3 and V4)
- ✧ Procedure for Power OFF
  - o Set HALT register to "1" or initiate a reset operation.
  - o Cut off external LCD driver voltage.
  - o Logic system (VDD) power OFF.

Note: Connect a serial resistor (50 to 100Ω) or fuse to the LCD driver power V0 or VOUT (when using only an internal voltage conversion circuit) of the system as a current limiter. Moreover, set up suitable resistor values corresponding to the LCD display grade.

7.32.2 When Using a Built-in Power Supply

- ✧ Procedure for Power ON
  - o Logic system (VDD) power ON
  - o Booster circuit system (VEE) power ON
  - o Initiate a reset operation, enable booster and voltage conversion circuit.

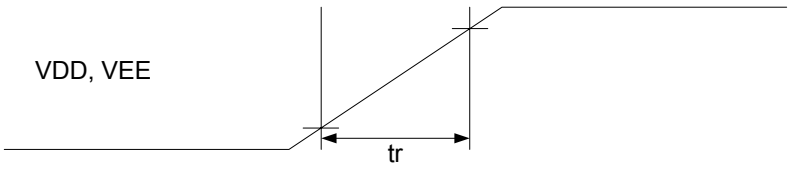
If the VDD and VEE voltages are not of the same potential, turn on the power logic system (VDD) first.

- ✧ Procedure for Power OFF
  - o Set the HALT register to "1" or reset the system.
  - o Booster circuit system (VEE) power OFF.
  - o Logic system (VDD) power OFF.

If VDD and VEE are not of the same potential, turn off the VEE first. After VEE, VOUT, V0, V1, V2, V3 and V4 voltages are below LCD ON voltage (threshold voltage for Liquid crystal turn on), power off the logic system (VDD).

7.32.3 Power Supply Rising Time

Though especially there is no constraint on the rising time of the power supply, the "tr" (rising time) of the following is recommended in the practical use.

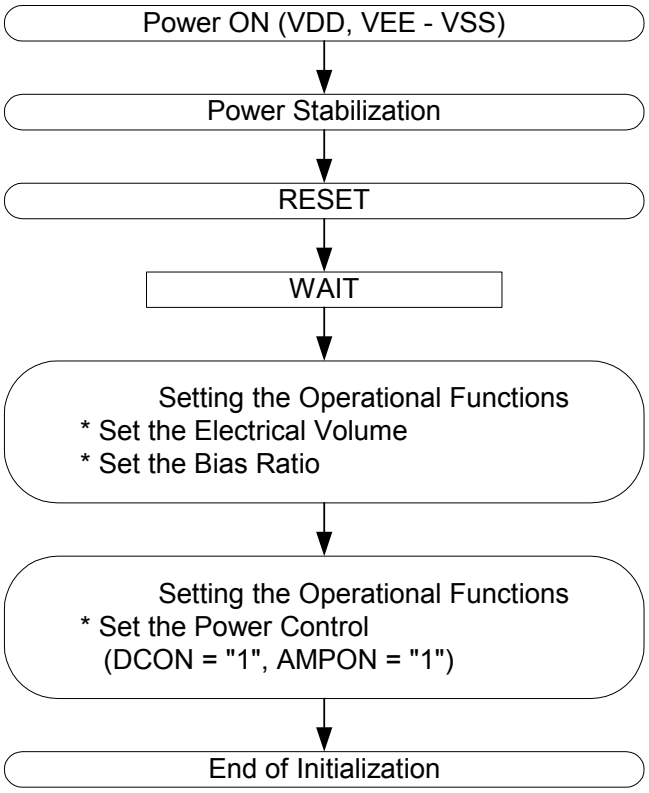


Item	Recommended Rising Time	Applicable Power
tr	30µs ~ 10ms	VDD, VEE

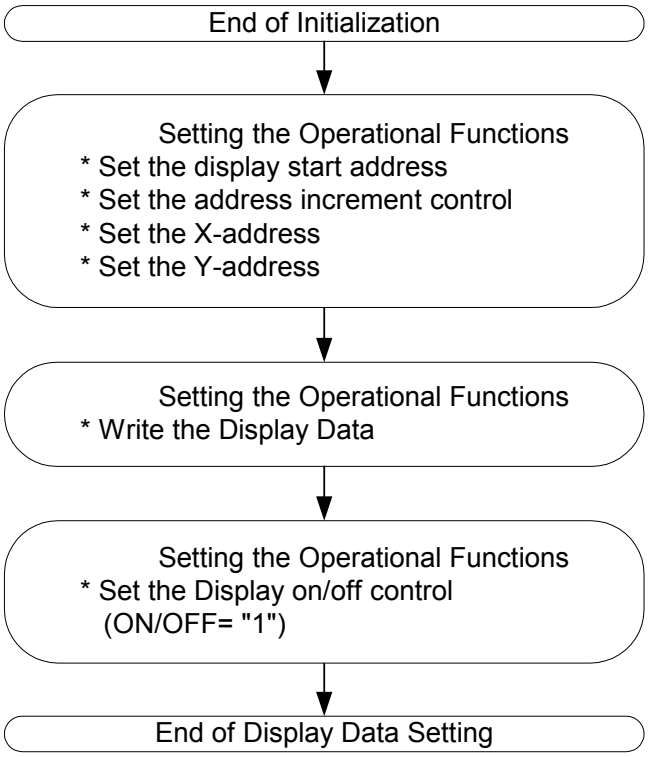
Note: The rising time is the time from 10% of VDD/VEE to 90%.

7.33 Example of Register Setting

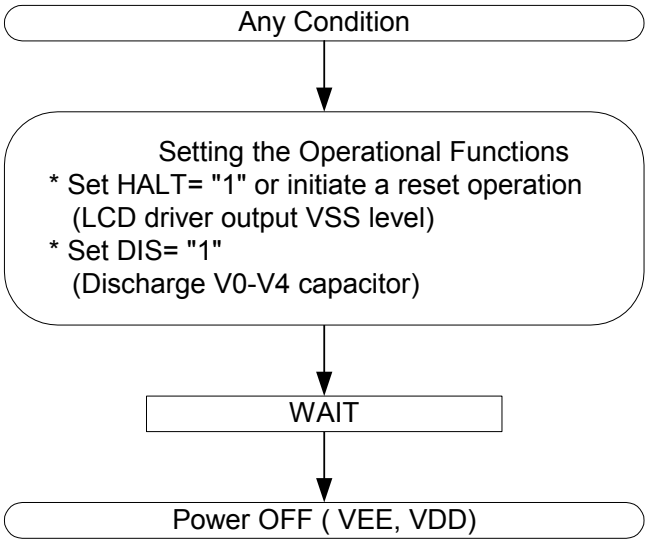
7.33.1 Initialization



7.33.2 Display Data



7.33.3 Power OFF



8 Control Register

8.1 Control Register

Control Register Table (Bank 0)

Control Register	Pins (for 80-family) & Bank							Address & Code								
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	Function
X Address (Lower nibble) [0H]	0	1	0	1	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
X Address (Upper nibble) [1H]	0	1	0	1	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Set of X direction Address in display RAM
Y Address (Lower nibble) [2H]	0	1	0	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Set of Y direction Address in display RAM
Y Address (Upper nibble) [3H]	0	1	0	1	0	0	0	0	0	1	1	AY7	AY6	AY5	AY4	Set of Y direction Address in display RAM
Display start address (Lower nibble) [4H]	0	1	0	1	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Set address of display RAM making common starting line display
Display start address (Upper nibble) [5H]	0	1	0	1	0	0	0	0	1	0	1	LA7	LA6	LA5	LA4	Set address of display RAM making common starting line display
n-line altemation (Lower nibble) [6H]	0	1	0	1	0	0	0	0	1	1	0	N3	N2	N1	N0	Set the number of altemated reverse line
n-line altemation (Upper nibble) [7H]	0	1	0	1	0	0	0	0	1	1	1	N7	N6	N5	N4	Set the number of altemated reverse line
Display control (1) [8H]	0	1	0	1	0	0	0	1	0	0	0	SHIFT	65K	ALLON	ON/OFF	SHIFT: Select common shift direction 65K: Select 65K gradation ALLON: All display ON ON/OFF: Display ON/OFF control
Display control (2) [9H]	0	1	0	1	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Display normal/reverse NLIN: n line reverse control SWAP: Display data swapping REF: Segment normal/reverse
Increment control [AH]	0	1	0	1	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Select window. AIM: Select increment mode AYI: Y increment, AXI: X increment
Power control [BH]	0	1	0	1	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: Internal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting
LCD Duty Ratio [CH]	0	1	0	1	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Set LCD drive duty ratio
Booster [DH]	0	1	0	1	0	0	0	1	1	0	1	SHP	VU2	VU1	VU0	Set number of boosting step for booster circuit
Bias ratio control [EH]	0	1	0	1	0	0	0	1	1	1	0	B3	B2	B1	B0	Set bias ratio for LCD driving voltage
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The asterisk "*" mark means "don't care"
Parentheses [ ] shows the control register address.

Control Register Table (Bank 1)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation Palette A0,A8,A16,A24 (Lower nibble) [0H]	0	1	0	1	0	0	1	0	0	0	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A0,A8,A16,A24
Gradation Palette A0,A8,A16,A24 (Upper nibble) [1H]	0	1	0	1	0	0	1	0	0	0	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A0,A8,A16,A24
Gradation Palette A1,A9,A17,A25 (Lower nibble) [2H]	0	1	0	1	0	0	1	0	0	1	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A1,A9,A17,A25
Gradation Palette A1,A9,A17,A25 (Upper nibble) [3H]	0	1	0	1	0	0	1	0	0	1	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A1,A9,A17,A25
Gradation Palette A2,A10,A18,A26 (Lower nibble) [4H]	0	1	0	1	0	0	1	0	1	0	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A2,A10,A18,A26
Gradation Palette A2,A10,A18,A26 (Upper nibble) [5H]	0	1	0	1	0	0	1	0	1	0	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A2,A10,A18,A26
Gradation Palette A3,A11,A19,A27 (Lower nibble) [6H]	0	1	0	1	0	0	1	0	1	1	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A3,A11,A19,A27
Gradation Palette A3,A11,A19,A27 (Upper nibble) [7H]	0	1	0	1	0	0	1	0	1	1	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A3,A11,A19,A27
Gradation Palette A4,A12,A20,A28 (Lower nibble) [8H]	0	1	0	1	0	0	1	1	0	0	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A4,A12,A20,A28
Gradation Palette A4,A12,A20,A28 (Upper nibble) [9H]	0	1	0	1	0	0	1	1	0	0	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A4,A12,A20,A28
Gradation Palette A5,A13,A21,A29 (Lower nibble) [AH]	0	1	0	1	0	0	1	1	0	1	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A5,A13,A21,A29
Gradation Palette A5,A13,A21,A29 (Upper nibble) [BH]	0	1	0	1	0	0	1	1	0	1	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A5,A13,A21,A29
Gradation Palette A6,A14,A22,A30 (Lower nibble) [CH]	0	1	0	1	0	0	1	1	1	0	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A6,A14,A22,A30
Gradation Palette A6,A14,A22,A30 (Upper nibble) [DH]	0	1	0	1	0	0	1	1	1	0	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A6,A14,A22,A30
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to " RE: set register bank number

Note: The asterisk "*" mark means "don't care"
Parentheses [ ] shows the control register address.

Control Register Table (Bank 2)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation Palette A7,A15,A23,A31 (Lower nibble) [0H]	0	1	0	1	0	1	0	0	0	0	0	PAX.3	PAX.2	PAX.1	PAX.0	Set the umber of Gradation Palette A7,A15,A23,A31
Gradation Palette A7,A15,A23,A31 (Upper nibble) [1H]	0	1	0	1	0	1	0	0	0	0	1	*	*	PAX.5	PAX.4	Set the umber of Gradation Palette A7,A15,A23,A31
Gradation Palette B0,B8,B16,B24 (Lower nibble) [2H]	0	1	0	1	0	1	0	0	0	1	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B0,B8,B16,B24
Gradation Palette B0,B8,B16,B24 (Upper nibble) [3H]	0	1	0	1	0	1	0	0	0	1	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B0,B8,B16,B24
Gradation Palette B1,B9,B17,B25 (Lower nibble) [4H]	0	1	0	1	0	1	0	0	1	0	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B1,B9,B17,B25
Gradation Palette B1,B9,B17,B25 (Upper nibble) [5H]	0	1	0	1	0	1	0	0	1	0	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B1,B9,B17,B25
Gradation Palette B2,B10,B18,B26 (Lower nibble) [6H]	0	1	0	1	0	1	0	0	1	1	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B2,B10,B18,B26
Gradation Palette B2,B10,B18,B26 (Upper nibble) [7H]	0	1	0	1	0	1	0	0	1	1	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B2,B10,B18,B26
Gradation Palette B3,B11,B19,B27 (Lower nibble) [8H]	0	1	0	1	0	1	0	1	0	0	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B3,B11,B19,B27
Gradation Palette B3,B11,B19,B27 (Upper nibble) [9H]	0	1	0	1	0	1	0	1	0	0	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B3,B11,B19,B27
Gradation Palette B4,B12,B20,B28 (Lower nibble) [AH]	0	1	0	1	0	1	0	1	0	1	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B4,B12,B20,B28
Gradation Palette B4,B12,B20,B28 (Upper nibble) [BH]	0	1	0	1	0	1	0	1	0	1	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B4,B12,B20,B28
Gradation Palette B5,B13,B21,B29 (Lower nibble) [CH]	0	1	0	1	0	1	0	1	1	0	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B5,B13,B21,B29
Gradation Palette B5,B13,B21,B29 (Upper nibble) [DH]	0	1	0	1	0	1	0	1	1	0	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B5,B13,B21,B29
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to " RE: set register bank number

Note: The asterisk "*" mark means "don't care"
Parentheses [ ] shows the control register address.

Control Register Table (Bank 3)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation Palette B6,B14,B22,B30 (Lower nibble) [0H]	0	1	0	1	0	1	1	0	0	0	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B6,B14,B22,B30
Gradation Palette B6,B14,B22,B30 (Upper nibble) [1H]	0	1	0	1	0	1	1	0	0	0	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B6,B14,B22,B30
Gradation Palette B7,B15,B23,B31 (Lower nibble) [2H]	0	1	0	1	0	1	1	0	0	1	0	PBX.3	PBX.2	PBX.1	PBX.0	Set the umber of Gradation Palette B7,B15,B23,B31
Gradation Palette B7,B15,B23,B31 (Upper nibble) [3H]	0	1	0	1	0	1	1	0	0	1	1	*	*	PBX.5	PBX.4	Set the umber of Gradation Palette B7,B15,B23,B31
Gradation Palette C0,C8,C16,C24 (Lower nibble) [4H]	0	1	0	1	0	1	1	0	1	0	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C0,C8,C16,C24
Gradation Palette C0,C8,C16,C24 (Upper nibble) [5H]	0	1	0	1	0	1	1	0	1	0	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C0,C8,C16,C24
Gradation Palette C1,C9,C17,C25 (Lower nibble) [6H]	0	1	0	1	0	1	1	0	1	1	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C1,C9,C17,C25
Gradation Palette C1,C9,C17,C25 (Upper nibble) [7H]	0	1	0	1	0	1	1	0	1	1	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C1,C9,C17,C25
Gradation Palette C2,C10,C18,C26 (Lower nibble) [8H]	0	1	0	1	0	1	1	1	0	0	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C2,C10,C18,C26
Gradation Palette C2,C10,C18,C26 (Upper nibble) [9H]	0	1	0	1	0	1	1	1	0	0	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C2,C10,C18,C26
Gradation Palette C3,C11,C19,C27 (Lower nibble) [AH]	0	1	0	1	0	1	1	1	0	1	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C3,C11,C19,C27
Gradation Palette C3,C11,C19,C27 (Upper nibble) [BH]	0	1	0	1	0	1	1	1	0	1	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C3,C11,C19,C27
Gradation Palette C4,C12,C20,C28 (Lower nibble) [CH]	0	1	0	1	0	1	1	1	1	0	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C4,C12,C20,C28
Gradation Palette C4,C12,C20,C28 (Upper nibble) [DH]	0	1	0	1	0	1	1	1	1	0	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C4,C12,C20,C28
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to " RE: set register bank number

Note: The asterisk "*" mark means "don't care"
Parentheses [ ] shows the control register address.

Control Register Table (Bank 4)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation Palette C5,C13,C21,C29 (Lower nibble) [0H]	0	1	0	1	1	0	0	0	0	0	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C5,C13,C21,C29
Gradation Palette C5,C13,C21,C29 (Upper nibble) [1H]	0	1	0	1	1	0	0	0	0	0	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C5,C13,C21,C29
Gradation Palette C6,C14,C22,C30 (Lower nibble) [2H]	0	1	0	1	1	0	0	0	0	1	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C6,C14,C22,C30
Gradation Palette C6,C14,C22,C30 (Upper nibble) [3H]	0	1	0	1	1	0	0	0	0	1	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C6,C14,C22,C30
Gradation Palette C7,C15,C23,C31 (Lower nibble) [4H]	0	1	0	1	1	0	0	0	1	0	0	PCX.3	PCX.2	PCX.1	PCX.0	Set the umber of Gradation Palette C7,C15,C23,C31
Gradation Palette C7,C15,C23,C31 (Upper nibble) [5H]	0	1	0	1	1	0	0	0	1	0	1	*	*	PCX.5	PCX.4	Set the umber of Gradation Palette C7,C15,C23,C31
Display start common [6H]	0	1	0	1	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Set Common Driver Start Line
Temperature Compensation [7H]	0	1	0	1	1	0	0	0	1	1	1	*	*	TCS1	TCS0	Temperature Compensation set
Display Select Control [8H]	0	1	0	1	1	0	0	1	0	0	0	PWM	GL SB	PS1	PS0	Select Plane(access/display) Select PWM Mode Set GLSB Bit.
RAM Data length Set [9H]	0	1	0	1	1	0	0	1	0	0	1	C256	HSW	ABS	WLS	Set Data length on RAM Access 8-bit access or 16-bit access
Electronic Volume (Lower nibble) [AH]	0	1	0	1	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Set Electronic Vollume Register (lower code)
Electronic Volume (Upper nibble) [BH]	0	1	0	1	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Set Electronic Vollume Register (upper code)
Register read Control [CH]	0	1	0	1	1	0	0	1	1	0	0	RA3	RA2	RA1	RA0	Set Register Address for read
Select Rf [DH]	0	1	0	1	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Select Rf ratio of OSC circuit
Extended Power Control [EH]	0	1	0	1	1	0	0	1	1	1	0	BF1	BF0	HPM	DIS	Discharge capacitance of V0,V1,V2,V3,V4 Pins
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to " RE: set register bank number

Note: The asterisk "*" mark means "don't care".
Parentheses [ ] shows the control register address.

Control Register Table (Bank 5)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Window X End Address (Lower nibble) [0H]	0	1	0	1	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Set X end address for window function access
Window X End Address (Upper nibble) [1H]	0	1	0	1	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Set X end address for window function access
Window Y End Address (Lower nibble) [2H]	0	1	0	1	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Set Y end address for window function access
Window Y End Address (Upper nibble) [3H]	0	1	0	1	1	0	1	0	0	1	1	EY7	EY6	EY5	EY4	Set Y end address for window function access
Start Address for line reverse (Lower nibble) [4H]	0	1	0	1	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Set start line for line reverse display
Start Address for line reverse (Upper nibble) [5H]	0	1	0	1	1	0	1	0	1	0	1	LS7	LS6	LS5	LS4	Set start line for line reverse display
End Address for line reverse (Lower nibble) [6H]	0	1	0	1	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Set end line for line reverse display
End Address for line reverse (Upper nibble) [7H]	0	1	0	1	1	0	1	0	1	1	1	LE7	LE6	LE5	LE4	Set end line for line reverse display
Line reverse control Burst RAM write control Reverse type [8H]	0	1	0	1	1	0	1	1	0	0	0	*	BST	BT	LR EV	BST: Burst RAM write ON / OFF BT: Reverse type select LREV: Line reverse control
Regulator multiple ratio Control Register [9H]	0	1	0	1	1	0	1	1	0	0	1	*	RM2	RM1	RM0	set regulator multiple ratio
EEPROM mode select register [AH]	0	1	0	1	1	0	1	1	0	1	0	M1	M0	VPP_ EXT	OSC	M1,M0:EEPROM mode select VPP_EXT:EEPROM power select OSC:oscillator frequency select
Vop calibration offset register [BH]	0	1	0	1	1	0	1	1	0	1	1	CV4	CV3	CV2	CV1	set Vop offset voltage
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0:for LS1 test,must set to "0" RE:set register bank number

Note: The asterisk "*" mark means "don't care"
Parentheses [ ] shows the control register address.
Address [CH], [DH], [EH] in Bank 5 of the control register are reserved.

8.2 Control Register Functions

The EM65571 has many control registers. In case of control register access, the upper nibble of the data bus (D7~D4) represents the register address, the lower nibble of the data bus (D3~D0) represents the data. The access example is shown in the following. The Pins (CSB, RS, RDB, WRB) setting is for the 80-family MPU interface. Only the setting of the terminal (RDB, WRB) is different, when it is accessed by the 68-family MPU.

Example: X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

Register address | Data

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Pins setting | Register Bank

In writing to the control register, direct addressing to D7~D4 of the data bus can be used. In case of a register read, first set the RA register for a specific register address, next read that specific register. Therefore, two steps are needed to perform a register read. Then, specific register output to D3~D0 of the data bus. Except for D3~D0 of the data bus, all are "H". Access to undefined register address area is not allowed. When RS is "L", all read/write operations are accessible in the display RAM. The data bus does not include the register address. In case of a write operation, D3~D0 data is written to the register designated at D7~D4 at the rising edge of the WRB signal. In

case of a read, a register can output to the data bus in RDB active period. The control register and display RAM have equal access time.

8.2.1 X-address Register (AX)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {AX3, AX2, AX1, AX0} = 0H, read address: 0H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AX7	AX6	AX5	AX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {AX7, AX6, AX5, AX4} = 0H, read address: 1H

The AX register is set to X-address of the display RAM. Data setting is divided into the lower nibble and the upper nibble or 4-bit each.

8.2.2 Y-Address Register (AY)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	AY3	AX2	AY1	AY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {AY3, AY2, AY1, AY0} = 0H, read address: 2H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	AY7	AY6	AY5	AY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {AY7, AY6, AY5, AY4} = 0H, read address: 3H

The AY register is set to Y-address of the display RAM. Data setting is divided into the lower nibble and the upper nibble or 4-bit each. Addresses 00H to 7FH corresponds to AY7 to AY0, and (NO AND operation) 80H to FFH are reserved but the addresses for (AY7 to AY0) = A0H, A1H are in the display RAM area for icon display.

8.2.3 Display Start Address Register (LA)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LA3	LA2	LA1	LA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {LA3, LA2, LA1, LA0}=0H, read address: 4H

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	LA7	LA6	LA5	LA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {LA7, LA6, LA5, LA4}=0H, read address: 5H

The LA register indicate first the output segment data in the display RAM. This segment data output to the common line is indicated by the SC register. After that the output common line is incremented.

LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	Line Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				j :				
0	1	1	1	1	1	1	1	127

8.2.4 n-line Alternate Register (N)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	N3	N2	N1	N0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {N3, N2, N1, N0} = 0H, read address: 6H

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	N7	N6	N5	N4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

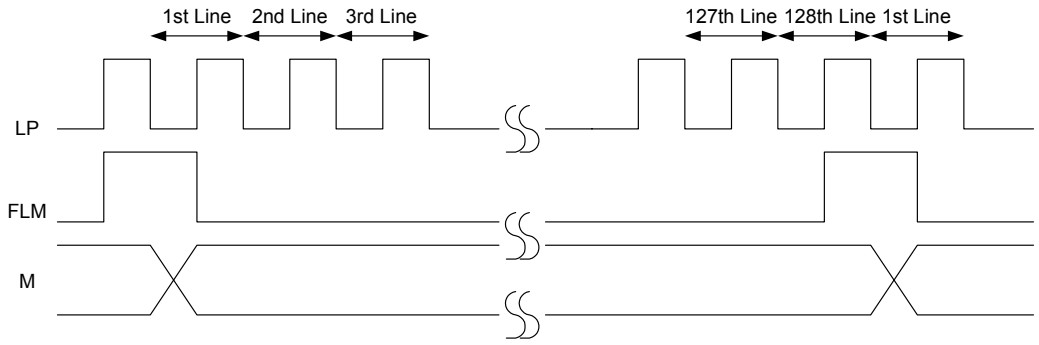
Note: During a reset: {N6, N5, N4} = 0H, read address: 7H

The reverse line number of the LCD alternate driver is required to be set in the register. The line number has a limit, which must be kept between 2 to 127 lines. The value set up by the alternate register is enabled when NLIN control bit is “1”. When NLIN control bit is “0”, the alternate driver waveform reverses each frame that is generated.

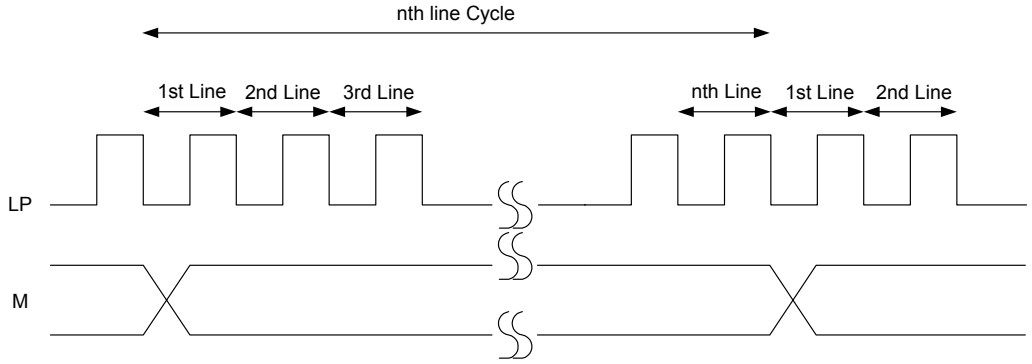
N7	N6	N5	N4	N3	N2	N1	N0	Line Address
0	0	0	0	0	0	0	0	-
0	0	0	0	0	0	0	1	2
				j j				
0	1	1	1	1	1	1	0	127

Alternate Timing

(i) NLIN = ”0” (in case of 1/128 DUTY Display)



(ii) NLIN = ”1”



8.2.5 Display Control (1) Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SHIFT	65K	ALLON	ON/OFF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {SHIFT, 65K, ALLON, ON/OFF} = 4H, read address: 8H

Various display controls are set up.

- ON/OFF
  To control display ON/OFF
  ON/OFF = “0”: Display OFF
  ON/OFF = “1”: Display ON

- ALLON
  Regardless of the data for display, all is on.
  This control has priority over display normal/reverse commands.
  ALLON = “0”: Normal display
  ALLON = “1”: All display lighted

- 65K
  Select 65K gradation display
  65K=”0”: 4096 or 256 gradation display, decided by C256 control bit.
  65K=”1”: 65K gradation display mode.

- SHIFT
  The shift direction of display scanning data in the common driver output is selected.
  SHIFT = “0”: COM0 → COM127 shift-scan
  SHIFT = “1”: COM127 → COM0 shift-scan

8.2.6 Display Control (2) Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	REV	NLIN	SWAP	REF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {REV, NLIN, SWAP, REF} = 0H, read address: 9H

Various display controls are set up.

✧ REF

When the MPU accesses the display RAM, the X address and data can reverse. The REF function is shown in the table below:

REF	Access from the MPU		Internal Access		Corresponding Segment Output
	X Address	D7-D0	X Address	D7-D0	
0	NH	D0(LSB) j D7(MSB)	NH	(LSB) j (MSB)	SEG(8*NH)Output j SEG(8*NH+7)Output
1	NH	D0(LSB) j D7(MSB)	MaxH-NH	(MSB) j (LSB)	SEG(8*(maxH-NH)+7)Output j SEG(8*(maxH-NH))Output

Note: maxH: The maximum X-address in each access mode.

The order of segment driver output can be reversed by the register, by register setting, thus lessening the limitations in placing the IC during an LCD module assembly.

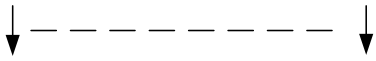
✧ NLIN

The NLIN control n-line alternate driver.
NLIN = “0”: n-line alternate driver OFF. In each frame, the alternate signals (M) are reversed.
NLIN =”1”: n-line alternate driver ON. Alternate is performed in accordance to data set up in the n-line alternate register.

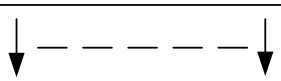
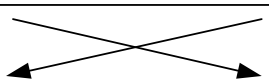
✧ SWAP

When data are written to the display RAM, the bit order of the written data are exchanged.
SWAP = “0”: Normal mode
SWAP = “1”: In data writing, bit order is exchange.

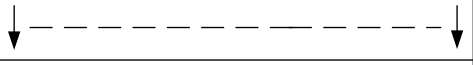
Example of exchanged bit order

Write Data	SWAP = 0	SWAP = 1
	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
		
Internal Data	d0 d1 d2 d3 d4 d5 d6 d7 d8 d9 d10 d11	d11 d10 d9 d8 d7 d6 d5 d4 d3 d2 d1 d0

8-bit Access (HSW=1)

Write Data	SWAP = 0	SWAP = 1
	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7
		
Internal Data	d0 d1 d2 d3 d4 d5 d6 d7	d7 d6 d5 d4 d3 d2 d1 d0

16-bit access (HSW=1)

Write Data	SWAP=0	SWAP=1
	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
		
Internal Data	d0 d1 d2 d3 d4 d5 d6 d7 d8 d9 d10 d11 d12 d13 d14 d15	d15 d14 d13 d12 d11 d10 d9 d8 d7 d6 d5 d4 d3 d2 d1 d0

CAUTION: REF and SWAP should both be set to "1"
When data is written to the display RAM, the written data is in normal bit order.
When data is read from the display RAM, the bit order of the read data is exchanged.

- REV
  In accordance to the of display RAM data, the lighting or not-lighting of the display is set up.
  REV ="0": When RAM data is at "H", the LCD voltage is ON (normal)
  REV ="1": When RAM data is at "L", the LCD voltage is ON (reversed)

8.2.6 Increment Control Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	WIN	AIM	AYI	AXI

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(During a reset: {WIN, AIM, AYI, AXI} = 0H, read address: AH)

This register controls the increment mode and window function when accessing the display RAM. The increment operation of AX and AY registers can be controlled by AIM, AYI and AXI registers setting and every write access or every read access to the display RAM. The AY register directly connects to the display RAM as Y address. The AX register connects to the address converter, and outputs to the display RAM as X address in the auto-increment mode, the AX and AY register are then incremented, but not directly increment the X and Y addresses.

In setting the control register, the address increment operation can be made without setting successive addresses for writing data to the display RAM or reading data from the MPU.

The WIN register is used for window function control.

WIN="0": Normal RAM access
WIN="1": Window function access

In the case of accessing the window function, the following register should be set before accessing the RAM.

WIN="1", AXI="1", AYI="1"
X-address, Y-address, Window X End Address, Window Y End Address

Moreover, the following address condition should be kept:

Window end X address Window start X address
Window end Y address Window start Y address

Refer to "6-7 Display RAM access using Window Function" for details on window function.

The increment control of X and Y-addresses by AIM, AYI and AXI registers are as follows.

AIM	Address Increment Timing
0	When writing to or reading from the Display RAM. This is effective when accessing successive address areas.
1	Only when writing to the Display RAM. This is effective the case of “Read Modify Write”

AYI	AXI	Select Address Increment Operation	Remark
0	0	Address is not incremented	(1)
0	1	X-Address is incremented	(2)
1	0	Y-Address is incremented	(3)
1	1	X and Y both are incremented	(4)

(1) Regardless of AIM, no increment for AX and AY register.
(2) Basing on the set-up of the AIM, automatically change the X-address.

In accordance with the REF register, the AX register and X-address becomes as follows.

REF	Transition of AX Register	Transition of X Address
0		Same as AX register
1	00H→ 01H→.....→max	max→ maxH→.... →00H

Note: maxH: internal maximum X-address in each access mode.

(3) Basing on the set-up of the AIM, automatically change the Y-address. Regardless of REF, increment by looping.

Transition of AY Register	Transition of Y Address
00H→ 01H→..... →7FH	Same as AY register

(4) According to the set-up of the AIM, simultaneously change the X and Y-address. When the X-address exceeds maxH, the Y-address incremented.

REF	Transition of AX and AY Register	Transition of X and Y Address
0	AX: 00H → 00H→ – – → max	Same as AX and AY register
1	AY: When each AX exceed maxH, increment AY 00H → 00H→ – – → 7FH	AX: max→ maxH→ – – →00H AY: Same as AY register

Note: maxH: The internal maximum X-address in each access mode.
Following shows address increment in window function access.

REF	Transition of AX and AY Register	Transition of X and Y Address
0	AX:	Same as AX and AY register
1	AX: START Address → START Address+1 → _ _ → END Address AY: When each AX exceed AE, increment AY AY: START Address → START Address+1 → _ _ → END Address	AX: maxH-(START Address) → maxH-(START Address+1) → _ _ → maxH-(END Address) AY: Same as AY register

Note: maxH: The internal maximum X-address in each access mode.

In each operation mode, the following increment operation is performed:

(i) When gradation display mode, 8-bit access is selected
Address is incremented as described above.

(ii) When in gradation display mode and 16-bit access are selected:

Accessing the RAM once, accesses two bytes.
The X-addresses increment in the order of 00H, 01H,…3EH, and 3FH.

8.2.7 Power Control Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	AMPON	HALT	DCON	ACL

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(During a reset: {AMPON, HALT, DCON, ACL} = 0H, read address: BH)

- ACL
  The internal circuit can be initialized.
  ACL = “0”: Normal operation
  ACL = “1”: Initialization ON
  When a reset operation begins internally after the ACL register is set to “1”, the ACL register is automatically cleared to “0”. An internal reset signal is generated by a clock (built-in oscillation circuit or CK input) for the display. Hence, include a WAIT period for the display clock for at least two cycles. After a WAIT period, proceed with the next operation.

- DCON
  The internal booster circuit is set ON/OFF
  DCON = “0”: Booster circuit OFF
  DCON=”1”: Booster circuit ON

- HALT
  The conditions of power saving are set ON/OFF by this command.
  HALT = “0”: Normal operation
  HALT=”1”: Power-saving operation
  When setting in the power-saving state, the consumed current can be reduced to a value near to the standby current.

The internal conditions at power saving are as follows.

a. The oscillating circuit and power supply circuit are stopped.
b. The LCD driver is stopped, and output of the segment driver and common driver are VSS level.
c. The clock input from the CK pin is inhibited.
d. The contents of the Display RAM data are maintained.
e. The operational mode maintains the state of command execution before executing power saving command.

✧ AMPON Command

The internal OP-AMP circuit block (voltage regulator, electronic volume, and voltage conversion circuit) is set ON/OFF by this command.
AMPON = “0”: The internal OP-AMP circuit OFF
AMPON = ”1”: The internal OP-AMP circuit ON

8.2.8 LCD Duty (DS)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	DS3	DS2	DS1	DS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {DS3, DS2, DS1, DS0} = 0H, read address: CH

The DS register is set to LCD display duty.

DS3	DS2	DS1	DS0	Display Width and Duty
0	0	0	0	8-dot width display in Y-direction, 1/10 duty
0	0	0	1	16-dot width display in Y-direction, 1/18 duty
0	0	1	0	24-dot width display in Y-direction, 1/26 duty
0	0	1	1	32-dot width display in Y-direction, 1/34 duty
0	1	0	0	48-dot width display in Y-direction, 1/50 duty
0	1	0	1	64-dot width display in Y-direction, 1/66 duty
0	1	1	0	72-dot width display in Y-direction, 1/74 duty
0	1	1	1	80-dot width display in Y-direction, 1/82 duty
1	0	0	0	96-dot width display in Y-direction, 1/98 duty
1	0	0	1	104-dot width display in Y-direction, 1/106 duty
1	0	1	0	112-dot width display in Y-direction, 1/114 duty
1	0	1	1	120-dot width display in Y-direction, 1/122 duty
1	1	1	1	128-dot width display in Y-direction, 1/130 duty

Partial display can be made possible by setting an arbitrary duty ratio.

8.2.9 Booster Setup (VU)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	*	VU2	VU1	VU0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {VU2, VU1, VU0} = 0H, read address: DH
The asterisk “*” mark means “Don’t care”

The booster steps setting for the VU register

VU2	VU1	VU0	Booster Operation
0	0	0	Booster disable (No operation)
0	0	1	2 times voltage output
0	1	0	3 times voltage output
0	1	1	4 times voltage output
1	0	0	5 times voltage output
1	0	1	6 times voltage output
1	1	0	7 times voltage output
1	1	1	Prohibit code

8.2.10 Bias Setting Register (B)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	B3	B2	B1	B0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {B3, B2, B1, B0} = 0H, read address: EH

This register is used to set the bias ratio. A bias ratio can be selected from 1/5 to 1/13 by setting B3, B2, B1, and B0.

B3	B2	B1	B0	Bias
0	0	0	0	1/5 Bias
0	0	0	1	1/6 Bias
0	0	1	0	1/7 Bias
0	0	1	1	1/8 Bias
0	1	0	0	1/9 Bias
0	1	0	1	1/10 Bias
0	1	1	0	1/11 Bias
0	1	1	1	1/12 Bias
1	0	0	0	1/13 Bias
1	0	0	1	Prohibit code
1	0	1	0	Prohibit code
1	0	1	1	Prohibit code
1	1	0	0	Prohibit code
1	1	0	1	Prohibit code
1	1	1	0	Prohibit code
1	1	1	1	Prohibit code

8.2.11 Register Access Control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	TST0	RE2	RE1	RE0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

Note: During a reset: {TST0, RE2, RE1, RE0} = 0H, read address: FH

The RE register is use set to number of register bank. In accessing each control register, set the RE register first.
The TST0 register is use for testing purposes, hence, this register must be set to “0”

8.2.13 Gradation Palette Register (PA0~PA7, PB0~PB7, PC0~PC7)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 0H
X= 0, 8, 16, or 24

D7	D6	D5	D4	D3	D2	D1	D0/
0	0	0	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 1H
X= 0, 8, 16, or 24
During a reset: PA04~PA00 = “00000”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 2H
X= 1, 9, 17, or 25

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 3H
X= 1, 9, 17, or 25
During a reset: PA14~PA10 = "00101")
The asterisk "*" mark means "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 4H
X= 2, 10, 18, or 26

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 5H
X= 2, 10, 18, or 26
During a reset: PA24~PA20 = "01010"
The asterisk "*" mark means "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 6H
X= 3, 11, 19, or 27

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 7H
X= 3, 11, 19, or 27
During a reset: PA34~PA30 = "01110"
The asterisk "*" mark means "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 8H
X= 4, 12, 20, or 28

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: 9H
X= 4, 12, 20, or 28
During a reset: PA44~PA40 = "10001"
The asterisk "*" mark means "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: AH
X= 5, 13, 21, or 29

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: BH
X= 5, 13, 21, or 29
During a reset: PA54~PA50 = “10101”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: CH
X= 6, 14, 22, or 30

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

Note: Read address: DH
X= 6, 14, 22, or 30
During a reset: PA64~PA60 = “11010”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PAX.3	PAX.2	PAX.1	PAX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 0H
X= 7, 15, 23, or 31

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	PAX.5	PAX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 1H
X= 7, 15, 23, or 31
During a reset: PA74~PA70 = “11111”
The asterisk “*”mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 2H
X= 0, 8, 16, or 24

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 3H
X= 0, 8, 16, or 24
During a reset: PB04~PB00 = “00000”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 4H
X= 1, 9, 17, or 25

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 5H
X= 1, 9, 17, or 25
During a reset: PB14~PB10 = “00101”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 6H
X= 2, 10, 18, or 26

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 7H
X= 2, 10, 18, or 26
During a reset: PB24~PB20 = “01010”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 8H
X= 3, 11, 19, or 27

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	–	–	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: 9H
X= 3, 11, 19, or 27
During a reset: PB34~PB30 = “01110”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: AH
X= 4, 12, 20, or 28

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	*	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: BH
X= 4, 12, 20, or 28
During a reset: PB44~PB40 = “10001”)
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: CH
X= 5, 13, 21, or 29

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	*	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

Note: Read address: DH
X= 5, 13, 21, or 29
During a reset: PB54~PB50 = “00101”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 0H
X= 6, 14, 22, or 30

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 1H
X= 6, 14, 22, or 30
During a reset: PB64~PB60 = “11010”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PBX.3	PBX.2	PBX.1	PBX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 2H
X= 7, 15, 23, or 31

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	PBX.5	PBX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 3H
X= 7, 15, 23, or 31
During a reset: PB74~PB70 = “11111”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 4H
X= 0, 8, 16, or 24

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 5H
X= 0, 8, 16, or 24
During a reset: PC04~PC00 = “00000”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 6H
X= 1, 9, 17, or 25

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 7H
X= 1, 9, 17, or 25
During a reset: PC14~PC10 = “00101”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 8H
X= 2, 10, 18, or 26

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	–	–	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: 9H
X= 2, 10, 18, or 26
During a reset: PC24~PC20 = “01010”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: AH
X= 3, 11, 19, or 27

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	*	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: BH
X= 3, 11, 19, or 27
During a reset: PC34~PC30 = “01110”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: CH
X= 4, 12, 20, or 28

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	*	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

Note: Read address: DH
= 4, 12, 20, or 28
During a reset: PC44~PC40 = “10001”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: 0H
X= 5, 13, 21, or 29

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: 1H
X= 5, 13, 21, or 29
During a reset: PC54~PC50 = “10101”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: 2H
X= 6, 14, 22, or 30

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: 3H
X= 6, 14, 22, or 30
During a reset: PC64~PC60 = “11010”
The asterisk “*” mark means “Don’t care”

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PCX.3	PCX.2	PCX.1	PCX.0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: 4H
X= 7, 15, 23, or 31

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	–	–	PCX.5	PCX.4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: 5H
X= 7, 15, 23, or 31
During a reset: PC74~PC70 = “11111”
The asterisk “*” mark means “Don’t care”

These gradation palette registers set up the gradation level. The EM65571 has 48 gradation levels.

Gradation level table (PWM = “0”, variable mode, 65K= “1”, C256=”*”)
[Three groups of Palettes Aj, Bj, and Cj (j = 0-31) are available

Palette	Gradation Level	Remarks	Palette	Gradation Level	Remarks
0 0 0 0 0 0	0	Gradation Palette0 Initial Value	0 1 1 0 0 0	24/48	Gradation Palette16 Initial Value
0 0 0 0 0 1	1/48		0 1 1 0 0 1	25/48	
0 0 0 0 1 0	2/48	Gradation Palette1 Initial Value	0 1 1 0 1 0	26/48	Gradation Palette17 Initial Value
0 0 0 0 1 1	3/48	Gradation Palette2 Initial Value	0 1 1 0 1 1	27/48	Gradation Palette18 Initial Value
0 0 0 1 0 0	4/48		0 1 1 1 0 0	28/48	
0 0 0 1 0 1	5/48	Gradation Palette3 Initial Value	0 1 1 1 0 1	29/48	Gradation Palette19 Initial Value
0 0 0 1 1 0	6/48	Gradation Palette4 Initial Value	0 1 1 1 1 0	30/48	Gradation Palette20 Initial Value
0 0 0 1 1 1	7//48		0 1 1 1 1 1	31/48	
0 0 1 0 0 0	8/48	Gradation Palette5 Initial Value	1 0 0 0 0	32/48	Gradation Palette21 Initial Value
0 0 1 0 0 1	9/48	Gradation Palette6 Initial Value	1 0 0 0 0 1	33/48	Gradation Palette22 Initial Value
0 0 1 0 1 0	10/48		1 0 0 0 1 0	34/48	
0 0 1 0 1 1	11/48	Gradation Palette7 Initial Value	1 0 0 0 1 1	35/48	Gradation Palette23 Initial Value
0 0 1 1 0 0	12/48	Gradation Palette8 Initial Value	1 0 0 1 0 0	36/48	Gradation Palette24 Initial Value
0 0 1 1 0 1	13/48		1 0 0 1 0 1	37/48	
0 0 1 1 1 0	14/48	Gradation Palette9 Initial Value	1 0 0 1 1 0	38/48	Gradation Palette25 Initial Value
0 0 1 1 1 1	15/48	Gradation Palette10 Initial Value	1 0 0 1 1 1	39/48	Gradation Palette26 Initial Value
0 1 0 0 0 0	16/48		1 0 1 0 0 0	40/48	
0 1 0 0 0 1	17/48	Gradation Palette11 Initial Value	1 0 1 0 0 1	41/48	Gradation Palette27 Initial Value
0 1 0 0 1 0	18/48	Gradation Palette12 Initial Value	1 0 1 0 1 0	42/48	Gradation Palette28 Initial Value
0 1 0 0 1 1	19/48		1 0 1 0 1 1	43/48	
0 1 0 1 0 0	20/48	Gradation Palette13 Initial Value	1 0 1 1 0 0	44/48	Gradation Palette29 Initial Value
0 1 0 1 0 1	21/48	Gradation Palette14 Initial Value	1 0 1 1 0 1	45/48	Gradation Palette30 Initial Value
0 1 0 1 1 0	22/48		1 0 1 1 1 0	46/48	
0 1 0 1 1 1	23/48	Gradation Palette15 Initial Value	1 0 1 1 1 1	47/48	Gradation Palette31 Initial Value

Gradation level table (PWM = “0”, variable mode, 65K= “0”, C256=”0”)
[Three groups of Palettes Aj, Bj, and Cj (j = 0-15) are available

Palette	Gradation Level	Remarks	Palette	Gradation Level	Remarks
0 0 0 0 0 0	0	Gradation Palette0 Initial Value	0 1 1 0 0 0	24/48	
0 0 0 0 0 1	1/48		0 1 1 0 0 1	25/48	Gradation Palette8 Initial Value
0 0 0 0 1 0	2/48		0 1 1 0 1 0	26/48	
0 0 0 0 1 1	3/48	Gradation Palette1 Initial Value	0 1 1 0 1 1	27/48	
0 0 0 1 0 0	4/48		0 1 1 1 0 0	28/48	Gradation Palette9 Initial Value
0 0 0 1 0 1	5/48		0 1 1 1 0 1	29/48	
0 0 0 1 1 0	6/48	Gradation Palette2 Initial Value	0 1 1 1 1 0	30/48	
0 0 0 1 1 1	7//48		0 1 1 1 1 1	31/48	Gradation Palette10 Initial Value
0 0 1 0 0 0	8/48		1 0 0 0 0	32/48	
0 0 1 0 0 1	9/48	Gradation Palette3 Initial Value	1 0 0 0 0 1	33/48	
0 0 1 0 1 0	10/48		1 0 0 0 1 0	34/48	Gradation Palette11 Initial Value
0 0 1 0 1 1	11/48		1 0 0 0 1 1	35/48	
0 0 1 1 0 0	12/48	Gradation Palette4 Initial Value	1 0 0 1 0 0	36/48	
0 0 1 1 0 1	13/48		1 0 0 1 0 1	37/48	Gradation Palette12 Initial Value
0 0 1 1 1 0	14/48		1 0 0 1 1 0	38/48	
0 0 1 1 1 1	15/48	Gradation Palette5 Initial Value	1 0 0 1 1 1	39/48	
0 1 0 0 0 0	16/48		1 0 1 0 0 0	40/48	Gradation Palette13 Initial Value
0 1 0 0 0 1	17/48		1 0 1 0 0 1	41/48	
0 1 0 0 1 0	18/48	Gradation Palette6 Initial Value	1 0 1 0 1 0	42/48	
0 1 0 0 1 1	19/48		1 0 1 0 1 1	43/48	Gradation Palette14 Initial Value
0 1 0 1 0 0	20/48		1 0 1 1 0 0	44/48	
0 1 0 1 0 1	21/48	Gradation Palette7 Initial Value	1 0 1 1 0 1	45/48	
0 1 0 1 1 0	22/48		1 0 1 1 1 0	46/48	Gradation Palette15 Initial Value
0 1 0 1 1 1	23/48		1 0 1 1 1 1	47/48	

Gradation level table (PWM = “0”, variable mode, 65K= “0”, C256=”1”)
[Three groups of Palettes Aj, Bj, and Cj (j = 0-7) are available

Palette	Gradation Level	Remarks	Palette	Gradation Level	Remarks
0 0 0 0 0 0	0	Gradation Palette0 Initial Value	0 1 1 0 0 0	24/48	
0 0 0 0 0 1	1/48		0 1 1 0 0 1	25/48	
0 0 0 0 1 0	2/48		0 1 1 0 1 0	26/48	Gradation Palette4 Initial Value
0 0 0 0 1 1	3/48		0 1 1 0 1 1	27/48	
0 0 0 1 0 0	4/48	Gradation Palette1 Initial Value	0 1 1 1 0 0	28/48	
0 0 0 1 0 1	5/48		0 1 1 1 0 1	29/48	
0 0 0 1 1 0	6/48		0 1 1 1 1 0	30/48	
0 0 0 1 1 1	7//48		0 1 1 1 1 1	31/48	
0 0 1 0 0 0	8/48		1 0 0 0 0 0	32/48	
0 0 1 0 0 1	9/48		1 0 0 0 0 1	33/48	Gradation Palette5 Initial Value
0 0 1 0 1 0	10/48		1 0 0 0 1 0	34/48	
0 0 1 0 1 1	11/48	Gradation Palette2 Initial Value	1 0 0 0 1 1	35/48	
0 0 1 1 0 0	12/48		1 0 0 1 0 0	36/48	
0 0 1 1 0 1	13/48		1 0 0 1 0 1	37/48	
0 0 1 1 1 0	14/48		1 0 0 1 1 0	38/48	
0 0 1 1 1 1	15/48		1 0 0 1 1 1	39/48	
0 1 0 0 0 0	16/48		1 0 1 0 0 0	40/48	Gradation Palette6 Initial Value
0 1 0 0 0 1	17/48		1 0 1 0 0 1	41/48	
0 1 0 0 1 0	18/48		1 0 1 0 1 0	42/48	
0 1 0 0 1 1	19/48	Gradation Palette3 Initial Value	1 0 1 0 1 1	43/48	
0 1 0 1 0 0	20/48		1 0 1 1 0 0	44/48	
0 1 0 1 0 1	21/48		1 0 1 1 0 1	45/48	
0 1 0 1 1 0	22/48		1 0 1 1 1 0	46/48	
0 1 0 1 1 1	23/48		1 0 1 1 1 1	47/48	Gradation Palette7 Initial Value

8.2.14 Display Start Common

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	SC3	SC2	SC1	SC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: During a reset:{ SC2, SC1, SC0} = 0H, read address: 6H

The SC register set up the scanning start output of the common driver.

SC3	SC2	SC1	SC0	Display Starting Common when SHIFT=0	Display Starting Common when SHIFT=1
0	0	0	0	COM0~	
0	0	0	1	COM10~	
0	0	1	0	COM20~	
0	0	1	1	COM30~	
0	1	0	0	COM40~	COM119~
0	1	0	1	COM50~	COM109~
0	1	1	0	COM60~	COM99~
0	1	1	1	COM70~	COM89~
1	0	0	0	COM80~	COM79~
1	0	0	1	COM90~	COM69~
1	0	1	0	COM100~	COM59~
1	0	1	1	COM110~	COM49~
1	1	0	0	COM120~	COM39~
1	1	0	1		COM29~
1	1	1	0		COM19~
1	1	1	1		COM9~

Note: SHIFT="0": COM0 to COM127 shift-scan
SHIFT="1": COM127 down to COM0 shift-scan

8.2.15 Temperature Compensation Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	TCS1	TCS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: During a reset:{ TCS1,TCS0 } = 0H, read address: 7H
The asterisk "*" mark means "Don't care"

TCS1	TCS0	Temperature Compensation Slope
0	0	-0.05% per °C
0	1	-0.1% per °C
1	0	-0.15% per °C
1	1	-0.2% per °C

The VREF (T) (Temperature compensation output voltage) is controlled by TCS1, TCS0 and the previous environment temperature T.

$$V_{REF}(T) = V_{REF0}[1 + TCS(25°C - T)]$$

TCS is selected by TCS1 and TCS0, VREF0 = 1.5V at 25°C

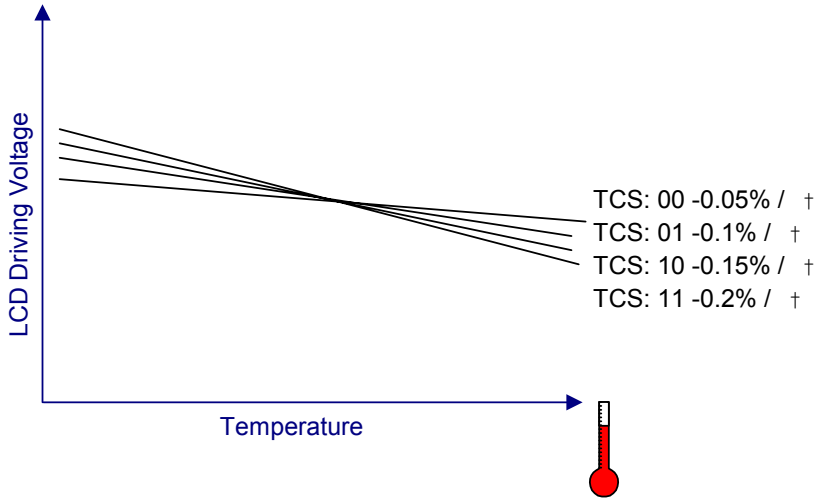


Figure 11 Temperature Compensation Slope

8.2.16 Display Select Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PWM	GLSB	PS1	PS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: During a reset: {PWM, GLSB} = 0H, read address: 8H)

- ✧ GLSB

  In 256 color mode, for the segment driver of 4-gradation display, select 4 gradations from 8 gradations using the 2 bits written to the corresponding RAM area and the 1 bit supplemented by the gradation LSB circuit. Supplement the 1 bit of data by setting the gradation LSB register (GLSB).

  Gradation LSB = "0": Selects 0 as the LSB information on the RAM for 4-gradation segment driver.

  Gradation LSB = "1": Selects 1 as the LSB information on the RAM for 4-gradation segment driver.

- ✧ PS1, PS0

  In 65K color mode, select the 48 gradation level from the 32 gradation palette. In 4096-color mode, select the 16 gradation level from the 32 gradation palette. In 256 color mode, just select a setting lower than 8 gradation.

PS1, PS0	Selected Palette
(0, 0)	PaletteX0~PaletteX7
(0, 1)	PaletteX8~PaletteX15
(1, 0)	PaletteX16~PaletteX23
(1, 1)	PaletteX24~PaletteX31

**X: A, B or C*

✧ PWM
The PWM register selects the gradation display mode.
PWM = “0”: Variable display mode using 32 gradations selected from 48 gradations in 65K color mode (65K=1, C256=”*”)
Variable display mode using 16 gradations selected from 48 gradations in 4096 color mode (65K=0, C256=0)
Variable display mode using 8 gradations selected from 48 gradations in 256 color mode (65K=0, C256=1)
PWM = “1”: 32-gradation fixed display mode

8.2.17 Data Bus Size Select

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	C256	HSW	ABS	WLS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: During a reset: {C256, HSW, ABS, WLS} = 0H, read address: 9H

✧ WLS
The WLS register selects a data bus size in accessing the MPU
WLS = “0”: The data bus size is 8-bit width
WLS = “1”: The data bus size is 16-bit width
When an MPU access to the control register used 16-bit bus size, high byte data is ignored.

✧ ABS
ABS= “0”: normal mode
ABS= “1”: change corresponding bit from input data bus

✧ HSW
HSW=“0”: High speed writing mode off
HSW=“1”: High speed writing mode on accessing the 8-bit data RAM

✧ C256
C256= “0”: 4096-color mode
C256= “1”: 256-color mode
*IF 65K=1, C256 is prohibited control bit.

8.2.18 Electronic Volume Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	DV3	DV2	DV1	DV0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: AH

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	DV6	DV5	DV4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: Read address: BH
During a reset: {DV6~DV0} = 00H
The asterisk “*” mark means “Don’t care”

The DV register can control the VBA voltage.
The DV register has 7 bits, so a 113 level voltage can be selected.

DV6	DV5	DV4	DV3	DV2	DV1	DV0	Output Voltage
0	0	0	1	0	0	0	8 (Smaller)
0	0	0	1	0	0	1	j
			j j				j j
1	1	1	0	1	1	1	j
1	1	1	1	0	0	0	120 (Larger)

The output voltage at VBA is specified by equation (1).

$$VBA = \left[1 + \frac{M + Offset}{381}\right] \times VREF \qquad (1)$$

where M: DV register value

Offset: CV1~CV4 setting

VREF: internal temperature compensation output voltage

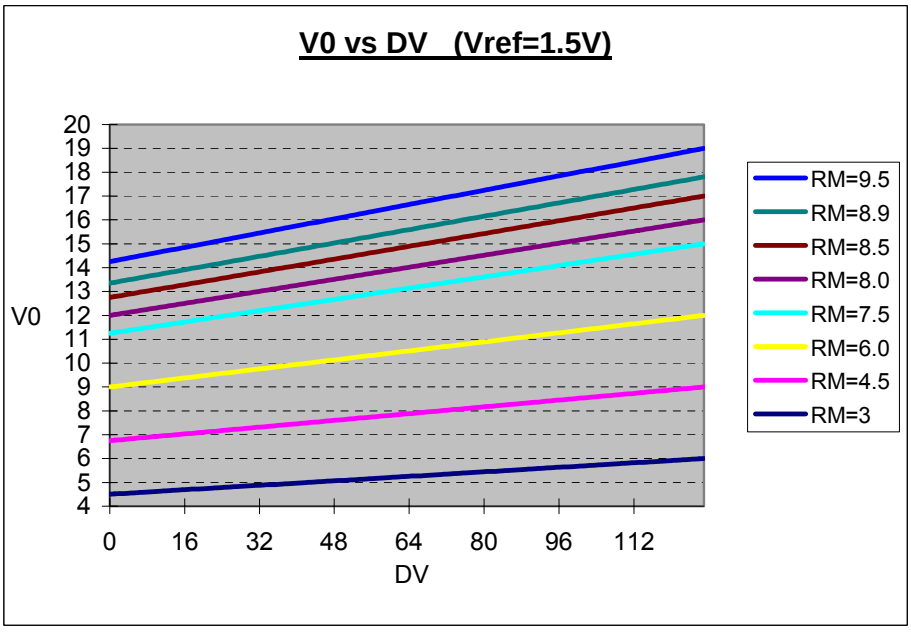
VBA ranges from 1.5V to 2V at 25 °C

The LCD driver voltage V0 is determined by the VBA level and the RM register value in equation (2).

$$V0 = VBA \times N \qquad (2)$$

where N : RM register setting

The relationship between V0 and DV setting values (when Vref = 1.5V) is shown below:



In order to prevent a transient voltage from being generated when an electronic volume code is set, the circuit is designed in such a way that the set value is not reflected immediately as a level but only after the upper bits (DV6-DV4) of the electronic code have been set. The set value becomes valid when the lower bits (DV3-DV0) of the electronic control volume code have also been set.

8.2.19 Resistance Ratio of CR Oscillator

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	RF2	RF1	RF0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: During a reset: {RF2, RF1, RF0} = 0H, read address: DH
The asterisk "*" mark means "Don't care"

The RF registers can control the resistance ratio of the CR oscillator. Therefore the frame frequency can change the RF register setting.
When changing the RF register value, the LCD display quality should be checked.

RF2	RF1	RF0	Operation
0	0	0	Initial Resistance Ratio
0	0	1	0.7 times the Initial Resistance Ratio
0	1	0	0.85 times the Initial Resistance Ratio
0	1	1	1.15 times the Initial Resistance Ratio
1	0	0	1.3 times the Initial Resistance Ratio
1	0	1	Code Prohibited
1	1	0	Code Prohibited
1	1	1	Code Prohibited

8.2.20 Extended Power Control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	BF1	BF0	HPM	DIS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: During a reset: {HPM, DIS} = 0H, {BF1, BF0}= 0H; read address: EH

- ✧ DIS
  The DIS register can control capacitors discharge that are connected between the power supply V0-V4 for LCD driver voltage and VSS.
  When using this register, refer to 7-30 (Discharge circuit).
  DIS = "0": Discharge OFF
  DIS = "1": Discharge start

- ✧ HPM
  The HPM register is the power control for the liquid crystal driver power supply circuit.
  HPM= "H": High power mode
  HPM= "L": Normal mode

✧ BF

BF1~BF0: Select the booster operating frequency. When the boosting frequency is high, the driving ability of the booster becomes high, but the current consumption is increased. When adjusting the boosting frequency, consider the external capacitors and the current consumption.

BF1	BF0	Booster Operating Clock Frequency
0	0	1.5kHz × 8
0	1	1.5kHz × 4
1	0	1.5kHz × 2
1	1	1.5kHz

8.2.21 Internal Register Read Address

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	RA3	RA2	RA1	RA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

Note: During a reset: {RA3, RA2, RA1, RA0} = BH

The RA register is set to specify the address for the register read operation. The EM65571 has many registers, including a register bank. There are 4 steps necessary to read a specific register.

1. Write 04H to the RE register to access the RA register.
2. Write a specific register address to the RA register.
3. Write a specific register bank to the RE register.
4. Read the specific contents.

8.2.22 Internal Register Data Read

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	Internal Register Read Data			

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

Note: The asterisk "*" mark means "Don't care"

This command is used to read data from an internal register. Before executing the command, you need to set the address and RE flag to read data from the internal register.

8.2.23 Windows End X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	EX3	EX2	EX1	EX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {EX3, EX2, EX1, EX0} = 0H, read address: 0H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	EX7	EX6	EX5	EX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {EX7, EX6, EX5, EX4} = 0H, read address: 1H)
The asterisk "*" mark means "Don't care"

Set the EX registers to the X-direction end address for Windows function.

8.2.24 Windows End Y Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	EY3	EY2	EY1	EY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {EY3, EY2, EY1, EY0} = 0H, read address: 2H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	EY7	EY6	EY5	EY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {EY7, EY6, EY5, EY4} = 0H, read address: 3H
The asterisk "*" mark means "Don't care"

Set the EY registers to the Y-direction end address for Windows function.

8.2.25 Line Reverse Start Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LS3	LS2	LS1	LS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {LS3, LS2, LS1, LS0} = 0H, read address: 4H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	LS7	LS6	LS5	LS4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {LS7, LS6, LS5, LS4} = 0H, read address: 5H
The asterisk "*" mark means "Don't care"

Set the LS registers to line reverse start address, then the following two conditions must be kept.

1. 00H ≤ LS ≤ 7FH
2. LS ≤ LE LE: Line reverse end address

8.2.26 Line Reverse End Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	LE3	LE2	LE1	LE0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(During a reset: {LE3, LE2, LE1, LE0} = 0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	LE7	LE6	LE5	LE4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(During a reset: {LE7, LE6, LE5, LE4} = 0H, read address: 7H)

Set the LE registers to line reverse end address, then the following two conditions must be kept.

1. 00H ≤ LS ≤ 7FH
2. LS ≤ LE LS: Line reverse start address

8.2.27 Line Reverse Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	BST	BT	LREV

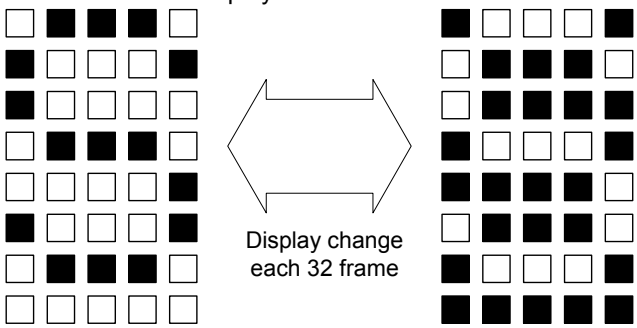
CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {BST, BT, LREV} = 0H, read address: 8H
The asterisk "*" mark means "Don't care"

- ✧ BST
  The BST register controls the Fast Burst RAM write function
  BST = "0": Burst RAM write function OFF
  BST = "1": Burst RAM write function ON

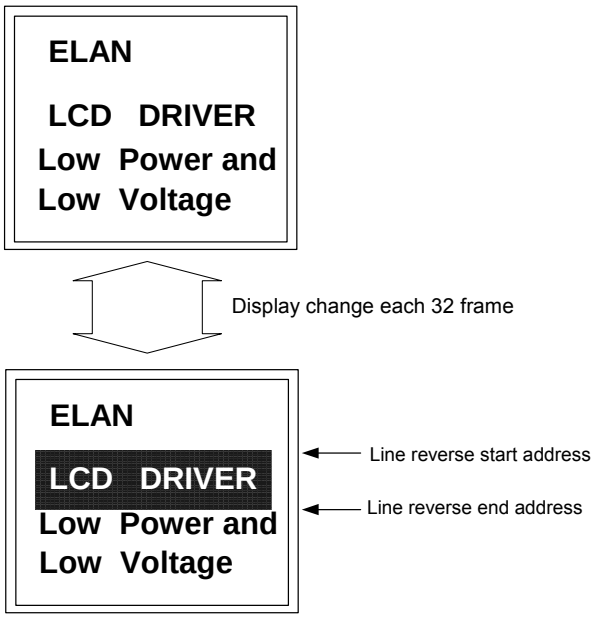
- ✧ LREV
  The LREV registers control line reverse display function.
  LREV = "0": Normal display (Not reverse).
  LREV = "1": Line reverse display enable.
  The area specified by the Line Reverse Start/End Register reverse display.
  The reverse type is selectable by BT register.
  When using the Line Reverse Display function, the LS and LE registers must keep the following relation: LS ≤ LE

- ✧ BT
  The BT register controls the line reverse type. This is an option for the line reverse display function.
  This BTs setting is only available when LREV="1"
  BT = "0": Reverse display
  BT = "1": Reverse display for each 32 frame.



Blink example (LREV = "1", BT = "1")

The LREV and BT setting don't influence the special segment outputs. The display area selected by COMA and COMB common outputs are also not influenced.



Blink example (LREV = "1", BT = "1")

8.2.28 Regulator Multiple Ratio Control Register

The V0 steps set to RM register.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	RM2	RM1	RM0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Note: During a reset: {RM2, RM1, RM0} = 0H, read address: 9H
The asterisk "*"mark means "Don't care"

The booster steps set to RM register.

RM2	RM1	RM0	Regulator Multiple Ratio Control
0	0	0	3.0 times the Voltage Output
0	0	1	4.5 times the Voltage Output
0	1	0	6.0 times the Voltage Output
0	1	1	7.5 times the Voltage Output
1	0	0	8.0 times the Voltage Output
1	0	1	8.5 times the Voltage Output
1	1	0	8.9 times the Voltage Output
1	1	1	9.5 times the Voltage Output

8.2.29 EEPROM Mode Select Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	M1	M0	VPP_EXT	OSC

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {M1, M0, VPP_EXT, OSC} = CH, read address: AH

The (M1, M0) register control EEPROM mode

(M1, M0)	EEPROM Operating Mode
00	Read
01	Program
10	Erase
11	Reserve

The VPP_EXT register controls the EEPROM power selection.
VPP_EXT=0 → Program or Erase EEPROM voltage is from an internal power source.
VPP_EXT=1 → Program or Erase EEPROM voltage is from an external power source. 16~18V is from an external VPP pin.
The OSC register controls the oscillator frequency selection.
OSC=0 → Initial oscillator frequency setting
OSC=1 → Oscillator frequency + 50%

8.2.30 Vop Calibration Offset Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	CV4	CV3	CV2	CV1

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

Note: During a reset: {CV4, CV3, CV2, CV1} = 0H, read address: BH)

The CV4~CV1 register controls the Vop calibration offset voltage selection.

$$VBA = \left[1 + \frac{M + Offset}{381}\right] \times VREF$$

where M: DV register setting

Offset: CV1~CV4 setting

CV4-CV1	Calibration Offset
0111	+7
0110	+6
…	…
0000	0
1000	-8
1001	-7
…	…
1111	-1

9 Relationship between Setting and Common/Display RAM

The relationship between the COM pin numbers and the addresses in the Y-direction on the display RAM changes according to the SHIFT command, LCD Duty Set command, Display Starting Common Position Set command, and Display Starting Line Set command.

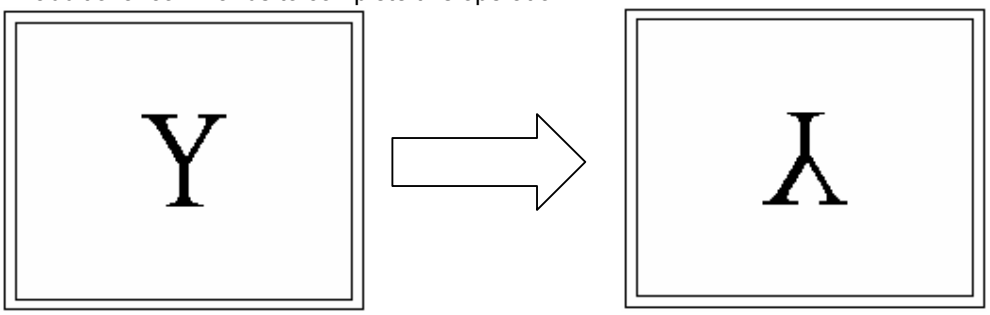
When “0” is selected for the display starting line:

The relationship between the COM pin and the addresses in the vertical direction of the display RAM (hereafter called MY) changes on a 15-dot basis according to the LCD Duty Set command and the Display Starting Common Position Set command. The common positions change in the forward direction when the SHIFT bit is “0”, and change in the reverse direction when the SHIFT bit is “1”. When “0” is selected as the value for LA7 to LA0 in the Display Starting Line Set command, the MY number corresponding to the display starting position is “0”. The MY numbers are sequentially shifted backward when display occurs. In any case, the relations of COMA = MY160 and COMB = MY161 do not change.

When non-zero is selected for the display starting line:

The relationship between the COM pins and the addresses in the vertical direction on the display RAM MY changes on a 15-dot basis according to the information in the LCD Duty Set command and Display Starting Common Position Set command. The common positions change in the forward direction when the SHIFT bit is “0”, and change in the reverse direction when the SHIFT bit is “1”. If non-zero is selected for the values for LA7 to LA0 in the Display Starting Line set command. The MY number corresponding to the display starting position shifts with the set value. The MY number shifts backward when display occurs. If it exceeds 159, it returns to 0, and then shifts sequentially. In any case, the relations of COMA = MY160 and COMB = MY161 do not change.

When you want a mirror image in the Y-direction like the following figure, you must set additional commands to complete this operation:




```
WRITE 0xF0  //bank 0
WRITE 0x8D  //shift=1 ; 65k color ; display on
WRITE 0x22  //Y address=2
WRITE 0xF4  //bank 4
WRITE 0x63  //SC=0011
```

10 Absolute Maximum Ratings

10.1 Absolute Maximum Ratings

Item	Symbol	Condition	Pin Used	Rating	Unit
Supply Voltage (1)	VDD	Ta=25	VDD	-0.3 ~ + 4.0	V
Supply Voltage (2)	VEE		VEE	-0.3 ~ + 4.0	V
Supply Voltage (3)	VOUT		VOUT	--0.3 ~ + 20.0	V
Supply Voltage (4)	VBA		VBA	1.5 ~ + 2.0	V
Supply Voltage (5)	V0		V0	-0.3 ~ + 18.0	V
Supply Voltage (6)	V1, V2, V3, V4		V1, V2, V3, V4	-0.3 ~ V0+ 0.3	V
Input Voltage	VI		*1	-0.3 ~ VDD+ 0.3	V
Storage Temperature	Tstg			-45 ~ +125	

10.2 Recommended Operating Conditions

Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Note
Supply Voltage	VDD1	VDD	2.2		3.3	V	*1
	VDD2	VDD	2.4		3.3	V	*2
	VEE	VEE	2.4		3.3	V	*3
Operating Voltage	V0	V0	5		18	V	*4
	VOUT	VOUT			20	V	*5
	VBA	VBA	1.5		2.0	V	
	VREF	VREF		1.5		V	
Operating Temperature	Topr		-30		85		

- Power supply for logic circuit.
- Power supply for analog circuit.
- Power supply for the internal boosting circuit. If applied voltage is the same as VDD, connect to VDD.
- Voltage V0>V1>V2>V3>V4>VSS must always be maintained.
- Voltage VOUT > V0 must always be maintained.

11 DC Characteristics

VSS=0V, VDD = 2.2 ~3.3V, Ta = -30 ~85°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
High level input voltage	VIH			0.8VDD	0.9VDD	VDD	V	1
Low level input voltage	VIL			0	0.1VDD	0.2VDD	V	1
High level output current	IOH1	VOH = VDD-0.4V		-2.7	-3.2	-3.5	mA	2
Low level output current	IOL1	VOL= 0.4V		2.7	3.2	3.5	mA	2
High level output current	IOH2	VOH = VDD-0.4V		-0.8	-1.0	-1.2	mA	3
Low level output current	IOL2	VOL= 0.4V		0.8	1.0	1.2	mA	3
Input leakage current	ILI1	VI = VSS or VDD		-2	0	2	µA	4
Output leakage current	ILO	VI = VSS or VDD		-2	0	2	µA	5
LCD driver output resistance	RON	Δ |Von| = 0.5V	V0=10V	1.0	1.3	1.6	KΩ	6
			V0=6V	1.2	1.7	2.2		
Standby current through VDD pin	ISTB	CK=0, CSB=VDD, Ta=25 , VDD=3V			5	15	µA	7
Oscillator frequency (variable gradation mode, 65K or 4096 or 256 color mode)	$Fosc_1$	VDD=3V , Ta=25 , Rf setting = (Rf2, Rf1, Rf0) = (000)		854	1005	1155	kHz	8
Oscillator frequency (48 gradation mode)	$Fosc_2$	VDD=3V, Ta=25 , Rf setting = (Rf2, Rf1, Rf0) = (000)		602	720	827	kHz	9
Oscillator frequency (16 gradation mode)	$Fosc_3$	VDD=3V, Ta=25 , Rf setting = (Rf2, Rf1, Rf0) = (000)		296	360	413	kHz	10
Oscillator frequency (8 gradation mode)	$Fosc_4$	VDD=3V , Ta=25 , Rf setting = (Rf2, Rf1, Rf0) = (000)		148	180	211	kHz	11

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Booster output Voltage on VOUT pin	VOUT1	Seven times boosting RL = 500KΩ (VOUT-VSS)	7×VEE×0.95 (VEE<=2.8)	7×VEE×0.98 (VEE<=2.8)	7×VEE×0.99 (VEE<=2.8)	V	12
	VOUT2	Six times boosting RL = 500KΩ (VOUT-VSS)	6×VEE×0.95	6×VEE×0.98	6×VEE×0.99	V	13
	VOUT3	Five times boosting RL = 500KΩ (VOUT-VSS)	5×VEE×0.95	5×VEE×0.98	5×VEE×0.99	V	14
	VOUT4	Four times boosting RL = 500KΩ (VOUT-VSS)	4×VEE×0.95	4×VEE ×0.98	4×VEE×0.99	V	15
	VOUT5	Three times boosting RL = 500KΩ (VOUT-VSS)	3×VEE×0.95	3×VEE×0.98	3×VEE×0.99	V	16
	VOUT6	Two times boosting RL = 500KΩ (VOUT-VSS)	2×VEE×0.95	2×VEE×0.98	2×VEE×0.99	V	17
Current consumption	IDD1	VDD = 3V, 6 times boosting, All ON pattern		600		μA	18
	IDD2	VDD = 3V, 6 times boosting, Check pattern		800		μA	19
VBA output voltage	VBA	VDD =2.4V~3.3V	1.5		2.0	V	20
VREF output voltage	VREF	VDD = 2.4 ~ 3.3V		1.5			21
V0 output voltage	V0	VDD = 2.4 ~ 3.3V	0.99×V0	V0	1.01×V0	V	

Relationship between the oscillating frequency (fosc) and external clock frequency (fCK) to the LCD frame frequency (fFLM) in each display mode

Original Oscillating Clock	Display Mode	Ratio of Display Duty Cycle (1/D)			
		1/130 to 1/98	1/82 to 1/50	1/34 to 1/26	1/18 to 1/10
When using a built-in oscillating circuit (fosc)	Variable gradation	fosc / (2×47×D)	fosc / (4×47×D)	fosc / (8×47×D)	fosc / (16×47×D)
	Simple gradation (65K color)	fosc / (2×31×D)	fosc / (4×31×D)	fosc / (8×31×D)	fosc / (16×31×D)
	Simple gradation (4096 color)	fosc / (2×15×D)	fosc / (4×15×D)	fosc / (8×15×D)	fosc / (16×15×D)
	Simple gradation (256 color)	fosc / (2×7×D)	fosc / (4×7×D)	fosc / (8×7×D)	fosc / (16×7×D)
When using an external clock from the CK pin. (fCK)	Variable gradation	fCK / (2×47×D)	fCK / (4×47×D)	fCK / (8×47×D)	fCK / (16×47×D)
	Simple gradation (65K color)	fCK / (2×31×D)	fCK / (4×31×D)	fCK / (8×31×D)	fCK / (16×31×D)
	Simple gradation (4096 color)	fCK / (2×15×D)	fCK / (4×15×D)	fCK / (8×15×D)	fCK / (16×15×D)
	Simple gradation (256 color)	fCK / (2×7×D)	fCK / (4×7×D)	fCK /(8×7×D)	fCK / (16×7×D)

- D0-D15, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins
- D0~D15 pins
- CLK pins
- CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins
- Applied when D0~D15 are in the state of high impedance.
- SEGA0~SEGA127, SEGB0~SEGB127, SEGC0~SEGC127. DSEGA0~DSEGA1, DSEGB0~DSEGB0 , DSEGC0~DSEGC1, COM0~COM79, COMA, COMB pins Resistance when applied with 0.5V between each output pin and each power supply (V0, V1, V2, V3, V4), and when applied with 1/13 bias.
- VDD pin. VDD pin current without load when the original oscillating clock stopped and at non-select (CSB=VDD)
- Oscillating frequency. When using a built-in oscillating circuit (variable gradation display mode 65K, 4096 or 256 color mode)
- Oscillating frequency. When a built-in oscillating circuit is used (48 gradation fixed display mode)
- Oscillating frequency. When a built-in oscillating circuit is used (16 gradation fixed display mode)
- Oscillating frequency. When a built-in oscillating circuit is used (8 gradation fixed display mode)
- VOUT pin. When the built-in oscillating circuit, built-in power supply, and boosting 7 times are used, this pin is applied. VEE ≤ 2.8 V. The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/13, 1/128 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”
- VOUT pin. When the built-in oscillating circuit, built-in power supply, and boosting 6 times are used, this pin is applied. VEE = 2.4 ~ 3.3. The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/13, 1/128 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”
- VOUT pin. When the built-in oscillating circuit, built-in power supply, and boosting 5 times are used, this pin is applied. VEE=2.4~3.3 V. The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/13, 1/128 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”
- VOUT pin. When the built-in oscillating circuit, built-in power supply, and boosting 4 times are used, this pin is applied. VEE=2.4~3.3 V. The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/13, 1/128 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”
- VOUT pin. When the built-in oscillating circuit, built-in power supply is used, and boosting 3 times are used, this pin is applied. VEE=2.4~3.3 V. The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/13, 1/128 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”
- VOUT pin. When the built-in oscillating circuit, built-in power supply, and boosting 2 times are used, this pin is applied. VEE=2.4~3.3 V. The electronic control is preset (The code is

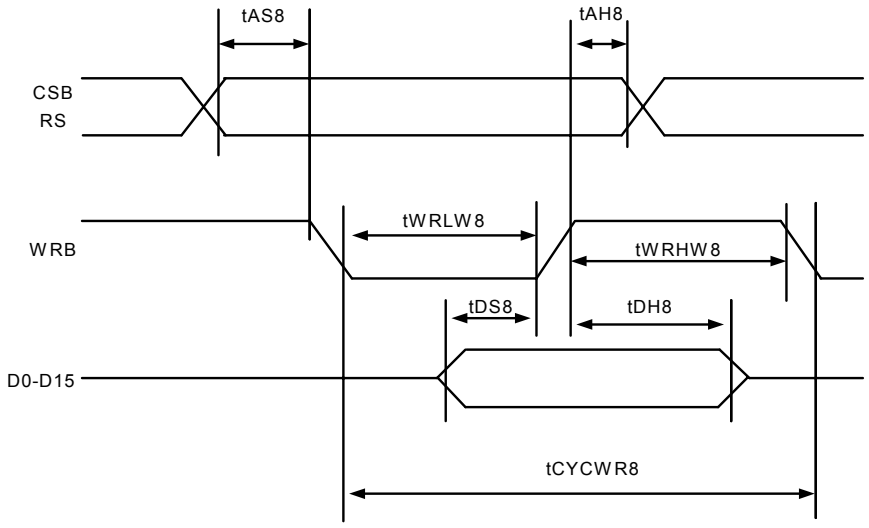
("1 1 1 1 1 1 1")). Measuring conditions: bias=1/5~1/13, 1/128 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1", BF="11"

- VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from the MPU, this pin is applied. Boosting 6 times is used when the electronic control is preset. (The code is ("1 1 1 1 1 1 1"). Display ALL ON pattern {Rf2, Rf1, Rf0 = ("0 0 0 ") } (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE , VBA=VREF, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1" , NLIN="0", (BF1, BF0) = (1,1), 1/128 duty, 1/13 bias, BF="11"
- VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from the MPU, this pin is applied. Boosting 6 times is used when the electronic control is preset. (The code is ("1 1 1 1 1 1 1"). Display a checkered pattern, {Rf2, Rf1, Rf0 = ("0 0 0 ") } (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1" , NLIN="0" ,(BF1,BF0)=(1,1) ,1/128 duty , 1/13 bias, BF="11"
- VBA pin. Measuring conditions: N times boosting (N=2~7), electronic control= "1 1 1 1 1 1 1", Displays a checkered pattern , DCON=AMPON="1" , NLIN="0" , 1/128 duty , VDD=VEE, VBA=VREF , C1=C2=1.0μF, C3=0.1μF , no load
- VREF pin. Measuring conditions: VDD = 3 volt, N times boosting (N=2 ~ 7), electronic control = "1 1 1 1 1 1 1", DCON=AMPON="1", NLIN="0", 1/128 duty.

Note: The capacitor C1 is used for booster related pin.
CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP1- , CAP4+ , CAP2- , CAP5+, CAP1-, CAP6+, CAP1- and VOUT, VSS
The capacitor C2 is used for bias related pin.
V0, V1, V2, V3, V4

12 AC Characteristic

12.1 80-family MPU Write Timing



VSS = 0V, VDD = 2.7~3.3V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in write	tCYCWR8		200			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		30			ns	
Write pulse “H” width	tWRHW8		135			ns	
Data setup time	tDS8		60			ns	D0~D15
Data hold time	tDH8		5			ns	

VSS = 0V, VDD = 2.4~2.7V, Ta = -30 ~ +85°C

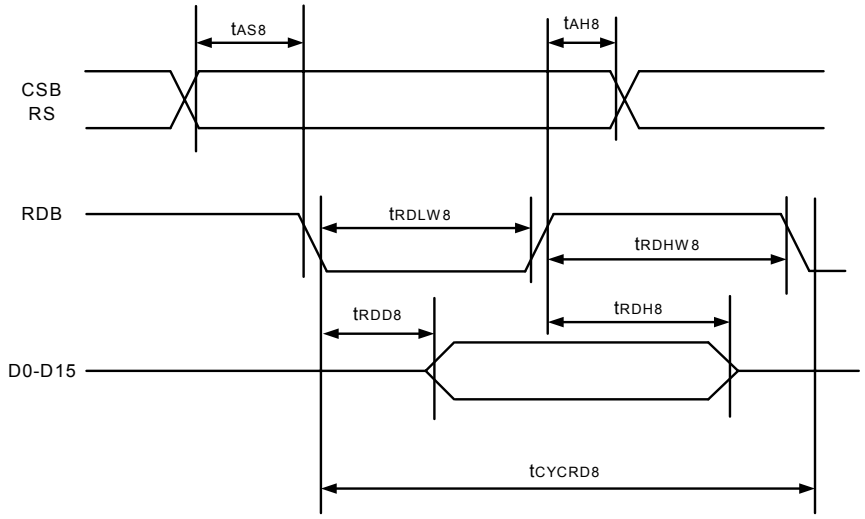
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in write	tCYCWR8		250			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		50			ns	
Write pulse “H” width	tWRHW8		160			ns	
Data setup time	tDS8		80			ns	D0~D15
Data hold time	tDH8		10			ns	

VSS = 0V, VDD = 2.2~2.4V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in write	tCYCWR8		500			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		100			ns	
Write pulse “H” width	tWRHW8		350			ns	
Data setup time	tDS8		100			ns	D0~D15
Data hold time	tDH8		20			ns	

Note: All the timings must be specified relative to 20% and 80% of the VDD voltage.

12.2 80-Family MPU Read Timing



VSS = 0V, VDD = 2.7~3.3V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in read	tCYCRD8		380			ns	RDB (E)
Read pulse “L” width	tRDLW8		200			ns	
Read pulse “H” width	tRDHW8		170			ns	
Data setup time	tRDD8	CL = 80 pF			210	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS = 0V, VDD = 2.4~2.7V, Ta = -30 ~ +85°C

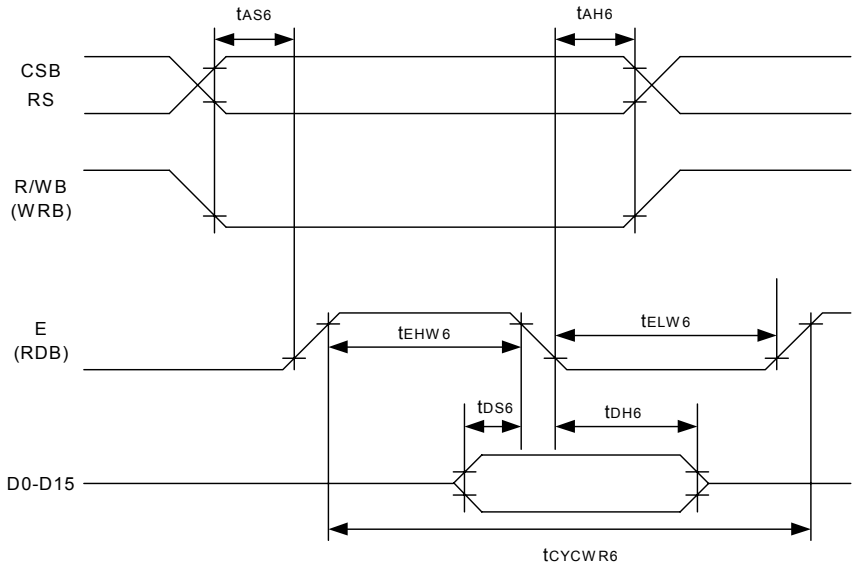
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in read	tCYCRD8		540			ns	RDB(E)
Read pulse “L” width	tRDLW8		290			ns	
Read pulse “H” width	tRDHW8		230			ns	
Data setup time	tRDD8	CL = 80 pF			300	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS = 0V, VDD = 2.2~2.4V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
System cycle time in read	tCYCRD8		840			ns	RDB(E)
Read pulse “L” width	tRDLW8		440			ns	
Read pulse “H” width	tRDHW8		380			ns	
Data setup time	tRDD8	CL = 80 pF			450	ns	D0~D15
Data hold time	tRDH8		10			ns	

Note: All the timings must be specified relative to 20% and 80% of the VDD voltage.

12.3 68-Family MPU Write Timing



VSS = 0V, VDD = 2.7 ~3.3V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCWR6		200			ns	RDB(E)
Write pulse “L” width	tELW6		30			ns	
Write pulse “H” width	tEHW6		135			ns	
Data setup time	tDS6		60			ns	D0~D15
Data hold time	tDH6		5			ns	

VSS=0V, VDD = 2.4 ~2.7V, Ta = -30 ~ +85°C

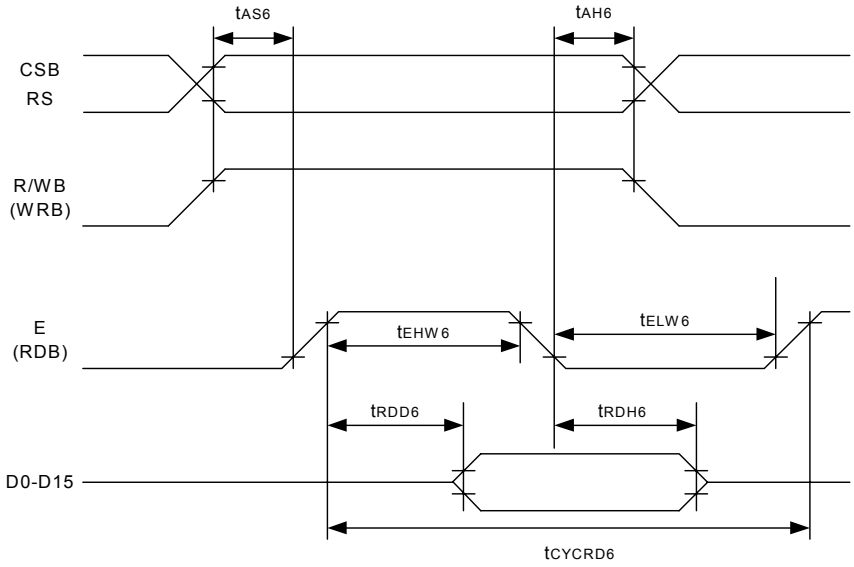
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCWR6		250			ns	RDB(E)
Write pulse “L” width	tELW6		50			ns	
Write pulse “H” width	tEHW6		160			ns	
Data setup time	tDS6		80			ns	D0~D15
Data hold time	tDH6		10			ns	

VSS = 0V, VDD = 2.2 ~2.4V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in write	tCYCWR6		500			ns	RDB(E)
Write pulse “L” width	tELW6		100			ns	
Write pulse “H” width	tEHW6		350			ns	
Data setup time	tDS6		100			ns	D0~D15
Data hold time	tDH6		20			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

12.4 68-Family MPU Read Timing



VSS = 0V, VDD = 2.7~3.3V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in read	tCYCRD6		380			ns	RDB(E)
Write pulse “L” width	tELW6		200			ns	
Write pulse “H” width	tEHW6		170			ns	
Data setup time	tRDD6	CL=50pF			210	ns	D0~D15
Data hold time	tRDH6		10			ns	

VSS = 0V, VDD = 2.4~2.7V, Ta = -30 ~ +85°C

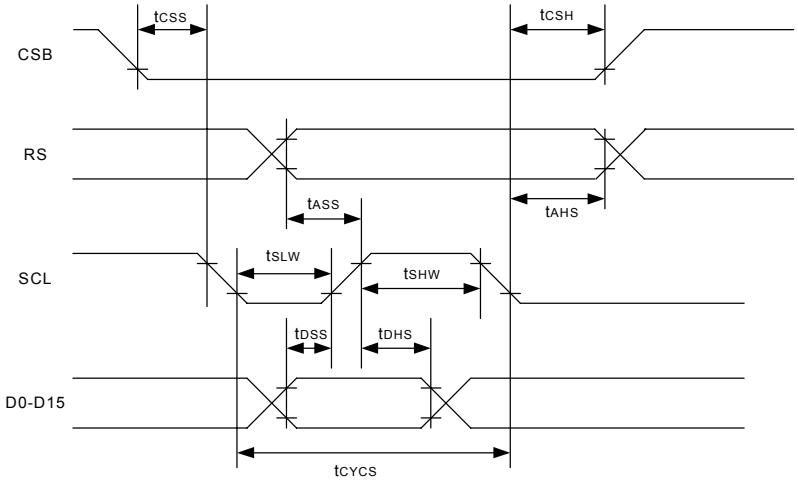
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in read	tCYCRD6		540			ns	RDB(E)
Write pulse “L” width	tELW6		290			ns	
Write pulse “H” width	tEHW6		230			ns	
Data setup time	tRDD6	CL=50pF			300	ns	D0~D15
Data hold time	tRDH6		10			ns	

14.4.3VSS = 0V, VDD = 2.2~2.4V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
System cycle time in read	tCYCRD6		1000			ns	RDB(E)
Write pulse “L” width	tELW6		450			ns	
Write pulse “H” width	tEHW6		500			ns	
Data setup time	tRDD6	CL=50pF			650	ns	D0~D15
Data hold time	tRDH6		10			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

12.5 Serial Interface Timing Diagram



VSS = 0V, VDD = 2.7~3.3V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		40			ns	RS
Address hold time	tAHS		40			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		40			ns	CSB
CSB hold time	tCSH		40			ns	

VSS = 0V, VDD = 2.4~2.7V, Ta = -30 ~ +85°C

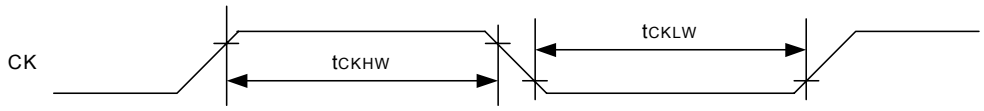
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		50			ns	RS
Address hold time	tAHS		50			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		50			ns	CSB
CSB hold time	tCSH		60			ns	

VSS = 0V, VDD = 2.2~2.4V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Serial clock period	tCYCS		230			ns	SCL
SCL pulse “H” width	tSHW		100			ns	
SCL pulse “L” width	tSLW		100			ns	
Address setup time	tASS		80			ns	RS
Address hold time	tAHS		80			ns	
Data setup time	tDSS		100			ns	SDA
Data hold time	tDHS		100			ns	
CSB-SCL time	tCSS		80			ns	CSB
CSB hold time	tCSH		100			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

12.6 Clock Input Timing



VSS = 0V, VDD = 2.4~3.3V, Ta = -30 ~ +85°C

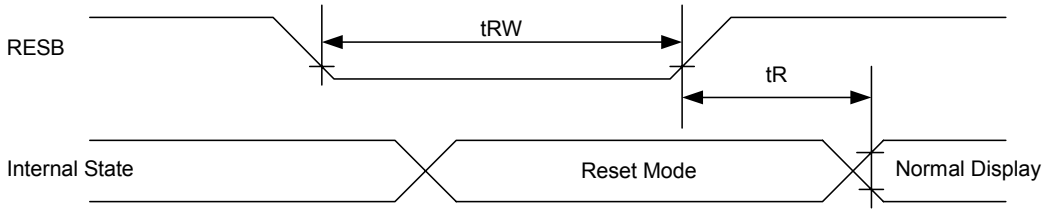
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
CK pulse “H” width (1)	tCKHW1		1.2		1.4	µs	CK 1
CK pulse “L” width (1)	tCKLW1		1.2		1.4	µs	
CK pulse “H” width (2)	tTCKHW2		5.4		6.5	µs	CK 2
CK pulse “L” width (2)	tCKLW2		5.4		6.5	µs	
CK pulse “H” width (3)	tCKHW3		3.8		4.5	µs	CK 3
CK pulse “L” width (3)	tCKLW3		3.8		4.5	µs	

VSS = 0V, VDD = 2.2~2.4V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
CK pulse “H” width (1)	tCKHW1	Note1	1.2		1.4	µs	CK [1]
CK pulse “L” width (1)	tCKLW1	Note1	1.2		1.4	µs	
CK pulse “H” width (2)	tCKHW2	Note2	5.4		6.5	µs	CK [2]
CK pulse “L” width (2)	tCKLW2	Note2	5.4		6.5	µs	
CK pulse “H” width (3)	tCKHW3	Note3	3.8		4.5	µs	CK [3]
CK pulse “L” width (3)	tCKLW3	Note3	3.8		4.5	µs	

Note: [1] Applied when the gradation display mode, 65K=”0”, PWM=”0”
[2] Applied when the simple gradation mode, 65K=”0”, PWM=”1”
[3] Applied when the monochrome mode, 65K=”1”

12.7 Reset Timing



VSS = 0V, VDD = 2.4~3.3V, Ta = -30 ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Reset time	tR				1	µs	
Reset pulse “L” width	tRW		10			µs	RESB

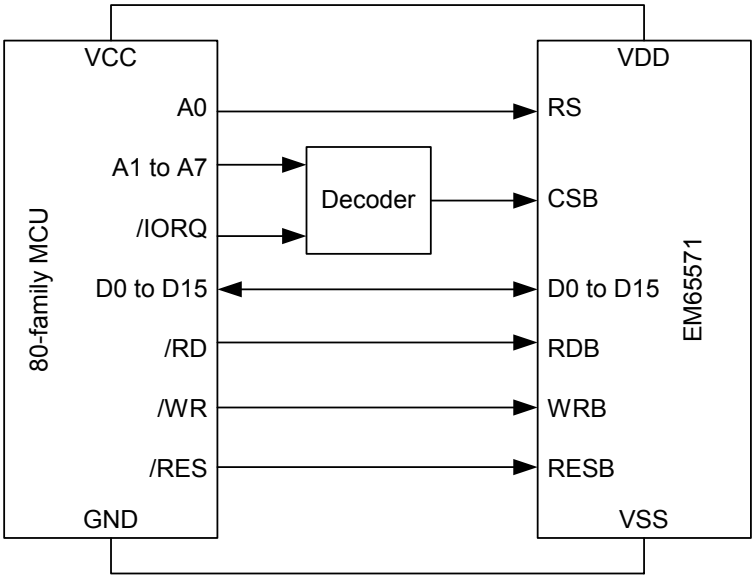
VSS = 0V, VDD = 2.2~2.4V, Ta = -30 ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Reset time	tR				1.5	µs	
Reset pulse “L” width	tRW		10			µs	RESB

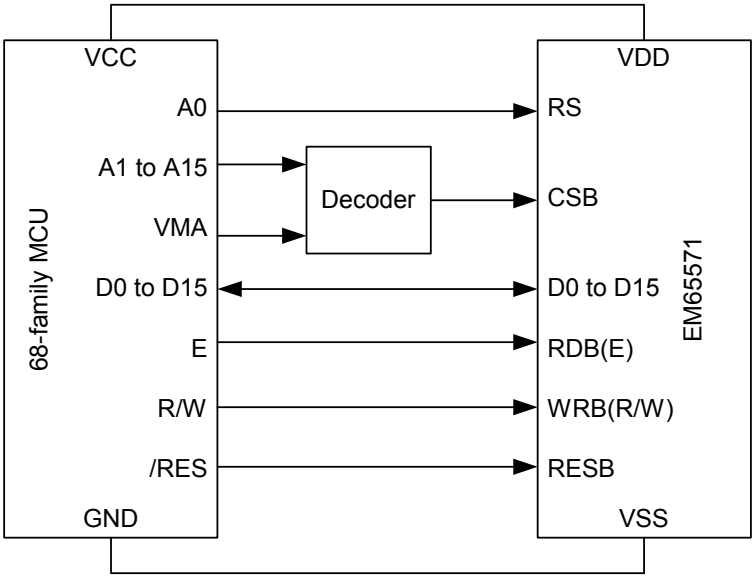
Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

13 Application Circuit

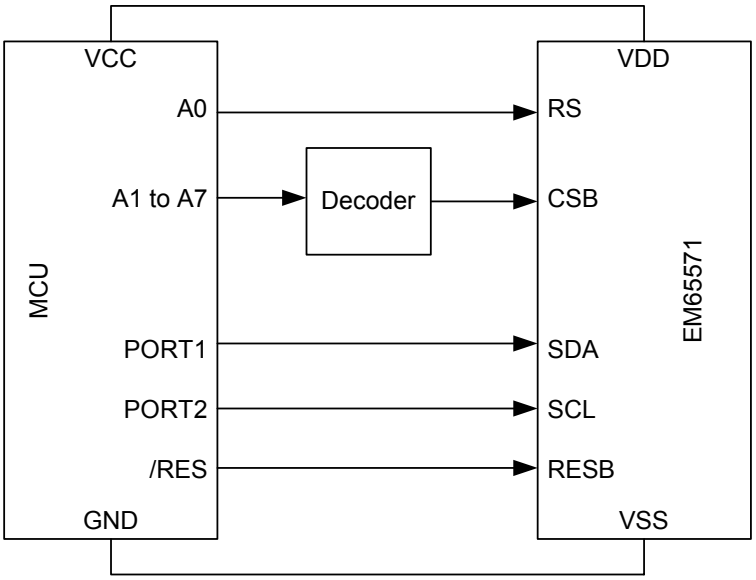
13.1 Connections of the 80-Family MPU



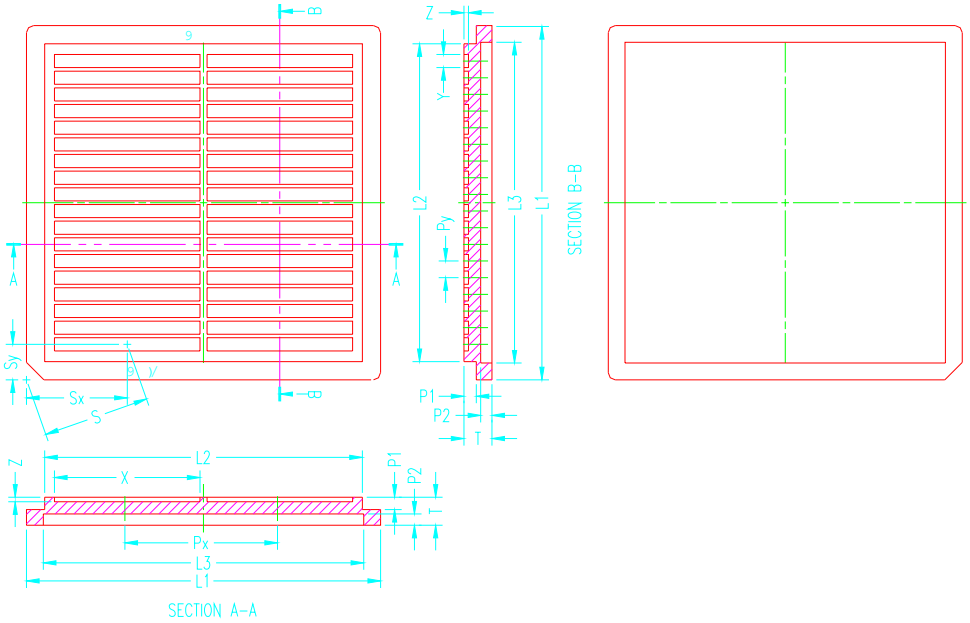
13.2 Connections of the 68-Family MPU



13.3 Connection of the MPU with Serial Interface



14 Tray Information



Tray Outline Dimension
Unit: mm

Symbol	Dimension	Symbol	Dimension
L1	50.60	Z	0.66
L2	45.40	Px	21.80
L3	45.80	Py	2.38
T	4.00	Nx	2
Sx	14.40	Ny	18
Sy	5.07	N	36
S	15.27	P1	1.76
X	20.80	P2	1.60
Y	1.88		