PN512

Transmission Module

Rev. 3.3 — 13 June 2007 **Product short data sheet**
124533

1. Introduction

This Product short data sheet describes the functionality of the transceiver IC PN512. It includes functional and electrical specifications. A complete specification is given in the product data sheet.

2. General description

The PN512 is a highly integrated transceiver IC for contactless communication at 13.56 MHz. This transceiver IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

The PN512 transceiver ICs support 4 different operating modes

- Reader/Writer mode supporting ISO 14443A/Mifare and FeliCa scheme
- Reader/Writer mode supporting ISO 14443B scheme
- Card Operation mode supporting ISO 14443A/Mifare and FeliCa scheme
- NFCIP-1 mode

Enabled in Reader/Writer mode for ISO 14443A/Mifare, the PN512's internal transmitter part is able to drive a reader / writer antenna designed to communicate with ISO 14443A/ Mifare cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO 14443A/Mifare compatible cards and transponders. The digital part handles the complete ISO 14443A framing and error detection (Parity & CRC).

The PN512 supports Mifare Classic (e.g. Mifare Standard) products. The PN512 supports contactless communication using Mifare higher transfer speeds up to 424 kbit/s in both directions.

Enabled in Reader/Writer mode for FeliCa, the PN512 transceiver IC supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The PN512 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The PN512 supports all layers of the ISO/IEC 14443B reader/writer communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardised protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443B anticollision are correctly implemented.

In Card Operation mode, the PN512 transceiver IC is able to answer to a reader/writer command either according to the FeliCa or ISO 14443A/Mifare card interface scheme. The PN512 generates the digital load modulated signals and in addition with an external circuit the answer can be sent back to the reader/writer. A complete card functionality is only possible in combination with a secure core IC using the S^2C interface.

Additionally, the PN512 transceiver IC offers the possibility to communicate directly to an NFCIP-1 device in the NFCIP-1 mode. The NFCIP-1 mode offers different communication mode and transfer speeds up to 424 kbit/s according to the Ecma 340 and ISO/IEC 18092 NFCIP-1 Standard. The digital part handles the complete NFCIP-1 framing and error detection.

Various host controller interfaces are implemented:

- 8-bit parallel interface[1]
- SPI interface
- serial UART (similar to RS232 with voltage levels according pad voltage supply)
- I^2C interface.

A purchaser of this NXP IC has to take care for appropriate third party patent licenses.

1. 8-bit parallel Interface only available in HVQFN40 package.

3. Features

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF Level detector
- Integrated data mode detector
- ISO 14443A/Mifare support
- ISO 14443B reader/writer support
- Typical operating distance in Reader/Writer mode for communication to a ISO 14443A/Mifare or FeliCa card up to 50 mm depending on the antenna size, tuning and power supply
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on the antenna size and tuning and power supply
- Typical operating distance in ISO 14443A/Mifare card or FeliCa Card Operation mode of about 100 mm depending on the antenna size and tuning and the external field strength
- Mifare Classic encryption in Reader/Writer mode support
- ISO 14443 higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Contactless communication according to the FeliCa scheme at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFCIP-1 up to 424 kbit/s
- S^2C interface
- Supported host controller interfaces
  - SPI interface up to 10 Mbit/s
  - I^2C interface up to 400 kbit/s in Fast mode, up to 3400 kbit/s in High-speed mode
  - serial UART in different transfer speeds up to 1228.8 kbit/s, framing according to the RS232 interface with voltage levels according pad voltage supply
  - 8-bit parallel interface with and without Address Latch Enable
- Comfortable 64 byte send and receive FIFO-buffer
- Flexible interrupt modes
- Hard reset with low power function
- Power-down mode per software
- Programmable timer
- Internal oscillator to connect 27.12 MHz quartz
- 2.5-3.6 V power supply
- CRC Co-processor
- Free programmable I/O pins
- Internal self test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AV_{DD}	Supply Voltage	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V,	[1][2]	2.5	-	3.6	V
DV_{DD}		$PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[1][2]				
TV_{DD}			[1][2]				
PV_{DD}	Pad power supply	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V, $PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[3]	1.6	-	3.6	V
SV_{DD}	S2C Pad Power Supply	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V,		1.6	-	3.6	V
I_{HPD}	Hard Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, N_{RESET} = LOW	[7]	-	-	5	µA
I_{SPD}	Soft Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, RF level detector on	[7]	-	-	10	µA
I_{DVDD}	Digital Supply Current	$DV_{DD} = 3$ V		-	6.5	9	mA
I_{AVDD}	Analog Supply Current	$AV_{DD} = 3$ V, bit RCVOff = 0		-	7	10	mA
$I_{AVDD,RCVOFF}$	Analog Supply Current, receiver switched off	$AV_{DD} = 3$ V, bit RCVOff = 1		-	3	5	mA
I_{PVDD}	Pad Supply Current		[5]	-	-	40	mA
I_{TVDD}	Transmitter Supply Current	Continuous Wave	[4][6][8]	-	60	100	mA
T_{amb}	operating ambient temperature			-30		+85	°C

[1] Supply voltage below 3 V reduces the performance (e.g. the achievable operating distance).

[2] AV_{DD}, DV_{DD} and TV_{DD} shall always be on the same voltage level.

[3] PV_{DD} shall always be on the same or lower voltage level than DV_{DD}.

[4] I_{TVDD} depends on TV_{DD} and the external circuitry connected to Tx1 and Tx2

[5] I_{PVDD} depends on the overall load at the digital pins.

[6] During operation with a typical circuitry the overall current is below 100 mA.

[7] I_{SPD} and I_{HPD} are the total currents over all supplies.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5120A0HN1/C1	HVQFN32	Plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617
PN5120A0HN/C1	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6× 6× 0.85 mm	SOT618

6. Block diagram

The Analog interface handles the modulation and demodulation of the analog signals according to the Card Receiving mode, Reader/Writer mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The Data mode detector detects a Mifare, FeliCa or NFCIP-1 mode in order to prepare the internal receiver to demodulate signals, which are sent to the PN512.

The communication (S^2C) interface provides digital signals to support communication for transfer speeds above 424 kbit/s and digital signals to communicate to a secure smart card IC.

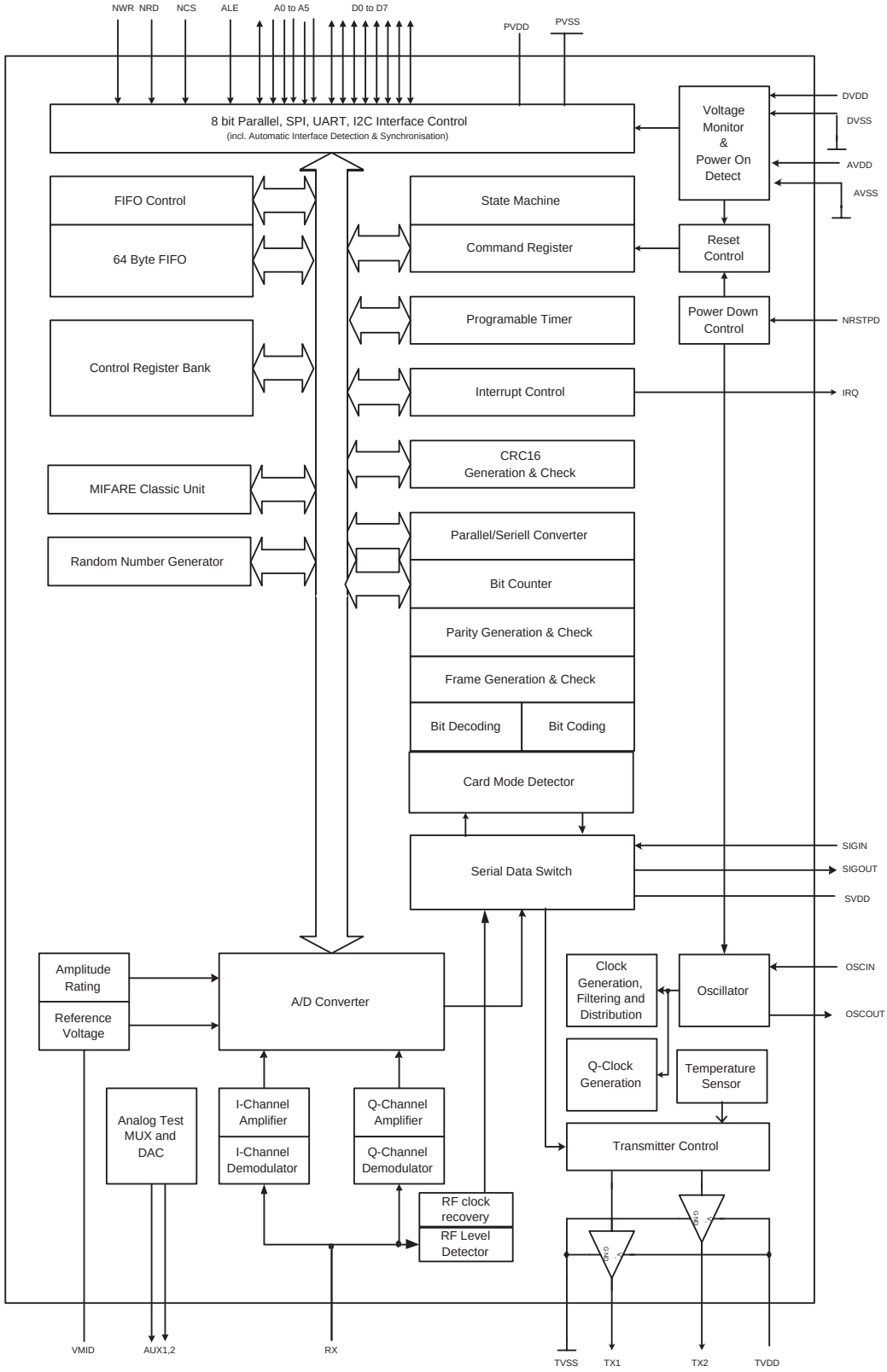
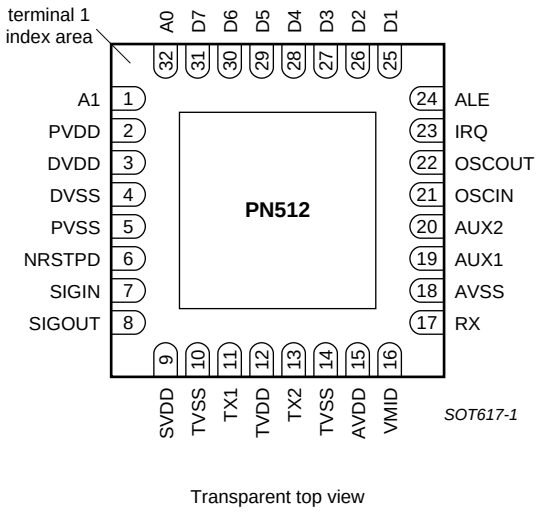


Fig 1. PN512 Block diagram

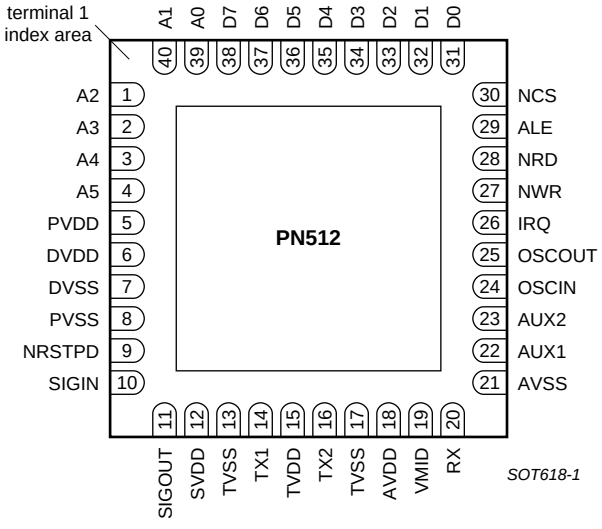
7. Pinning information

7.1 Pinning



Transparent top view

Fig 2. Pinning configuration HVQFN32 (SOT617-1)



Transparent top view

Fig 3. Pinning configuration HVQFN40 (SOT618)

7.2 Pin description

Table 3. Pin description HVQFN32

Symbol	Pin	Type	Description
A1	1	I	**Address Line**
PVDD	2	PWR	**Pad power supply**
DVDD	3	PWR	**Digital Power Supply**
DVSS	4	PWR	**Digital Ground**
PVSS	5	PWR	**Pad power supply ground**
NRSTPD	6	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
SIGIN	7	I	**Communication Interface Input:** accepts a digital, serial data stream
SIGOUT	8	O	**Communication Interface Output**: delivers a serial data stream
SVDD	9	PWR	**S^2C Pad Power Supply:** provides power to the S^2C pads
TVSS	10	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
TX1	11	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
TVDD	12	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
TX2	13	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
TVSS	14	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
AVDD	15	PWR	**Analog Power Supply**
VMID	16	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
RX	17	I	**Receiver Input**
AVSS	18	PWR	**Analog Ground**
AUX1	19	O	**Auxiliary Outputs:** These pins are used for testing.
AUX2	20	O	
OSCIN	21	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
OSCOUT	22	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
IRQ	23	O	**Interrupt Request:** output to signal an interrupt event
ALE	24	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
D1 to D7	25 to 31	I/O	**8-bit Bi-directional Data Bus.** **Remark:** An 8-bit parallel interface is not available. **Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address. **Remark:** For serial interfaces this pins can be used for test signals or I/Os.
A0	32	I	**Address Line**

Table 4. Pin description HVQFN40

Symbol	Pin	Type	Description
A2 to A5	1 to 4	I	**Address Line**
PVDD	5	PWR	**Pad power supply**
DVDD	6	PWR	**Digital Power Supply**
DVSS	7	PWR	**Digital Ground**
PVSS	8	PWR	**Pad power supply ground**
NRSTPD	9	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
SIGIN	10	I	**Communication Interface Input:** accepts a digital, serial data stream
SIGOUT	11	O	**Communication Interface Output**: delivers a serial data stream
SVDD	12	PWR	**S^2C Pad Power Supply:** provides power to the S^2C pads
TVSS	13	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
TX1	14	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
TVDD	15	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
TX2	16	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
TVSS	17	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
AVDD	18	PWR	**Analog Power Supply**
VMID	19	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
RX	20	I	**Receiver Input**
AVSS	21	PWR	**Analog Ground**
AUX1	22	O	**Auxiliary Outputs:** These pins are used for testing.
AUX2	23	O	
OSCIN	24	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
OSCOUT	25	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
IRQ	26	O	**Interrupt Request:** output to signal an interrupt event
NWR	27	I	**Not Write:** strobe to write data (applied on D0 to D7) into the PN512 register
NRD	28	I	**Not Read:** strobe to read data from the PN512 register (applied on D0 to D7)
ALE	29	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
NCS	30	I	**Not Chip Select:** selects and activates the host controller interface of the PN512
D0 to D7	31 to 38	I/O	**8-bit Bi-directional Data Bus.** **Remark:** For serial interfaces this pins can be used for test signals or I/Os. **Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address.
A0 to1 A1	39 to 40	I	**Address Line**

8. Operating modes

PN512 transceiver IC supports the following operating modes:

- Reader/Writer mode supporting ISO 14443A/Mifare, ISO 14443B & FeliCa scheme
- Card Operation mode supporting ISO 14443A/ Mifare and FeliCa scheme
- NFCIP-1 mode

The modes support different transfer speeds and modulation schemes. The following chapters will explain the different modes in detail.

Note: All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

8.1 Reader/Writer mode

Generally 3 Reader/Writer modes are supported. The PN512 can act as a reader/writer for ISO 14443A/Mifare, ISO 14443B or FeliCa cards.

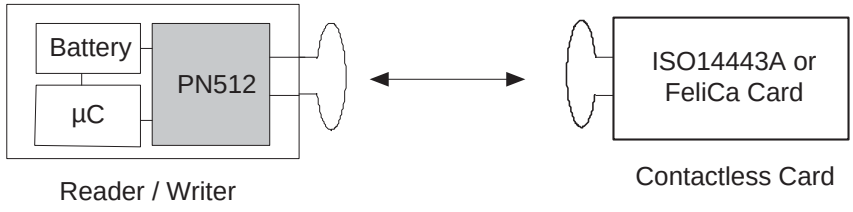


Fig 4. Reader/Writer mode

In the Reader/Writer mode the PN512 enables the communication to a contactless ISO 14443A/Mifare, ISO 14443B or FeliCa card.

8.1.1 ISO 14443A/Mifare reader/writer functionality

The ISO 14443A/Mifare Reader/Writer mode is the general reader to card communication scheme according to the ISO 14443A/Mifare specification.The following diagram describes the communication on a physical level, the communication table describes the physical parameters.

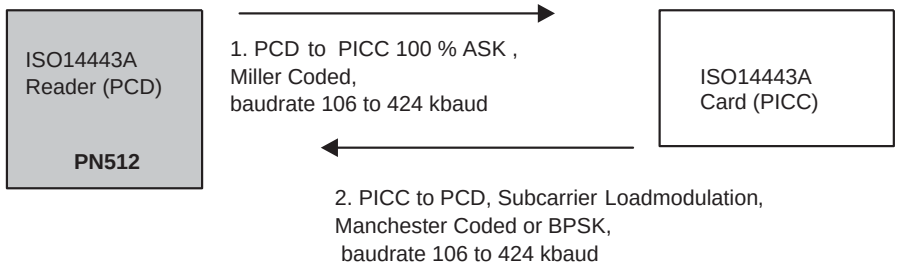


Fig 5. ISO 14443A/Mifare Reader/Writer mode communication diagram

Table 5. Communication overview for ISO 14443A/Mifare reader/writer

Communication direction		ISO 14443A/Mifare	Mifare Higher transfer speeds	
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
PN512 → PICC (send data from the PN512 to a card)	Modulation on reader side	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bitlength	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PICC → PN512 (receive data from a card)	modulation on card side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK

The contactless UART of PN512 and a dedicated external host controller are required to handle the complete Mifare/ISO 14443A/Mifare protocol.

8.1.1.1 Data Coding and framing according to ISO 14443A/Mifare

The internal CRC co-processor calculates the CRC value according to the definitions given in the ISO 14443A part 3 and handles parity generation internally according to the transfer speed.

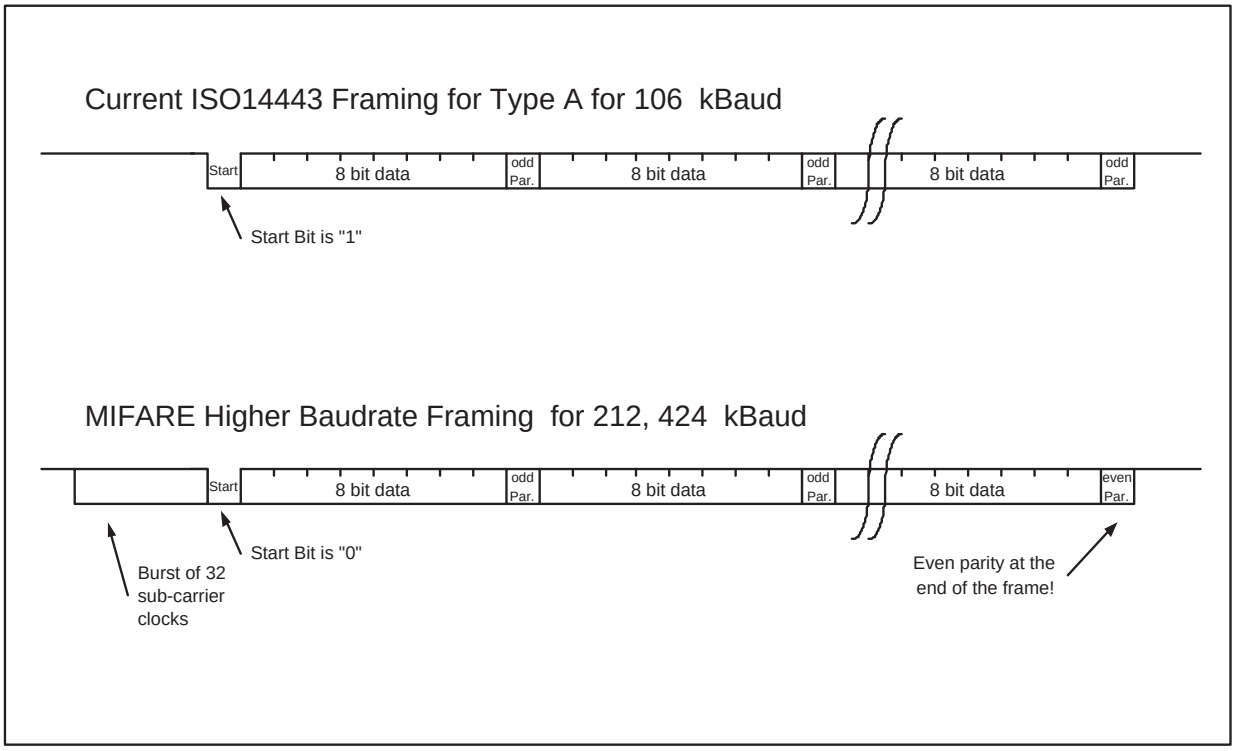


Fig 6. Data Coding and framing according to ISO 14443A

8.1.2 FeliCa reader/writer functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The following diagram describes the communication on a physical level, the communication overview describes the physical parameters.

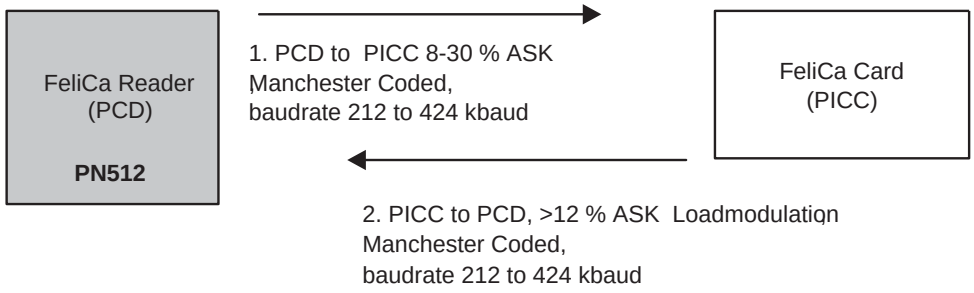


Fig 7. FeliCa reader/writer Communication Diagram

Table 6. Communication overview for FeliCa reader/writer

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
PN512 → card	Modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) µs	(32/13.56) µs
card → PN512	Loadmodulation on card side	>12% ASK	>12% ASK
	bit coding	Manchester coding	Manchester coding

The contactless UART of PN512 and a dedicated external host controller are required to handle the complete FeliCa protocol.

8.1.2.1 FeliCa framing and coding

Table 7. FeliCa framing and coding

Preamble						Sync		Len	n-Data	CRC
00h	00h	00h	00h	00h	00h	B2h	4Dh			

To enable the FeliCa communication a 6 byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2 bytes Sync bytes (B2h, 4Dh) are sent to synchronize the receiver.

The following Len byte indicates the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the host controller has to send the Len- and data-bytes to the PN512's FIFO buffer. The preamble and the sync bytes are generated by the PN512 automatically and must not be written to the FIFO by the host controller. The PN512 performs internally the CRC calculation and adds the result to the data frame.

Example for FeliCa CRC Calculation:

Table 8. Start Value for the CRC Polynomial: (00h), (00h)

Preamble						Sync		Len	2 Data Bytes		CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh	03h	ABh	CDh	90h	35h

8.1.3 ISO 14443B reader/writer functionality

The international standard ISO 14443 standard covers 2 communication schemes: the ISO 14443-A and the ISO 14443B.

The PN512 reader IC fully supports the ISO 14443.

The following registers and bits cover the ISO 14443B communication scheme:

As a reference documentation the international standard ISO 14443 'Identification cards- Contactless integrated circuit(s) cards- Proximity cards, part 1-4' can be taken.

Note: NXP Semiconductors does not offer a software library to design in the ISO 14443B protocol.

8.2 NFCIP-1 mode

The NFCIP-1 communication differentiates between an active and a Passive Communication mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.
- Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

In order to fully support the NFCIP-1 standard the PN512 supports the Active and Passive Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

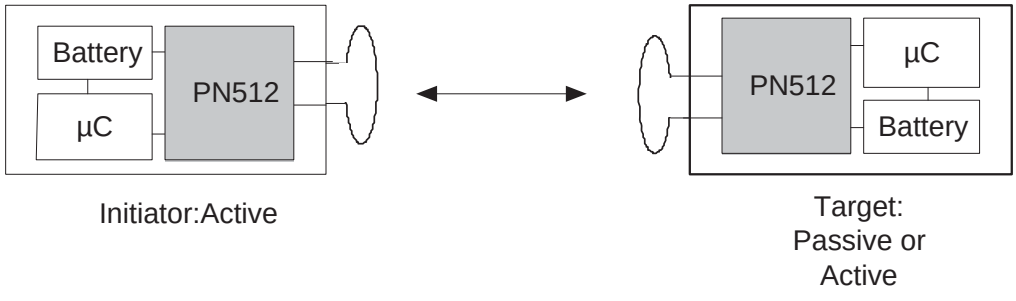


Fig 8. NFCIP-1 mode

8.2.1 Active Communication mode

Active Communication mode means both the initiator and the target are using their own RF field to transmit data.

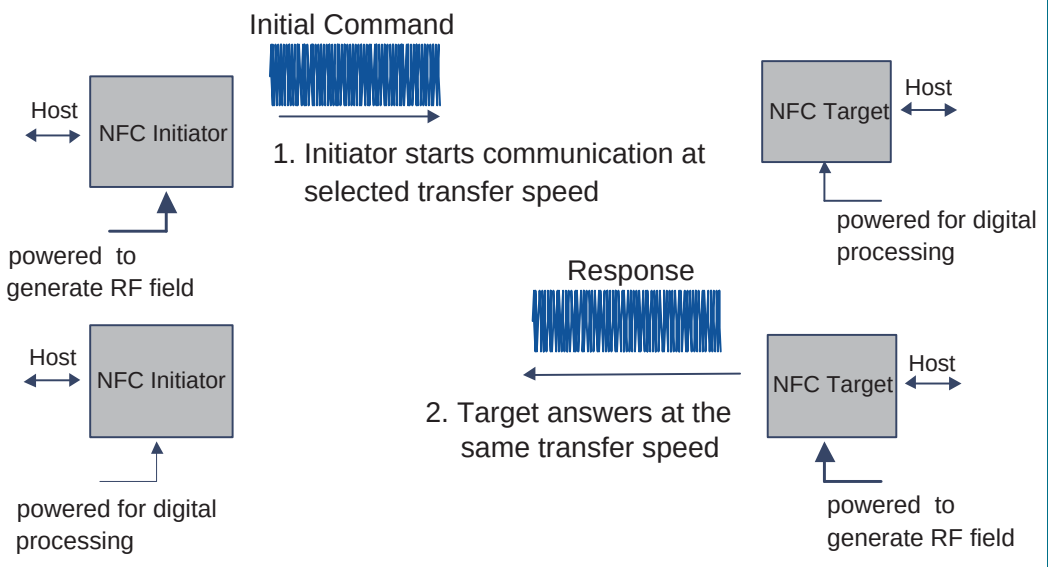


Fig 9. Active Communication mode

Table 9. Communication Overview for Active Communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator → Target	According to ISO 14443A 100% ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded		digital capability to handle this communication	
Target → Initiator					

The contactless UART of PN512 and a dedicated host controller are required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The PN512 supports these transfer speeds only with dedicated external circuits.

8.2.2 Passive Communication mode

Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

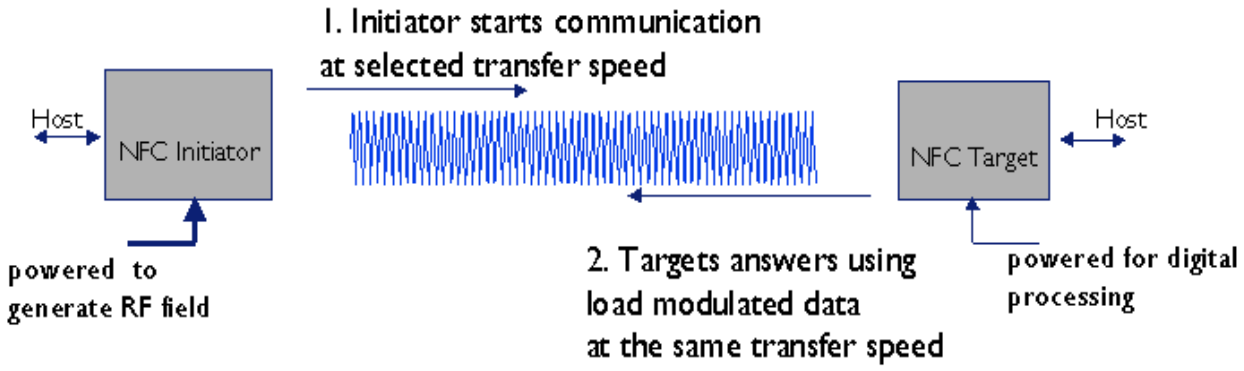


Fig 10. Passive Communication mode

Table 10. Communication Overview for Passive Communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator → Target	According to ISO 14443A 100% ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded		digital capability to handle this communication	
Target → Initiator	According to ISO 14443A subcarrier load modulation, Manchester Coded	According to FeliCa, >12% ASK Manchester Coded			

The contactless UART of PN512 and a dedicated host controller are required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The PN512 supports these transfer speeds only with dedicated external circuits.

8.2.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive Communication mode is defined in the NFCIP-1 standard.

Table 11. Framing and Coding Overview

Transfer speed	Framing and Coding
106 kbit/s	According to the ISO 14443A/Mifare scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

8.2.4 NFCIP-1 Protocol Support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the NFCIP-1 standard. However the datalink layer is according to the following policy:

- Speed shall not be changed while continuum data exchange in a transaction.
- Transaction includes initialization and anticollision methods and data exchange (in continuous way, meaning no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz general rules to start NFCIP-1 communication are defined in the following way.

1. Per default NFCIP-1 device is in Target mode meaning its RF field is switched off.
2. The RF level detector is active.
3. Only if application requires the NFCIP-1 device shall switch to Initiator mode.
4. Initiator shall only switch on its RF field if no external RF field is detected by RF Level detector during a time of TIDT.
5. The initiator performs initialization according to the selected mode.

8.3 Card Operation mode

The PN512 can be addressed like a FeliCa or ISO 14443A/Mifare card. This means that the PN512 can generate an answer in a load modulation scheme according to the ISO 14443A/Mifare or FeliCa interface description.

Note: The PN512 does not support a complete card protocol. This has to be handled by a dedicated card SAM or a host controller. The card-SAM is optional.

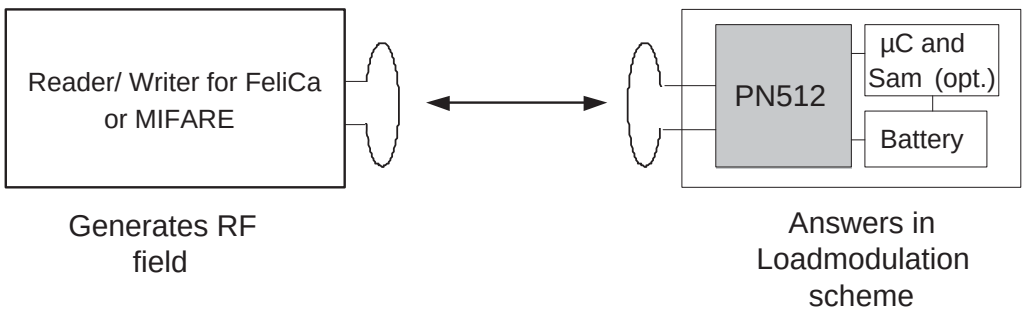


Fig 11. Card Operation mode

8.3.1 Mifare Card Operation mode

Table 12. Mifare Card Operation mode

Communication direction		ISO 14443A/Mifare	Mifare Higher transfer speeds	
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
reader / writer → PN512	Modulation on reader side	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
	Bitlength	(128/13.56) μs	(64/13.56) μs	(32/13.56) μs
PN512 → reader/ writer	Modulation on PN512 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK

8.3.2 FeliCa Card Operation mode

Table 13. FeliCa Card Operation Mode

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
reader/writer → PN512	Modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) μs	(32/13.56) μs
PN512 → reader/ writer	Load modulation on PN512 side	>12% ASK load modulation	>12% ASK load modulation
	bit coding	Manchester coding	Manchester coding

9. Application design-in information

The figure below shows a typical circuit diagram, using a complementary antenna connection to the PN512.

The antenna tuning and RF part matching is described in the application note PN512 transceiver IC; Antenna and RF Design Guide.

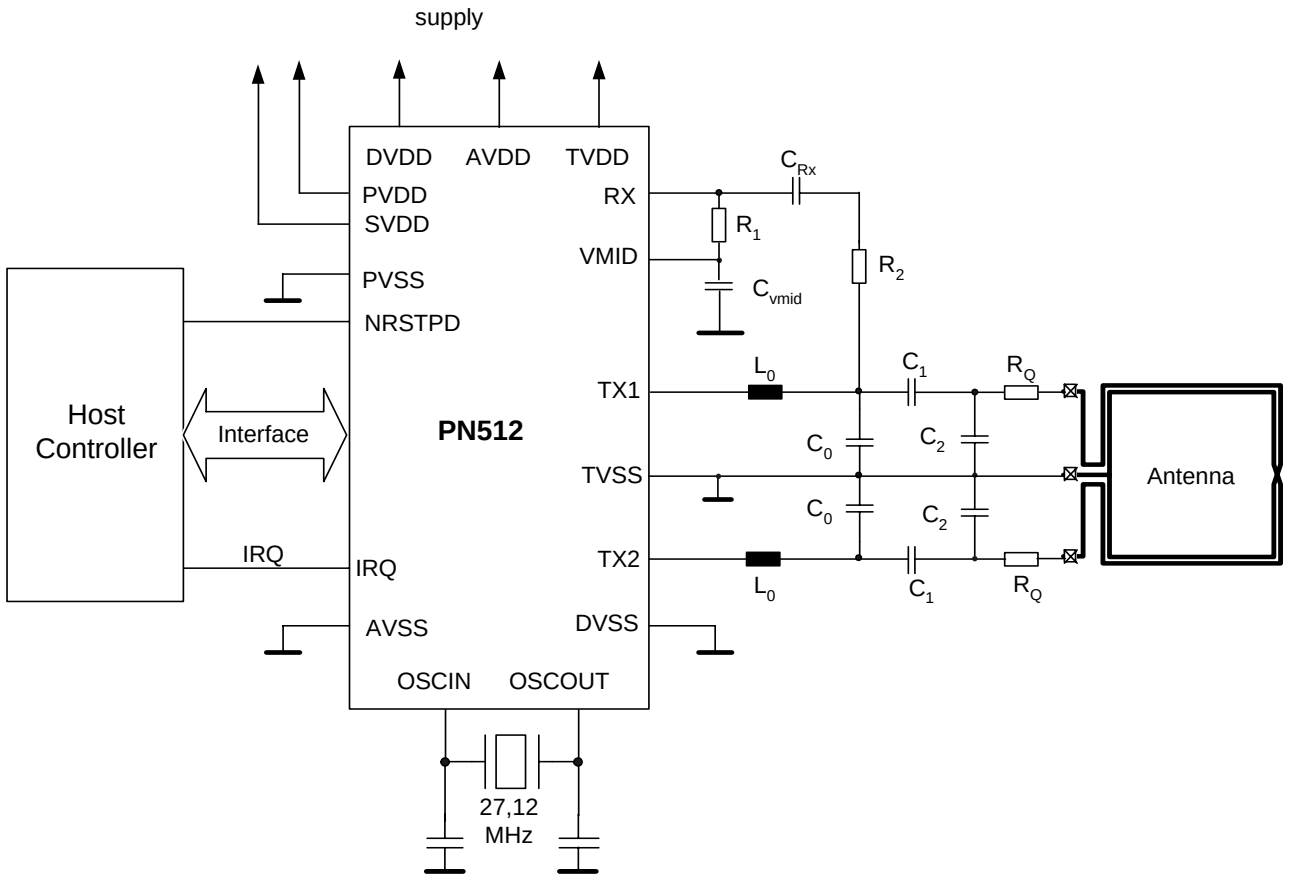


Fig 12. Typical Circuit Diagram

10. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
PV_{DD}	Supply voltage		-0.5	+4.0	V
P_{tot}	Total power dissipation per package (V_{BUS} and DV_{DD} in short cut mode)		-	200	mW
T_J	Junction temperature range			100	°C
ESDH	ESD Susceptibility (Human Body model)	1500 Ω, 100 pF; JESD22-A114-B		2000	V
ESDM	ESD Susceptibility (Machine model)	0.75 μH, 200 pF; JESD22-A114-A		200	V
ESDC	ESD Susceptibility (Charge Device model)	Field induced model; JESC22-C101-A		500	V

11. Package information

The PN512 can be delivered in 2 different packages.

Table 15. Package Information

Package	Remarks
HVQFN32	8-bit parallel interface not supported
HVQFN40	Supports the 8-bit parallel interface

12. Abbreviations

Table 16. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
Loadmodulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) measured at the card's coil.
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin).
PCD	Proximity Coupling Device. Definition for a Card reader/writer according to the ISO 14443 specification.
PICC	Proximity Cards. Definition for a contactless Smart Card according to the ISO 14443 specification.
PCD → PICC	Communication flow between a PCD and a PICC according to the ISO 14443A/Mifare
PICC → PCD	Communication flow between a PICC and a PCD according to the ISO 14443A/Mifare.
SAM	Secure Access Module
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).

13. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
124533	June 2007	Product short data sheet		Revision 3.2
Modifications:	• Add Section 14.4 “Licenses”			
124532	Januar 2007	Product short data sheet		Revision 3.1
Modifications:	• Usage of expression “host controller” unified			
124531	October 2006	Product short data sheet		Revision 3.0
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
	• Section 7.2 “Pin description” on page 8: - corrected in Table 3 “Pin description HVQFN32” Type of Pin 12: 0 -> **PWR** - corrected in Table 4 “Pin description HVQFN40” on page 9 Type of Pin 15: 0 -> **PWR** • Section 8.1.3 “ISO 14443B reader/writer functionality” on page 13: - added new Section			
124530	07 June 2006	Product short data sheet		
	• Initial version			

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Tables

17. Figures

continued >>

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