CY23FS08-04

FailSafe™ 1.8V Zero Delay Buffer

Features

- Internal DCXO for continuous glitch free operation
- Zero input-output propagation delay
- Low output cycle-to-cycle jitter (<46 ps RMS)
- Low output-output skew (<200 ps)
- 3.84 MHz reference input
- Supports industry standard input crystals
- Up to 133 MHz (industrial) outputs
- Phase-locked loop (PLL) bypass mode
- Dual reference inputs
- 28-pin SSOP
- 1.8V output power supplies
- 3.3V core power supply
- Industrial temperature

Functional Description

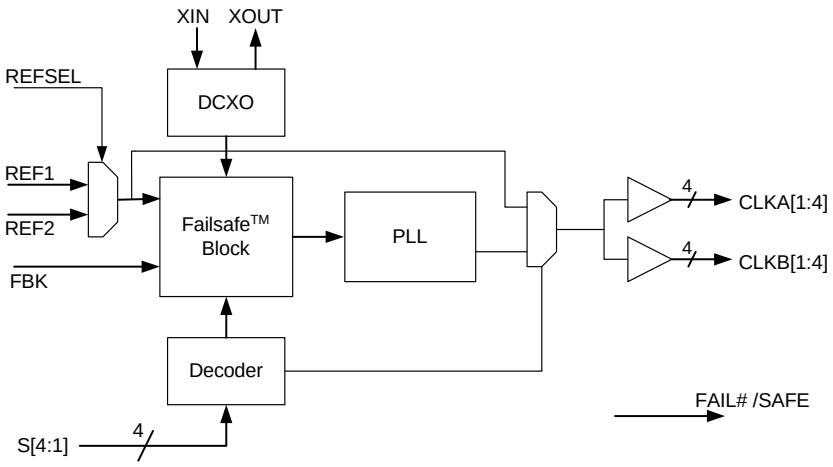
The CY23FS08-04 is a FailSafe Zero Delay Buffer with two reference clock inputs and eight phase aligned outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure.

Continuous, glitch free operation is achieved by using a DCXO that serves as a redundant clock source in the event of a reference clock failure by maintaining the last frequency and phase information of the reference clock.

The unique feature of the CY23FS08-04 is that the DCXO is in fact, the primary clocking source, that is synchronized (phase aligned) to the external reference clock. When this external clock is restored, the DCXO automatically resynchronizes to the external clock.

The frequency of the crystal that is connected to the DCXO is chosen as an integer factor of the frequency of the reference clock. This factor is set by four select lines: S[4:1]. For more information, see Table 2 on page 3. The CY23FS08-04 has three split power supplies; one for core, another for Bank A outputs, and the third for Bank B outputs. Each output power supply, except VDDC is connected to 1.8V. VDDC is the power supply pin for internal circuits and is connected to 3.3V.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 28 Pin SSOP

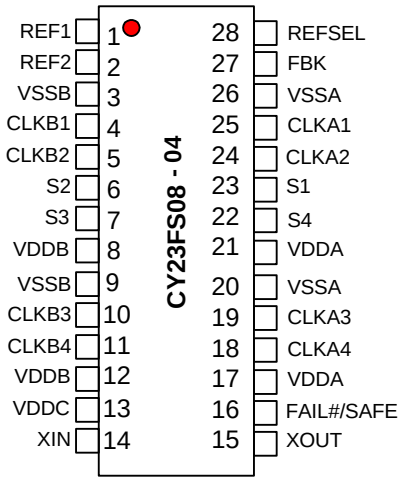


Table 1. Pin Definition - 28 Pin SSOP

Pin Number	Pin Name	Description
1,2	REF1,REF2	**5V Tolerant.** Reference clock inputs [3].
4,5,10,11	CLKB[1:4]	**Bank B Clock Outputs.**[1] CLKB3 and CLKB4 are differential signals when terminated as shown in Figure 8 on page 6. CLKB3 is negtive output, CLKB4 is positive output.
25,24,19,18	CLKA[1:4]	**Bank A Clock Outputs.**[1]
27	FBK	**No Connect, Internal Feedback.**
23,6,7,22	S[1:4]	**Frequency Select Pins.**[2]
14	XIN	**Reference Crystal Input.**
15	XOUT	**Reference Crystal Output.**
16	FAIL#/SAFE	**Valid Reference Indicator.** A high level indicates a valid reference input.
13	VDDC	**3.3V Power Supply for the Internal Circuitry.**
8,12	VDDB	**1.8V Power Supply for Bank B Outputs.**
3,9	VSSB	**Ground.**
17,21	VDDA	**1.8V Power Supply for Bank A Outputs.**
20,26	VSSA	**Ground.**
28	REFSEL	**Reference Select.** Selects the active reference clock from either REF1 or REF2. REFSEL = 1, REF1 is selected, REFSEL = 0, REF2 is selected.[3]

Notes
1. Weak pull downs on all outputs.
2. Weak pull ups on these inputs.
3. Weak pull downs on these inputs.

Table 2. Configuration Table

S[4:1]	XTAL (MHz)		REF(MHz)		Xtal/REF Ratio	OUT/REF Ratio							
	Min	Max	Min	Max		CLKA1	CLKA2	CLKA3	CLKA4	CLKB1	CLKB2	CLKB3	CLKB4
0000	15.36	16.384	3.84	4.096	4	32	32	32	32	32	32	32	32
0001	15.36	16.384	3.84	4.096	4	Off	Off	32	32	32	32	32	32
0010	15.36	16.384	3.84	4.096	4	Off	Off	Off	Off	32	32	32	32
0011	15.36	16.384	3.84	4.096	4	Off	Off	16	16	32	32	32	32
0100	15.36	16.384	3.84	4.096	4	Off	Off	Off	Off	Off	Off	32	32
0101	15.36	16.384	3.84	4.096	4	8	8	16	16	32	32	32	32
0110	15.36	16.384	3.84	4.096	4	8	8	8	8	16	16	16	16
0111	15.36	16.384	3.84	4.096	4	1	1	10	10	20	20	20	20
1xxx	-	-	-	-	-	Off	Off	Off	Off	Off	Off	Off	Off

FailSafe Function

The CY23FS08-04 is targeted at clock distribution applications that can or currently require continued operation, if the main reference clock fail. Existing approaches to this requirement have used multiple reference clocks with either internal or external methods for switching between references. The problem with this technique is that it leads to interruptions (or glitches) when transitioning from one reference to another. This often requires complex external circuitry or software to maintain system stability. The technique implemented in this design completely eliminates any switching of references to the PLL that greatly simplifies the system design.

The CY23FS08-04 PLL is driven by the crystal oscillator that is phase aligned to an external reference clock. It is aligned in a way that the output of the device is effectively phase aligned to reference via the external feedback loop. This is accomplished by using a digitally controlled capacitor array to pull the crystal frequency over an approximate range of ±100 ppm from its nominal frequency.

In this mode, if the reference frequency fails (that is, stop or disappear), the DCXO maintains its last setting. Then a flag signal (FAIL#/SAFE) is set to indicate failure of the reference clock.

The CY23FS08-04 provides four select bits, S1 through S4 to control the reference to crystal frequency ratio. The DCXO is internally tuned to the phase and frequency of the external reference only when the reference frequency divided by this ratio is within the DCXO capture range. If the frequency is out of range, a flag is set on the FAIL#/SAFE pin notifying the system that the selected reference is not valid. If the reference moves in range, then the flag is cleared indicating the system that the selected reference is valid.

Figure 2. Fail#/safe timing for input reference failing catastrophically

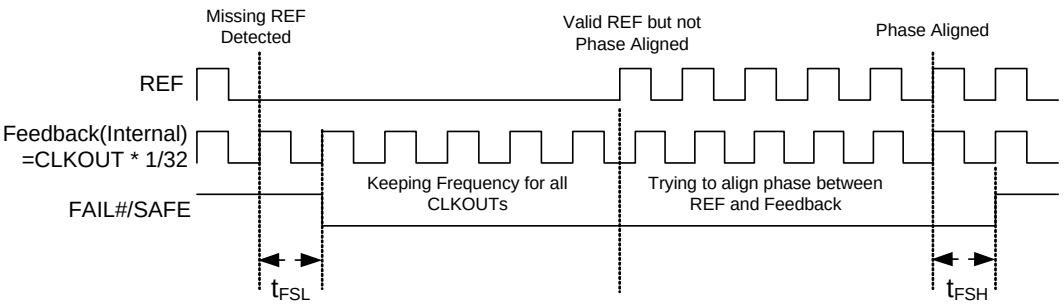


Figure 3. Fail#/safe Timing formula

$$t_{FSL(max)} = t_{REF} + 25ns$$

$$t_{FSH(min)} = t_{REF} + 25ns$$

Table 3. FailSafe Timing Table

Parameter	Description	Conditions	Min	Max	Unit
t_{FSL}	Fail#/Safe Assert Delay	Measured at 80% to 20%, Load = 15 pF		See Figure 3	ns
t_{FSH}	Fail#/Safe Deassert Delay	Measured at 80% to 20%, Load = 15 pF	See Figure 3		ns

DCXO and capture range

Failsafe has DCXO for tracking to incoming reference clock. The CY23FS08-04 is configured its capture range of approx +/- 100ppm with using pullable crystal that specified in Table 7.

Figure 4. FailSafe Timing Diagram: Input Reference Slowly Drifting Out of FailSafe Capture Range

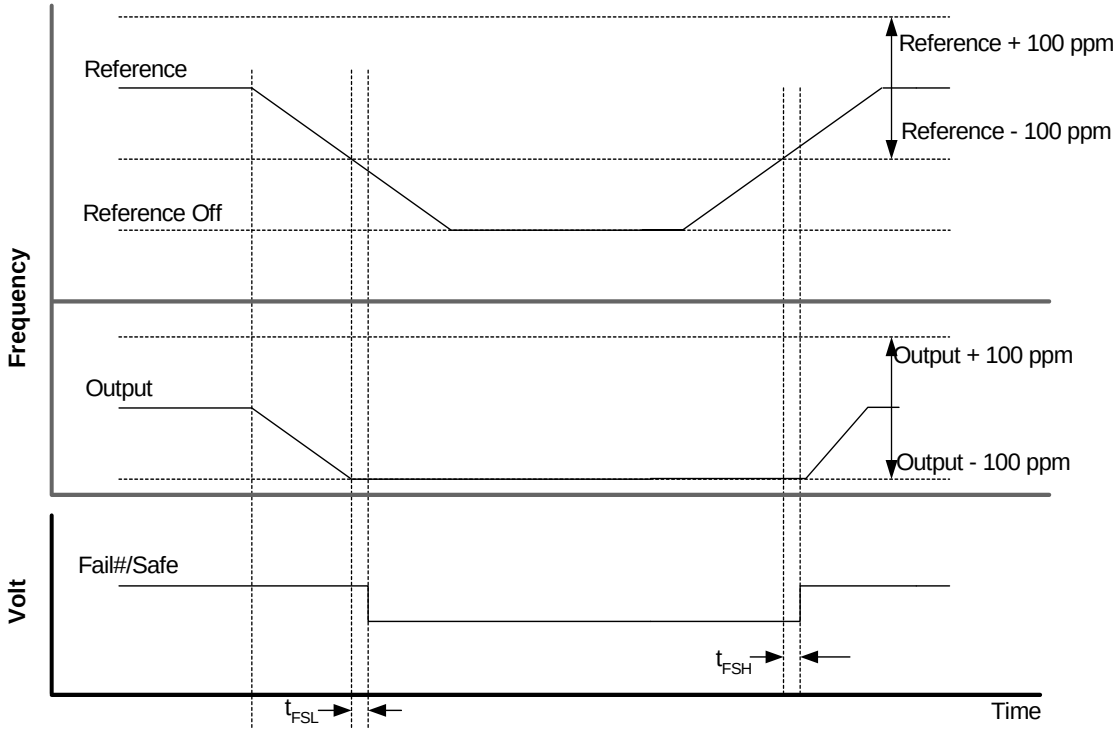


Figure 5. FailSafe Reference Switching Behavior

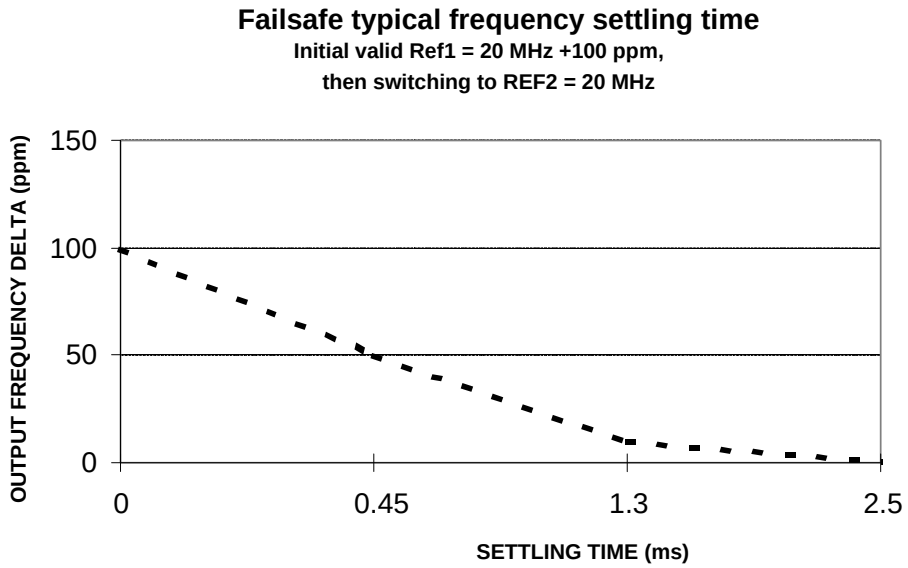


Figure 6. FailSafe Effective Loop Bandwidth (Min)

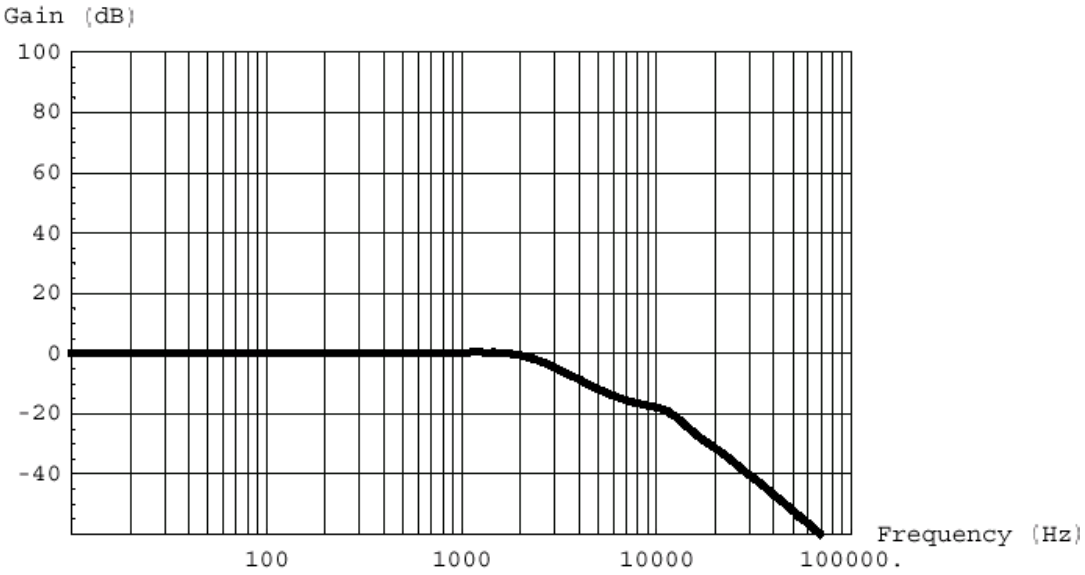


Figure 7. Sample Timing of Muxing Between Two Reference Clocks 180°C Out of Phase and Resulting Output Phase Offset Typical Settling Time (105 MHz)

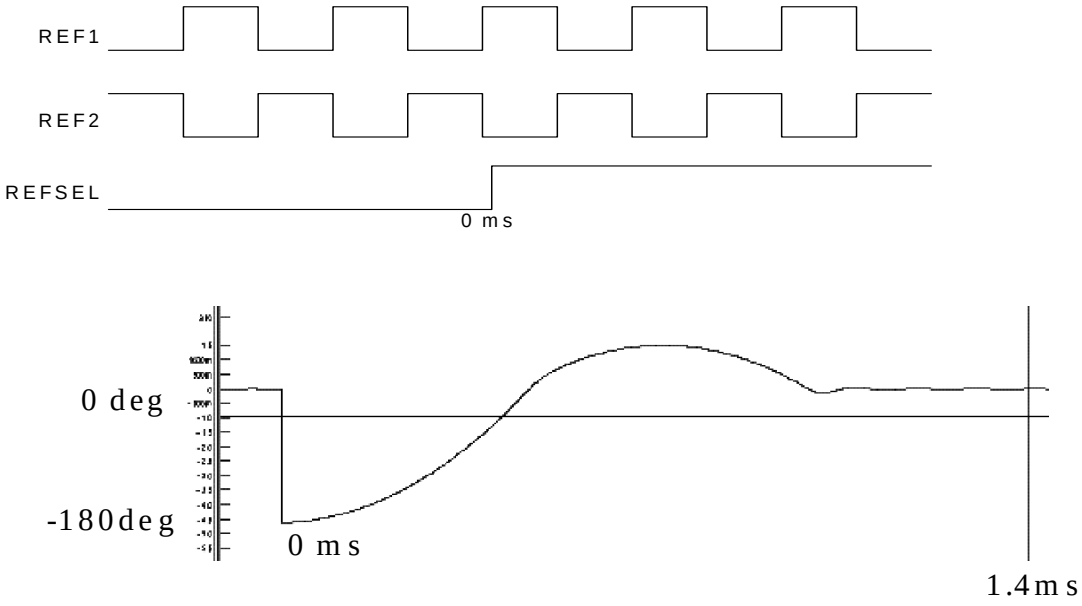
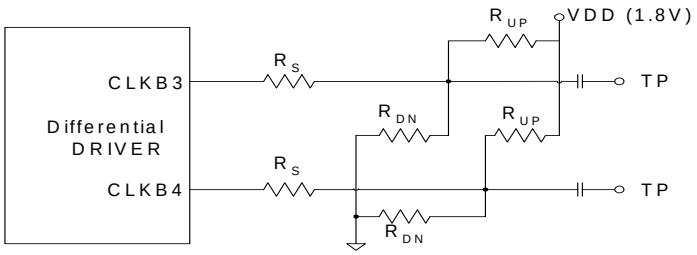
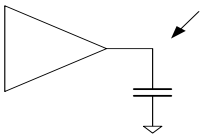


Figure 8. Output Termination for Differential Output and Measurement Setup for Single-Ended Outputs

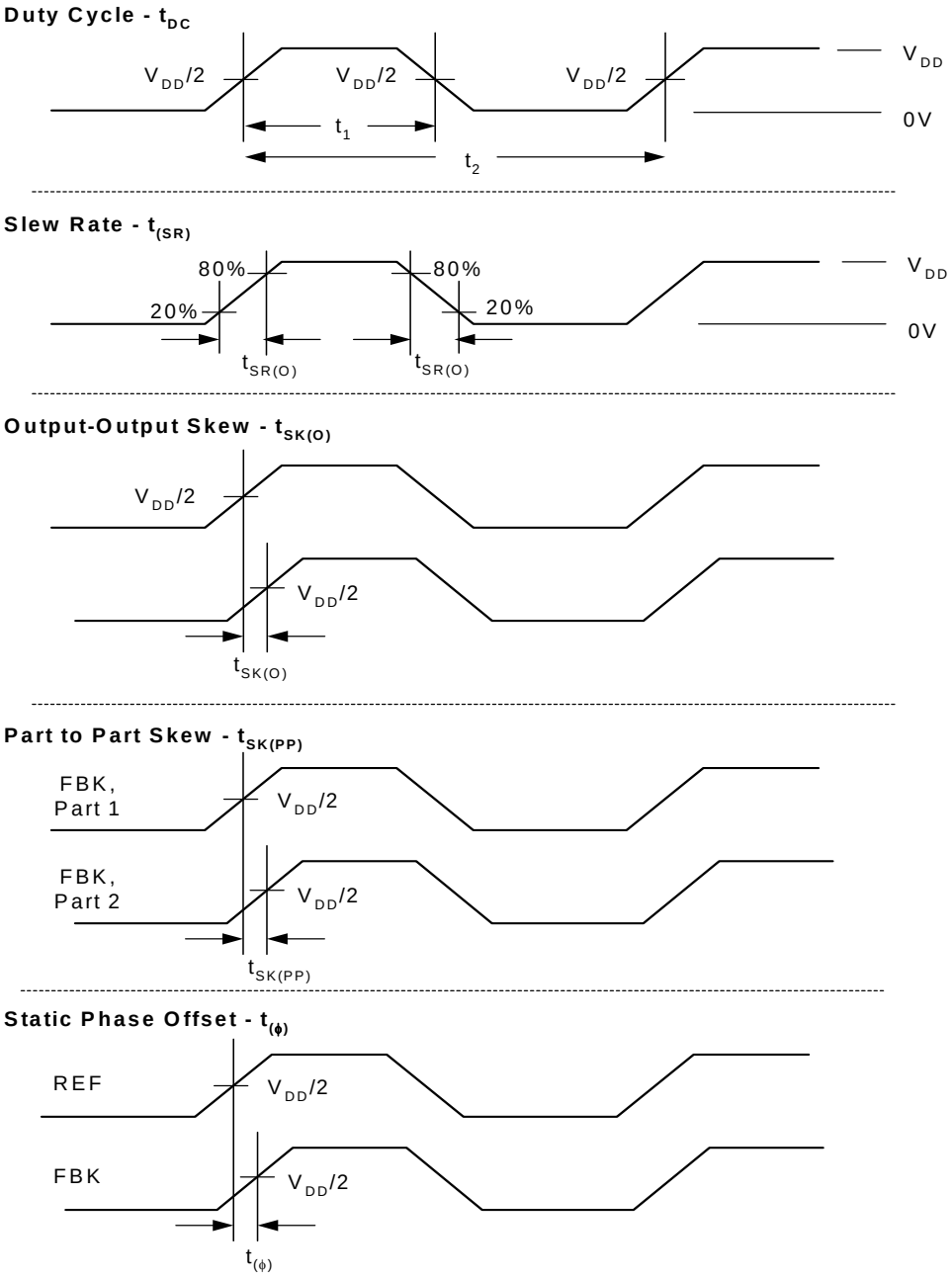


Differential Output Termination Network for CLKB3 and CLKB4



Measurement point for single-ended clocks

Figure 9. Waveforms for Timing Parameters



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD}+0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Industrial Grade	–40	85	°C
T_J	Temperature, Junction	Functional		125	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000		V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Specification 883E Method 1012.1	36.17		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	100.6		°C/W
UL–94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.

Table 4. Operating Conditions for FailSafe Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DDC}	3.3V Supply Voltage	3.135	3.465	V
V_{DDA}, V_{DDB}	1.8V Supply Voltage Range	1.70	1.90	V
T_A	Ambient Operating Temperature, Industrial	–40	85	°C
C_L	Output Load Capacitance		15	pF
C_{IN}	Input Capacitance (Except XIN)		7	pF
C_{XIN}	Crystal Input Capacitance (All internal caps off)	10	13	pF
T_{PU}	Power Up Time for all VDDs to Reach Minimum Specified Voltage (Power ramps are monotonic)	0.05	500	ms

Table 5. Electrical Characteristics for FailSafe Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	CMOS Levels, 30% of V_{DD}			$0.3xV_{DD}$	V
V_{IH}	Input High Voltage	CMOS Levels, 70% of V_{DD}	$0.7xV_{DD}$			V
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$ (100k pull up only)			50	µA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$ (100k pull down only)			50	µA
I_{OL}	Output Low Current	V_{OL} = 0.5V, V_{DD} = 1.8V	10			mA
I_{OH}	Output High Current	$V_{OH} = V_{DD}$ – 0.5V, V_{DD} = 1.8V			10	mA
I_{DD}	Dynamic Current	V_{DDA}, V_{DDB}, and V_{DDC} are all at the maximum values, I_{OUT} = 0mA, output frequency = maximum			75	mA
I_{DDQ}	Quiescent Current	All inputs are grounded, PLL and DCXO are in bypass mode, Reference input = 0			250	µA

Table 6. Switching Characteristics for FailSafe Industrial Temperature Devices

Parameter [5]	Description	Test Conditions	Min	Typ	Max	Unit
f_{REF}	Reference Frequency	Industrial Grade	1.0	–	4.1	MHz
f_{OUT}	Output Frequency	15 pF Load	1.0	–	133	MHz
f_{XIN}	DCXO Frequency		15	–	25	MHz
t_{DC}	Duty Cycle	Measured at $V_{DD}/2$	40	–	60	%
$t_{SR(I)}$	Input Slew Rate	Measured on REF1 Input, 30% to 70% of V_{DD}	0.5	–	4.0	V/ns
$t_{SR(O)}$	Output Slew Rate	Measured from 20% to 80% of V_{DD} = 1.8V, 15 pF Load	0.3	–	3.0	V/ns
$t_{SK(O)}$	Output to Output Skew	All outputs equally loaded, measured at $V_{DD}/2$	–	110	200	ps
$t_{SK(IB)}$	Intrabank Skew	All outputs equally loaded, measured at $V_{DD}/2$	–	–	75	ps
$t_{(\phi)}$ [4]	Static Phase Offset	Measured at $V_{DD}/2$	–	–	250	ps
$t_{D(\phi)}$ [4]	Dynamic Phase Offset	Measured at $V_{DD}/2$	–	150	200	ps
$t_{J(CC)}$	Cycle-to-Cycle Jitter	Load = 15 pF, $f_{OUT} \geq 6.25$ MHz	–	200	250	ps
			–	18	46	ps_{RMS}

Table 7. Pullable Crystal Specifications

Parameter	Description	Min	Typ	Max	Unit
CR load	Crystal Load Capacitance		16		pF
C_0 / C_1	C_0 / C_1 Ratio		240		
ESR	Equivalent Series Resistance			50	Ω

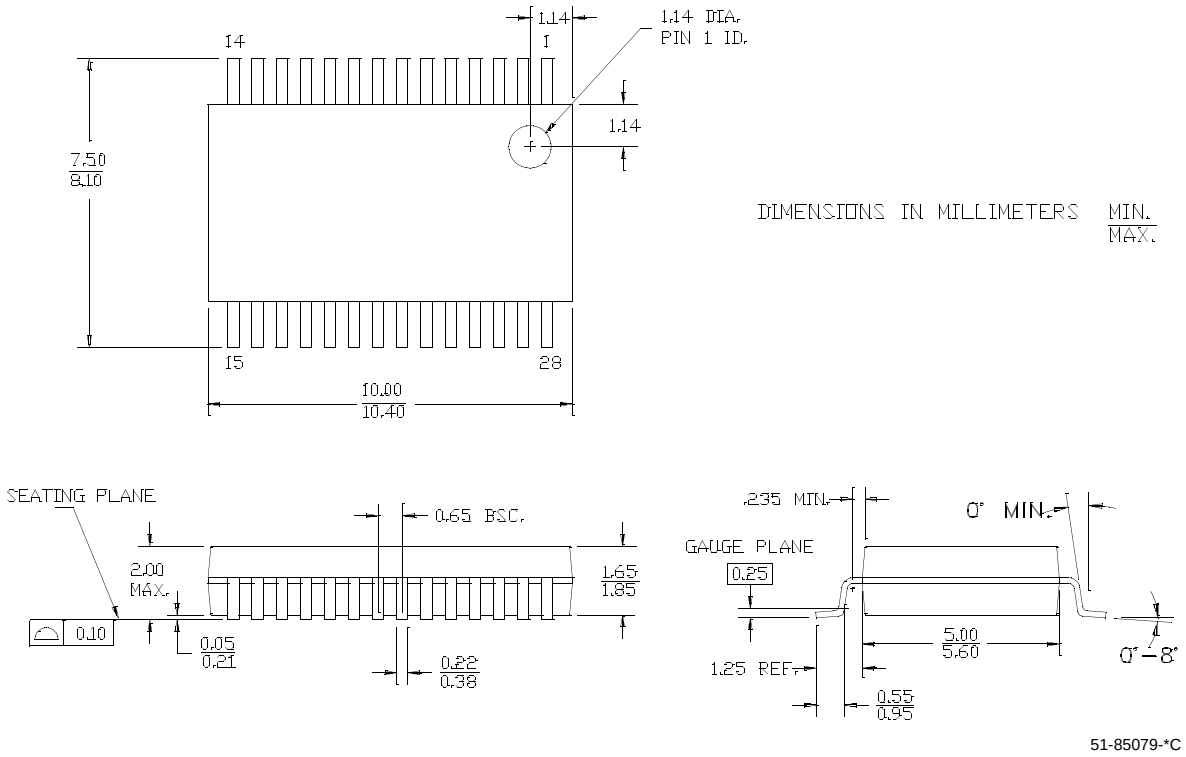
Notes
4. The $t_{(\phi)}$ reference feedback input delay is guaranteed for a maximum 4:1 input edge ratio between the two signals as long as $t_{SR(I)}$ is maintained.
5. Parameters are guaranteed by design and characterization. Not 100% tested in production.

Ordering Information

Part Number	Package Type	Product Flow
Pb-Free		
CY23FS08OXI-04	28-pin SSOP	Industrial, –40°C to 85°C
CY23FS08OXI-04T	28-pin SSOP – Tape and Reel	Industrial, –40°C to 85°C

Package Drawing and Dimensions

Figure 10. 28-Pin (5.3 mm) Shrunk Small Outline Package O28



Document History Page

Document Title: CY23FS08-04 FailSafe™ 1.8V Zero Delay Buffer Document Number: 001-17042				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1493204	See ECN	XHT/WWZ/ AESA	New data sheet