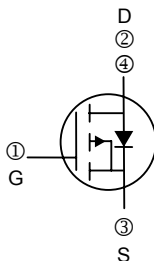


RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

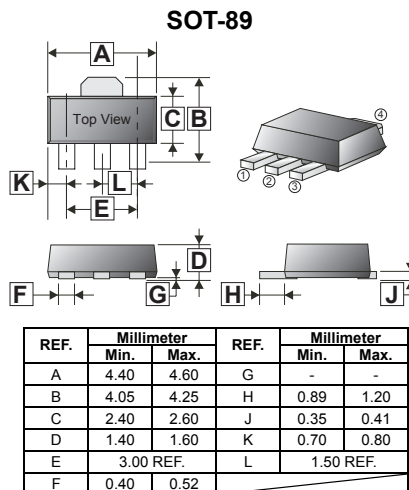
FEATURES

- The SGM2305A provide the designer with best combination of fast switching, low on-resistance and cost-effectiveness.
- The SGM2305A is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.
- Simple Drive Requirement
- Surface Mount Device



PACKAGE INFORMATION

Weight: 0.0508 g (approximately)



MARKING



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ³	$I_D @ T_A = 25^\circ\text{C}$	-3.2	A
Continuous Drain Current ³	$I_D @ T_A = 70^\circ\text{C}$	-2.6	A
Pulsed Drain Current ^{1,2}	I_{DM}	-10	A
Total Power Dissipation	$P_D @ T_A = 25^\circ\text{C}$	1.5	W
Linear Derating Factor		0.012	W / $^\circ\text{C}$
Operating Junction & Storage temperature	T_J, T_{STG}	-55~150	$^\circ\text{C}$

THERMAL DATA

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient ³ Max.	$R_{\theta JA}$	83.3	$^\circ\text{C} / \text{W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	$V_{GS} = 0, I_D = -250 \mu\text{A}$
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	-	-0.1	-	V / $^\circ\text{C}$	Reference to 25°C , $I_D = -1 \text{ mA}$
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	-	-1.2	V	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$
Forward Trans-conductance	g_{fs}	-	9	-	S	$V_{DS} = -5\text{V}, I_D = -3\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 12\text{V}$
Drain-Source Leakage Current ($T_J = 25^\circ\text{C}$)	I_{DSS}	-	-	-1	μA	$V_{DS} = -30 \text{ V}, V_{GS} = 0$
Drain-Source Leakage Current ($T_J = 70^\circ\text{C}$)		-	-	-25		$V_{DS} = -24 \text{ V}, V_{GS} = 0$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	-	65	m Ω	$V_{GS} = -10\text{V}, I_D = -3.2\text{A}$
		-	-	80		$V_{GS} = -4.5\text{V}, I_D = -3.0\text{A}$
		-	-	150		$V_{GS} = -2.5\text{V}, I_D = -2.0\text{A}$
		-	-	250		$V_{GS} = -1.8\text{V}, I_D = -1.0\text{A}$
Total Gate Charge ²	Q_g	-	10	18	nC	$I_D = -3.2 \text{ A}$ $V_{DS} = -24 \text{ V}$ $V_{GS} = -4.5 \text{ V}$
Gate-Source Charge	Q_{gs}	-	1.8	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	3.6	-		
Turn-on Delay Time ²	$T_{d(on)}$	-	7	-	nS	$V_{DS} = -15 \text{ V}$ $I_D = -3.2 \text{ A}$ $V_{GS} = -10 \text{ V}$ $R_G = 3.3 \Omega$ $R_D = 4.6 \Omega$
Rise Time	T_r	-	15	-		
Turn-off Delay Time	$T_{d(off)}$	-	21	-		
Fall Time	T_f	-	15	-		
Input Capacitance	C_{iss}	-	735	1325	pF	$V_{GS} = 0 \text{ V}$ $V_{DS} = -25 \text{ V}$ $f = 1.0 \text{ MHz}$
Output Capacitance	C_{oss}	-	100	-		
Reverse Transfer Capacitance	C_{rss}	-	80	-		

SOURCE-DRAIN DIODE

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Forward On Voltage ²	V_{SD}	-	-	-1.2	V	$I_S = -1.2\text{A}, V_{GS} = 0\text{V}$
Reverse Recovery Time ²	T_{rr}	-	24	-	ns	$I_S = -3.2\text{A}, V_{GS} = 0\text{V}$
Reverse Recovery Charge	Q_{rr}	-	19	-	nC	$dI/dt = 100 \text{ A} / \mu\text{S}$

- Notes:
1. Pulse width limited by safe operating area.
 2. Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
 3. Surface mounted on FR4 board, $t \leq 10\text{sec}$.

CHARACTERISTIC CURVES

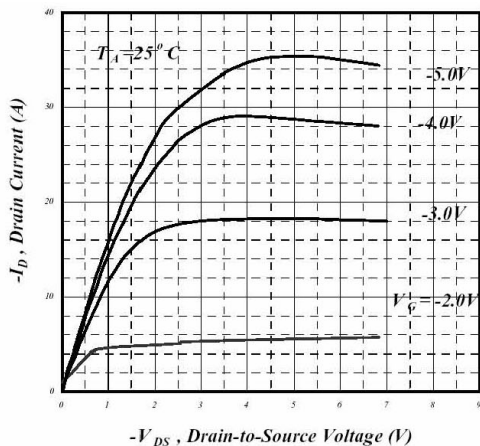


Fig 1. Typical Output Characteristics

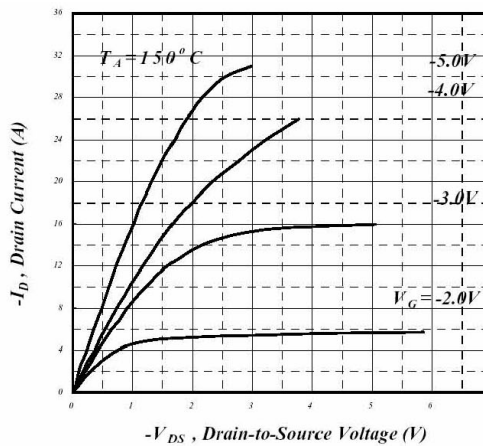


Fig 2. Typical Output Characteristics

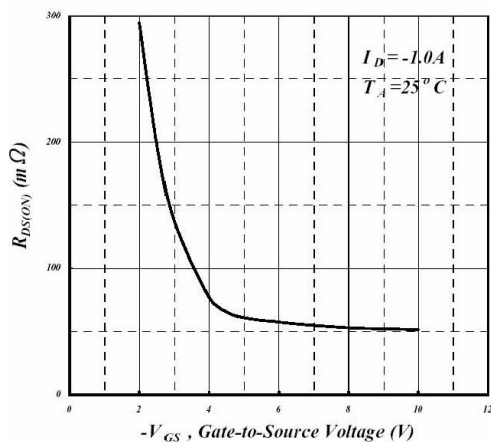


Fig 3. On-Resistance v.s. Gate Voltage

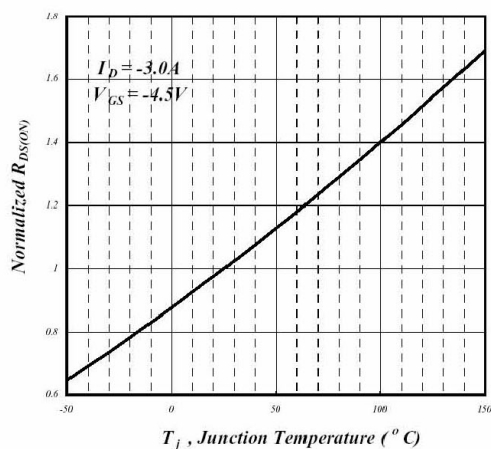


Fig 4. Normalized On-Resistance v.s. Junction Temperature

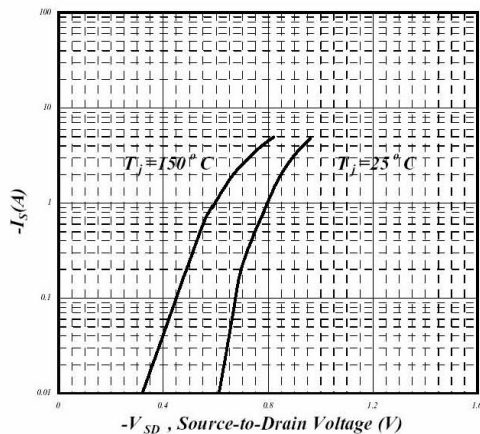


Fig 5. Forward Characteristics of Reverse Diode

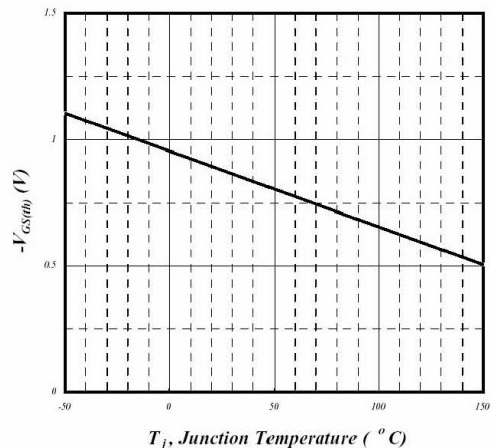


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTIC CURVES (cont'd)

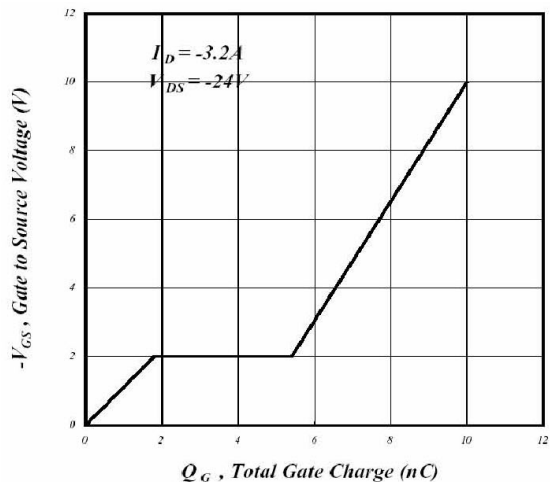


Fig 7. Gate Charge Characteristics

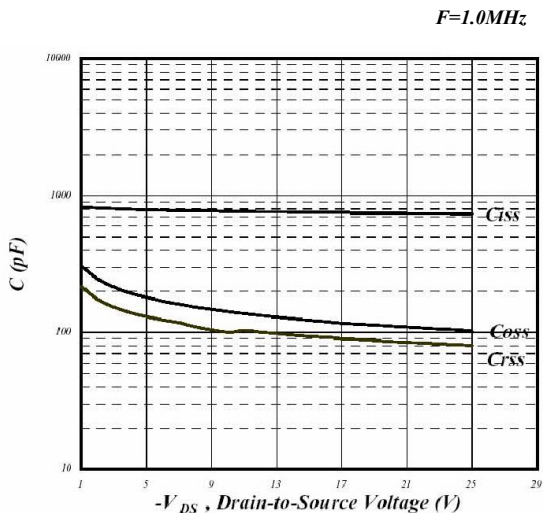


Fig 8. Typical Capacitance Characteristics

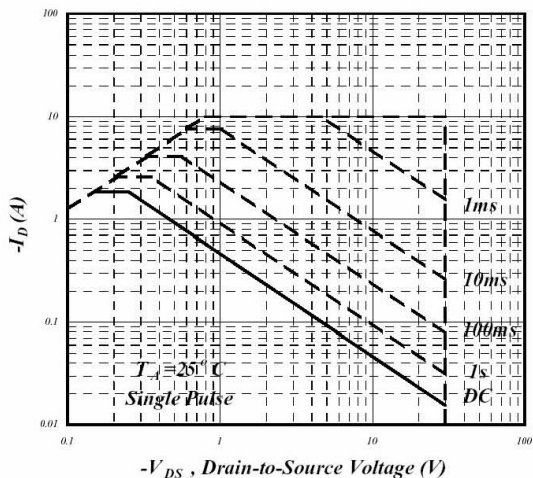


Fig 9. Maximum Safe Operating Area

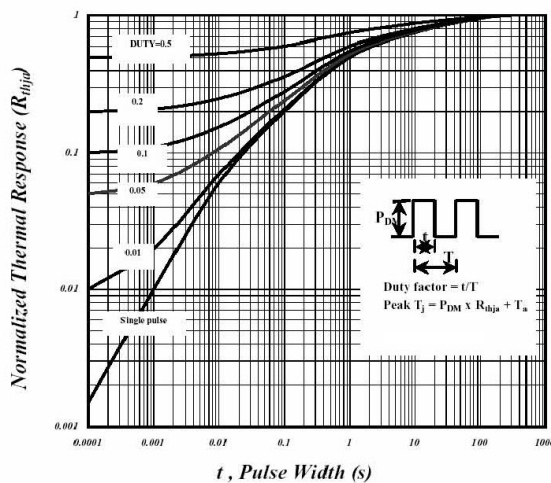


Fig 10. Effective Transient Thermal Impedance

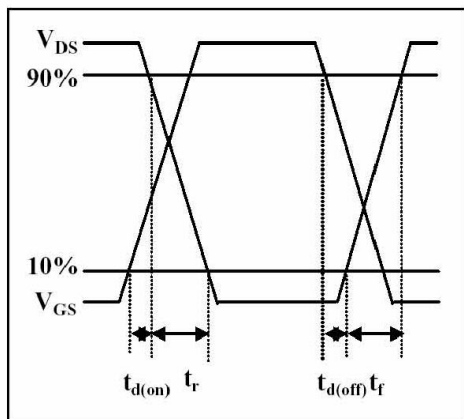


Fig 11. Switching Time Waveform

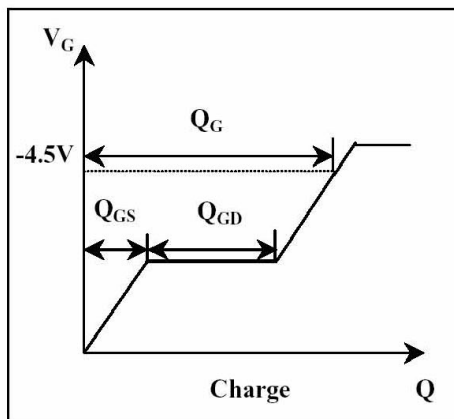


Fig 12. Gate Charge Waveform