NGB8207AN

Ignition IGBT

20 A, 365 V, N−Channel D²PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Overvoltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil−on−Plug and Driver−on−Coil Applications
- Gate−Emitter ESD Protection
- Temperature Compensated Gate−Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage for Interfacing Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Minimum Avalanche Energy − 500 mJ
- Gate Resistor (R_G) = 70 Ω
- This is a Pb−Free Device

Applications

- Ignition Systems

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CES}	365	V
Gate−Emitter Voltage	V_{GE}	±15	V
Collector Current−Continuous @ T_C = 25°C − Pulsed	I_C	20 50	A_{DC} A_{AC}
Continuous Gate Current	I_G	1.0	mA
Transient Gate Current (t ≤ 2 ms, f ≤ 100 Hz)	I_G	20	mA
ESD (Charged−Device Model)	ESD	2.0	kV
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	500	V
Total Power Dissipation @ T_C = 25°C Derate above 25°C (Note 1)	P_D	165 1.1	W W/°C
Operating & Storage Temperature Range	T_J, T_{stg}	−55 to +175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Assuming infinite heatsink Case−to−Ambient

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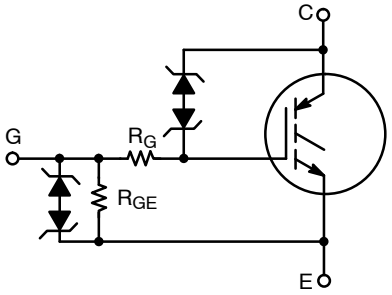
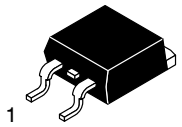
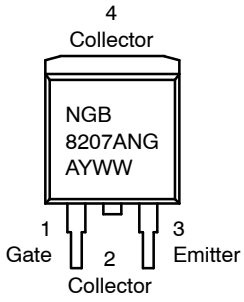
20 AMPS
365 VOLTS
$V_{CE(on)}$ = 1.75 V
Typ @ I_C = 10 A, V_{GE} ≥ 4.5 V





D²PAK
CASE 418B
STYLE 4

MARKING DIAGRAM



NGB8207AN = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NGB8207ANT4G	D²PAK (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

UNCLAMPED COLLECTOR−TO−EMITTER AVALANCHE CHARACTERISTICS ($-40° \le T_J \le 150°C$)

Characteristic	Symbol	Value	Unit
Single Pulse Collector−to−Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 10 V, Pk I_L = 16.5 A, L = 3.7 mH, R_g = 1 kΩ Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 10 V, Pk I_L = 10 A, L = 6.1 mH, R_g = 1 kΩ Starting T_J = 125°C	E_{AS}	 500 306	mJ
Reverse Avalanche Energy V_{CC} = 100 V, V_{GE} = 20 V, Pk I_L = 25.8 A, L = 6.0 mH, Starting T_J = 25°C	$E_{AS(R)}$	2000	mJ

THERMAL CHARACTERISTICS

Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.9	°C/W
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	50	°C/W
Maximum Temperature for Soldering Purposes, 0.125 in from case for 5 seconds (Note 3)	T_L	275	°C

2. When surface mounted to an FR4 board using the minimum recommended pad size.
3. For further details, see Soldering and Mounting Techniques Reference Manual: SOLDERRM/D.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector−Emitter Clamp Voltage	BV_{CES}	I_C = 2.0 mA	T_J = −40°C to 150°C	325	350	375	V
		I_C = 10 mA	T_J = −40°C to 150°C	340	365	390	
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 24 V, V_{GE} = 0 V	T_J = 25°C		0.1	2.0	μA
		V_{CE} = 250 V, V_{GE} = 0 V	T_J = 25°C	−	1.0	5	
			T_J = 150°C	−	10	125	
			T_J = −40°C	−	0.25	2.5	
Reverse Collector−Emitter Clamp Voltage	$B_{VCES(R)}$	I_C = −75 mA	T_J = 25°C	25	27	29	V
			T_J = 150°C	25	29	31	
			T_J = −40°C	24	26	29	
Reverse Collector−Emitter Leakage Current	$I_{CES(R)}$	V_{CE} = −24 V	T_J = 25°C	−	0.5	1.1	mA
			T_J = 150°C	20	25	40	
			T_J = −40°C	−	0.03	1.0	
Gate−Emitter Clamp Voltage	BV_{GES}	I_G = ±5.0 mA	T_J = −40°C to 150°C	12	13	14.5	V
Gate−Emitter Leakage Current	I_{GES}	V_{GE} = ±10 V	T_J = −40°C to 150°C	500	700	1000	μA
Gate Resistor	R_G		T_J = −40°C to 150°C		70		Ω
Gate−Emitter Resistor	R_{GE}		T_J = −40°C to 150°C	14.25	16	25	kΩ
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GE(th)}$	I_C = 1.0 mA, V_{GE} = V_{CE}	T_J = 25°C	1.2	1.5	2.0	V
			T_J = 150°C	0.7	1.0	1.3	
			T_J = −40°C	1.4	1.7	2.0	
Threshold Temperature Coefficient (Negative)				−	4.0	−	mV/°C
Collector−to−Emitter On−Voltage	$V_{CE(on)}$	I_C = 6.0 A, V_{GE} = 4.0 V	T_J = 25°C	1.15	1.5	1.75	V
			T_J = 150°C	1.2	1.4	1.75	
			T_J = −40°C	1.2	1.6	1.75	
		I_C = 10 mA, V_{GE} = 4.5 V	T_J = 25°C	−	0.62	1.0	

*Maximum Value of Characteristic across Temperature Range.
4. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)							
Collector−to−Emitter On−Voltage	$V_{CE(on)}$	I_C = 8.0 A, V_{GE} = 4.0 V	T_J = 25°C	1.2	1.65	2.0	V
			T_J = 150°C	1.4	1.6	2.0	
			T_J = −40°C	1.4	1.7	2.0	
		I_C = 10 A, V_{GE} = 3.7 V	T_J = 25°C	1.35	1.8	2.2	
			T_J = 150°C	1.5	1.9	2.2	
			T_J = −40°C	1.5	1.85	2.2	
		I_C = 10 A, V_{GE} = 4.0 V	T_J = 25°C	1.35	1.8	2.1	
			T_J = 150°C	1.5	1.8	2.1	
			T_J = −40°C	1.5	1.8	2.1	
		I_C = 10 A, V_{GE} = 4.5 V	T_J = 25°C	1.35	1.75	2.05	
			T_J = 150°C	1.4	1.75	2.1	
			T_J = −40°C	1.4	1.8	2.1	
Forward Transconductance	gfs	I_C = 6.0 A, V_{CE} = 5.0 V	T_J = 25°C	–	15.8	–	Mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{ISS}	f = 10 kHz, V_{CE} = 25 V	T_J = 25°C	750	810	900	pF
Output Capacitance	C_{OSS}			75	90	105	
Transfer Capacitance	C_{RSS}			4	7	12	
SWITCHING CHARACTERISTICS							
Turn−On Delay Time (Resistive) Low Voltage	$t_{d(on)}$	V_{CE} = 14 V, R_L = 1.0 Ω, V_{GE} = 5.0 V, R_G = 1000 Ω	T_J = 25°C	0.5	0.55	0.7	μSec
Rise Time (Resistive) Low Voltage	t_r		T_J = 25°C	2.0	2.32	2.7	
Turn−Off Delay Time (Resistive) Low Voltage	$t_{d(off)}$	V_{CE} = 14 V, R_L = 1.0 Ω, V_{GE} = 5.0 V, R_G = 1000 Ω	T_J = 25°C	2.0	2.5	3.0	
Fall Time (Resistive) Low Voltage	t_f		T_J = 25°C	8.0	10	13	
Turn−On Delay Time (Resistive) High Voltage	$t_{d(on)}$	V_{CE} = 300 V, R_L = 46 Ω, V_{GE} = 5.0 V, R_G = 1000 Ω	T_J = 25°C	0.5	0.65	0.75	
Rise Time (Resistive) High Voltage	t_r		T_J = 25°C	0.7	1.8	2.0	
Turn−Off Delay Time (Resistive) High Voltage	$t_{d(off)}$	V_{CE} = 300 V, R_L = 46 Ω, V_{GE} = 5.0 V, R_G = 1000 Ω	T_J = 25°C	4.0	4.7	6.0	
Fall Time (Resistive) High Voltage	t_f		T_J = 25°C	6.0	10	15	

*Maximum Value of Characteristic across Temperature Range.

4. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

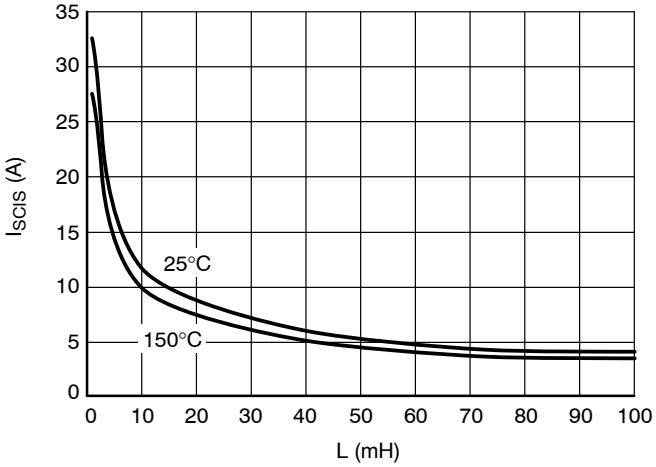


Figure 1. Typical Self Clamped Inductive Switching Performance (SCIS)

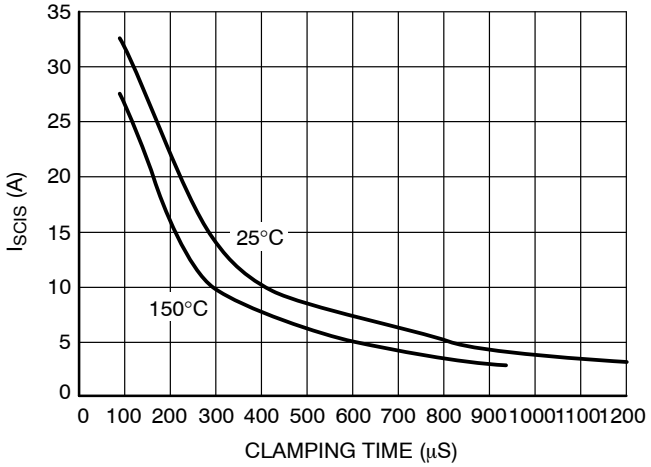


Figure 2. Typical Self Clamped Inductive Switching Performance (SCIS)

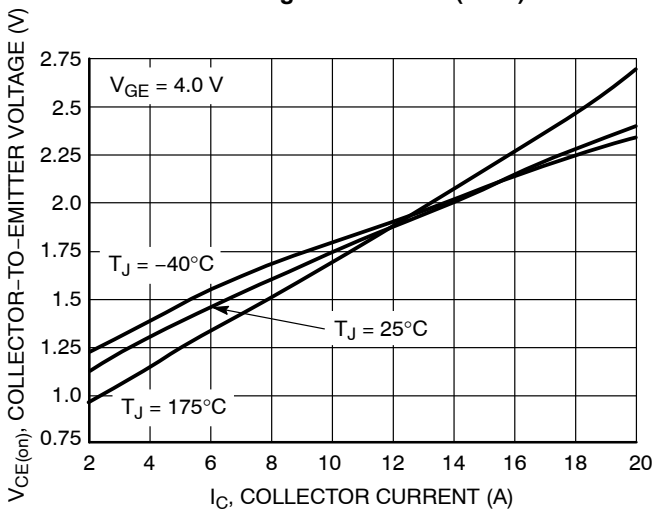


Figure 3. Collector−to−Emitter Voltage vs. Collector Current

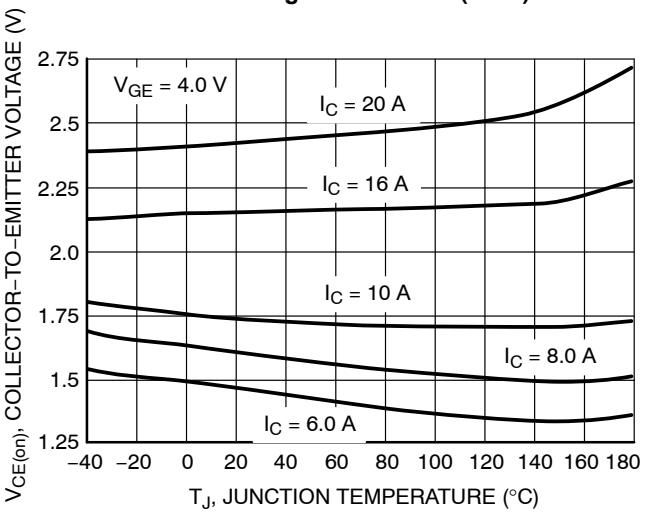


Figure 4. Collector−to−Emitter Voltage vs. Junction Temperature

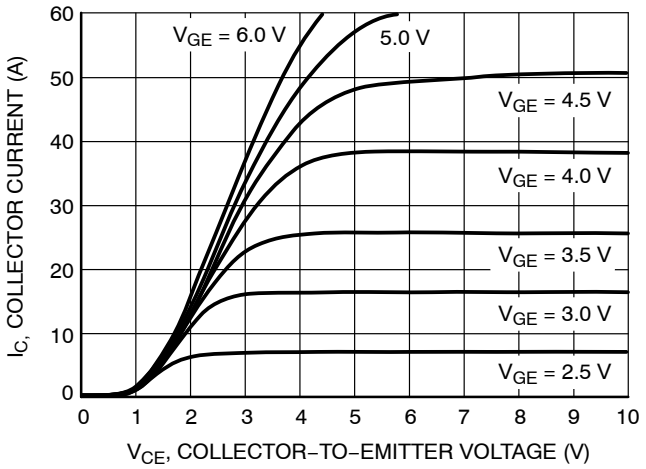


Figure 5. On−Region Characteristics @ T_J = 25°C

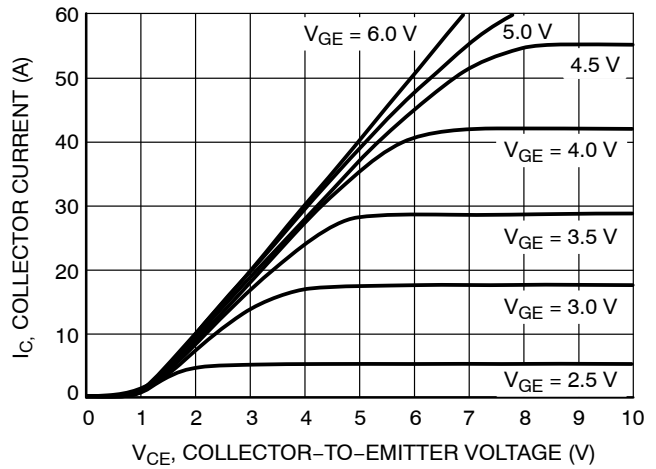


Figure 6. On−Region Characteristics @ T_J = −40°C

TYPICAL ELECTRICAL CHARACTERISTICS

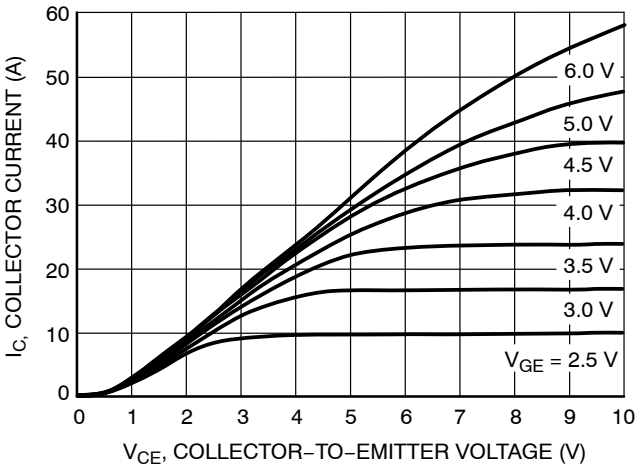


Figure 7. On−Region Characteristics @ T_J = 175°C

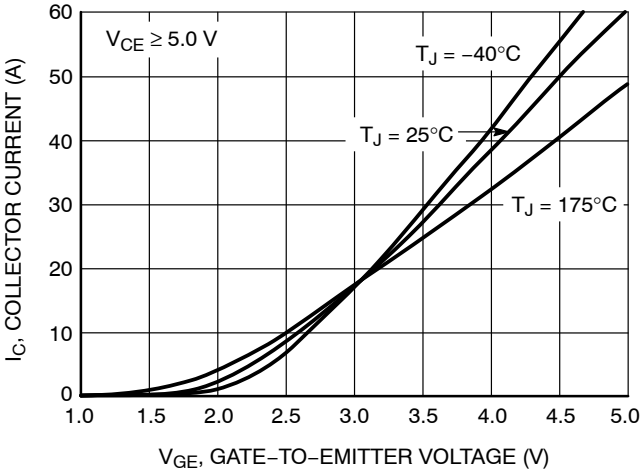


Figure 8. Transfer Characteristics

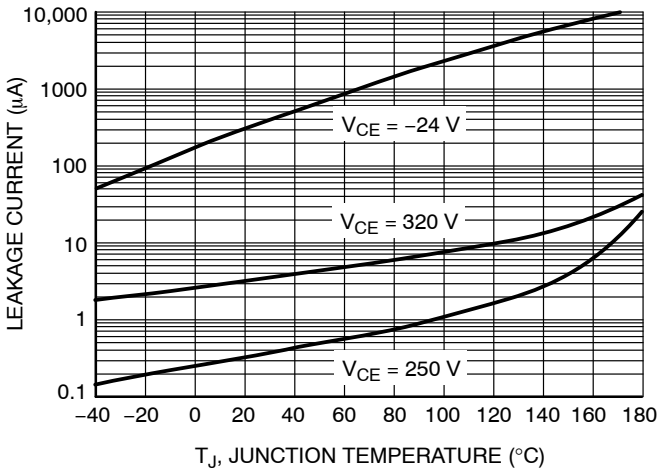


Figure 9. Collector−to−Emitter Leakage Current vs. Junction Temperature

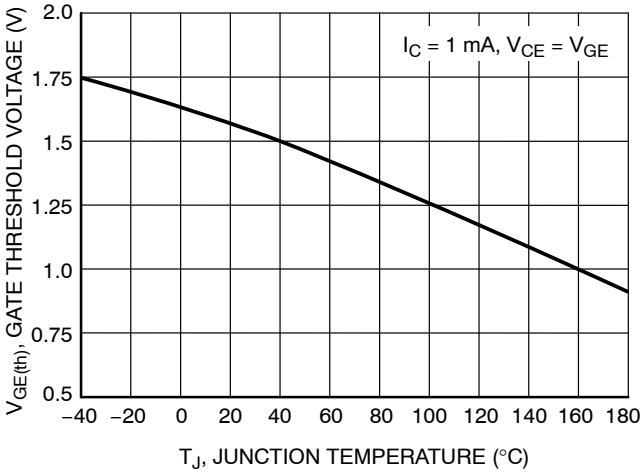


Figure 10. Gate Threshold Voltage vs. Temperature

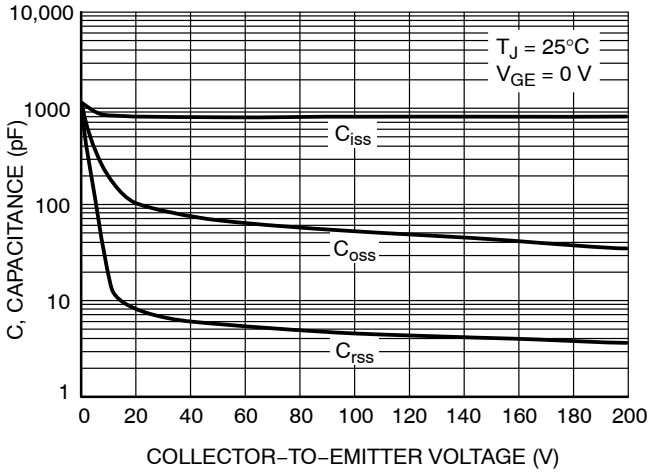


Figure 11. Capacitance Variation

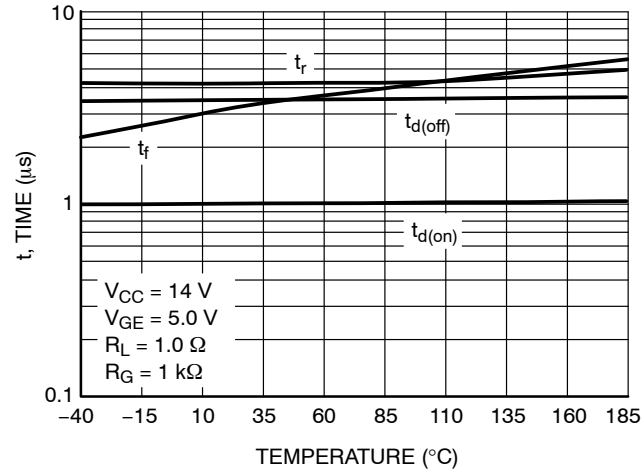


Figure 12. Resistive Switching Time Variation vs. Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

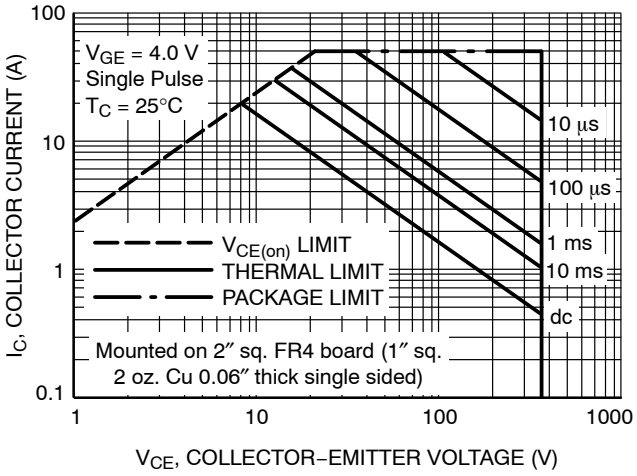


Figure 13. Forward Biased Safe Operating Area

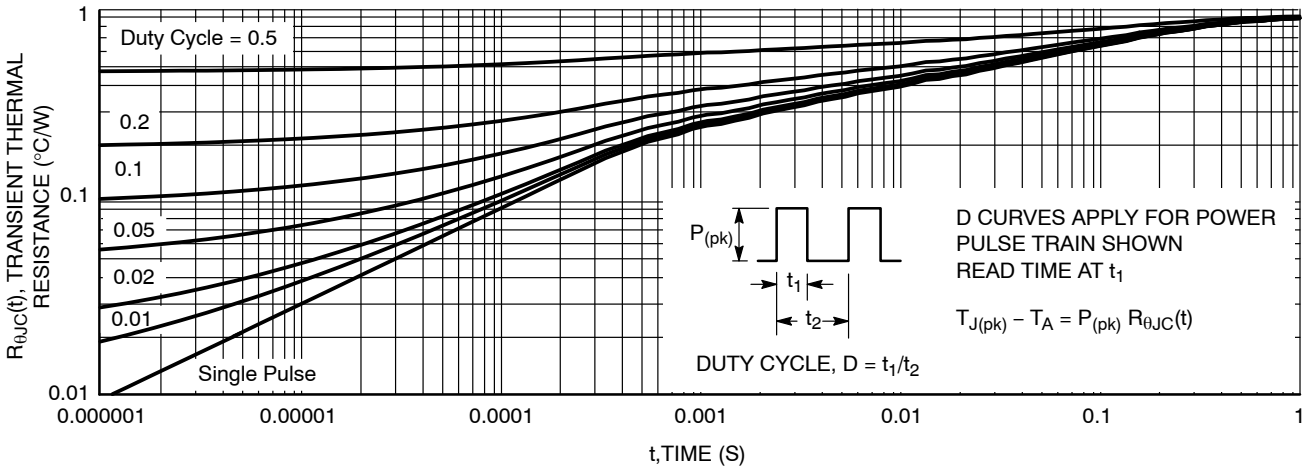
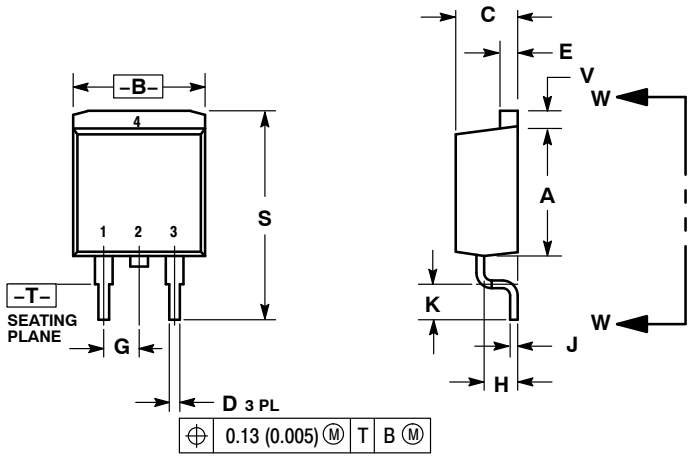


Figure 14. Best Case Transient Thermal Resistance (Non−normalized Junction−to−Case Mounted on Cold Plate)

NGB8207AN

PACKAGE DIMENSIONS

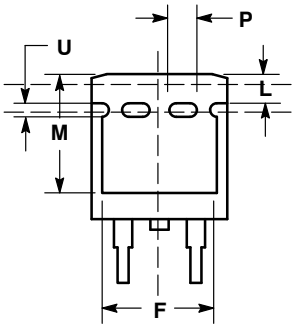
D²PAK 3
CASE 418B−04
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

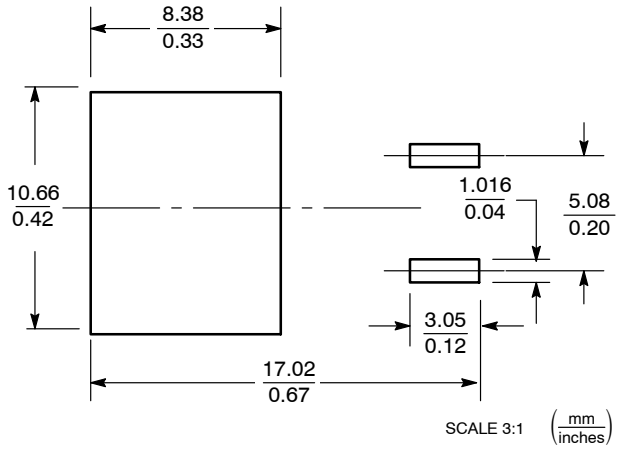
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



VIEW W−W

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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