TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel IGBT

GT8G134

Strobe Flash Applications

- Compact and Thin (TSSOP-8) package
- Enhancement-mode
- Peak collector current: I_C = 150 A (max)
  (@V_{GE}=2.5V(min))/

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	400	V
Gate-emitter voltage	DC	V_{GES}	± 4	V
	Pulse	V_{GES}	± 5	
Collector current	Pulse (Note 1)	I_{CP}	150	A
Collector power dissipation (t=10 s)	(Note 2a)	P_C (1)	1.1	W
	(Note 2b)	P_C (2)	0.6	W
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55~150	°C

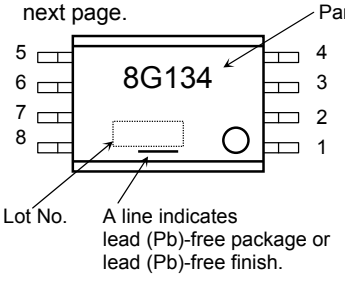
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

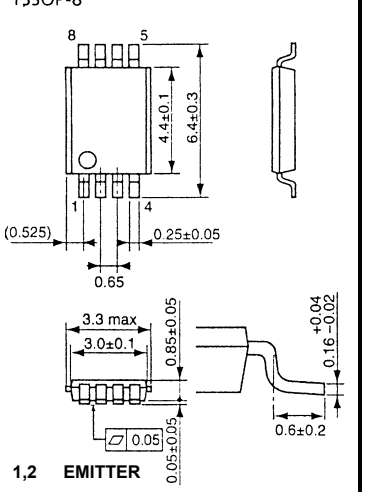
Characteristics	Symbol	Rating	Unit
Thermal resistance , junction to ambient (t = 10 s) (Note2a)	$R_{th\ (j\text{-}a)}$ (1)	114	°C/W
Thermal resistance , junction to ambient (t = 10 s) (Note2b)	$R_{th\ (j\text{-}a)}$ (2)	208	°C/W

Marking (Note 3)

Note : For (Note 1) , (Note 2a) , (Note 2b) and (Note 3) , Please refer to the next page.



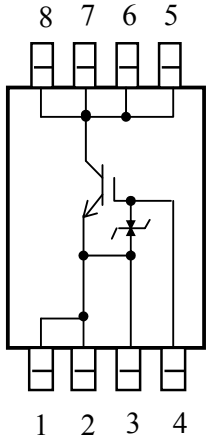
Unit: mm



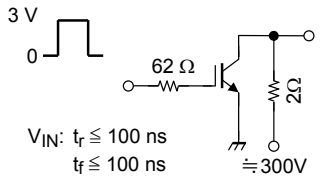
JEDEC	—
JEITA	—
TOSHIBA	—

Weight: 0.035 g (typ.)

Circuit Configuration



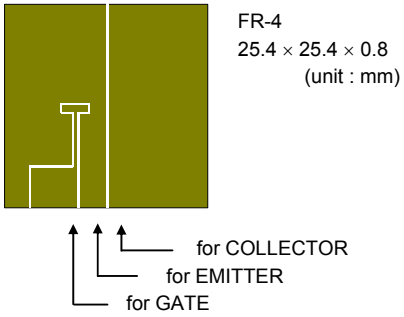
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GES}	$V_{GE} = \pm 4$ V, $V_{CE} = 0$	—	—	± 10	μA
Collector cut-off current		I_{CES}	$V_{CE} = 400$ V, $V_{GE} = 0$	—	—	10	μA
Gate-emitter cut-off voltage		$V_{GE\ (OFF)}$	$I_C = 1$ mA, $V_{CE} = 5$ V	0.65	1.0	1.35	V
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	$I_C = 150$ A, $V_{GE} = 2.5$ V	—	3.4	—	V
Input capacitance		C_{ies}	$V_{CE} = 10$ V, $V_{GE} = 0$, f = 1 MHz	—	4560	—	pF
Switching time	Rise time	t_r		—	0.6	—	μs
	Turn-on time	t_{on}		—	0.8	—	
	Fall time	t_f		—	1.2	—	
	Turn-off time	t_{off}		—	1.8	—	

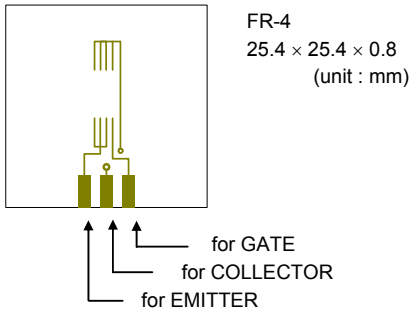
Note

Note 1: Please use devices on condition that the junction temperature is below 150°C.
Repetitive rating: pulse width limited by maximum junction temperature.

Note 2a : Device mounted on a glass-epoxy board (a)



Note 2b : Device mounted on a glass-epoxy board (b)



Note 3: ○ on lower right of the marking indicates Pin 1.

※ Weekly code: (Three digits)

□□□
Week of manufacture
(01 for first week of year, continues up to 52 or 53)
Year of manufacture
(One low-order digits of calendar year)

※ Pb-Free Finish (Only a coating lead terminal) :
It is marking about an underline to a week of manufacture mark.

□□□

Caution on handling

This device is MOS gate type. Therefore , please care of a protection from ESD in your handling .

Caution in design

You should be design dV/dt value under Icp=150A is below 400 V/μs when IGBT turn off under Ta=70℃ .
You should be design to don't flow collector current through terminal number 3 .

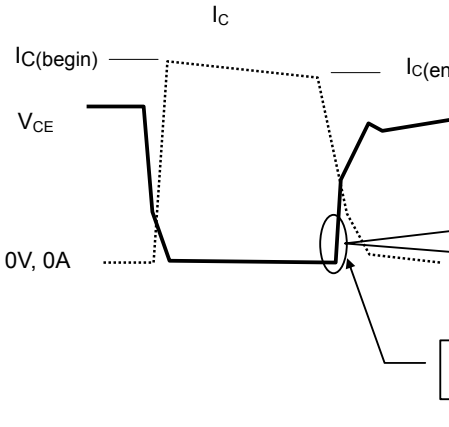
●definition of dv/dt

The slope of V_{CE} from 30v to 90v (attached figure.1)

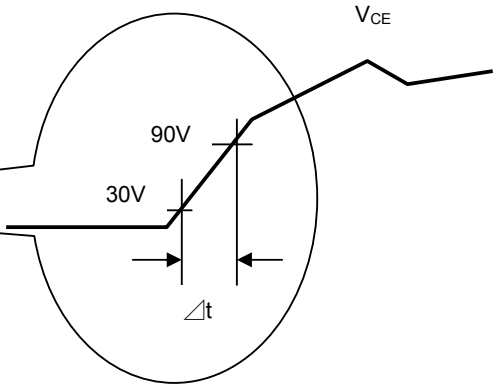
$$dv/dt = (90V-30V) / (\Delta t)$$

$$= 60V / \Delta t$$

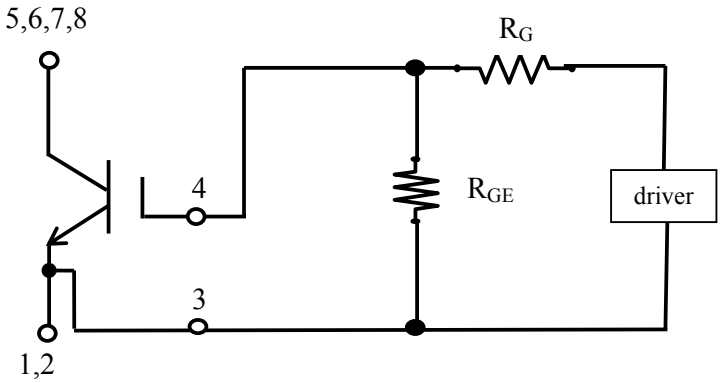
●waveform



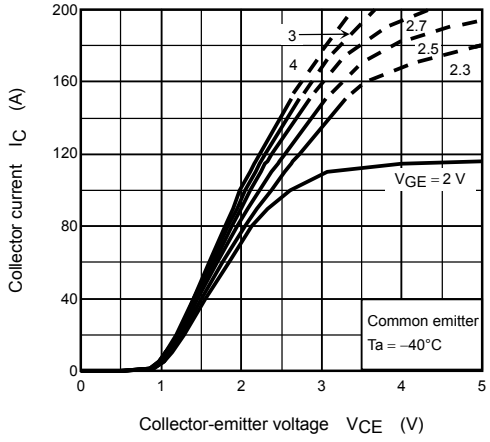
●waveform (expansion)



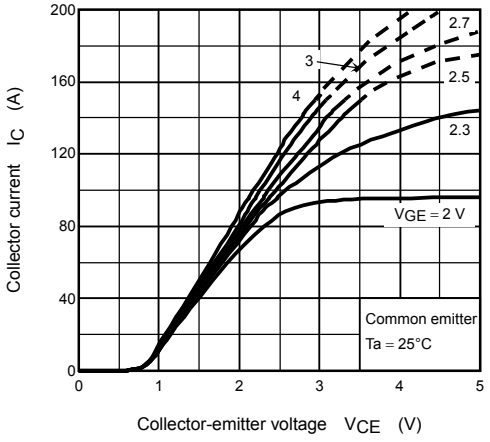
●Gate drive connection



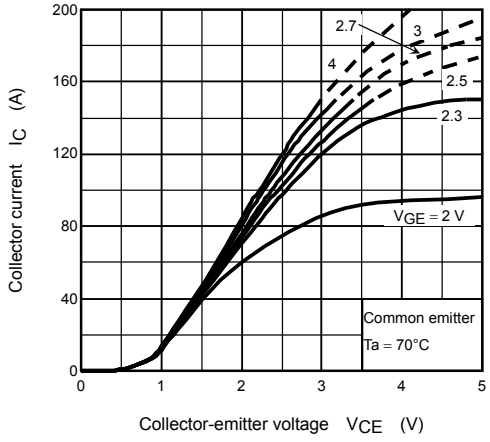
$I_C - V_{CE}$



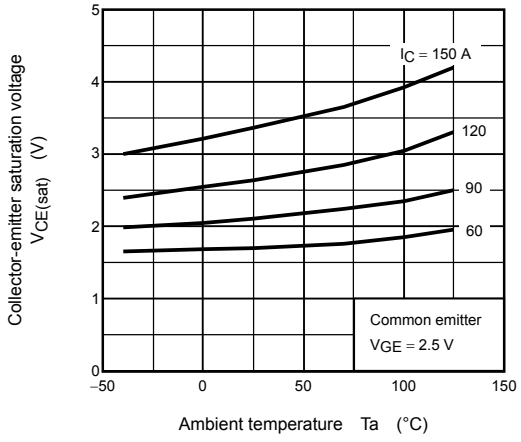
$I_C - V_{CE}$



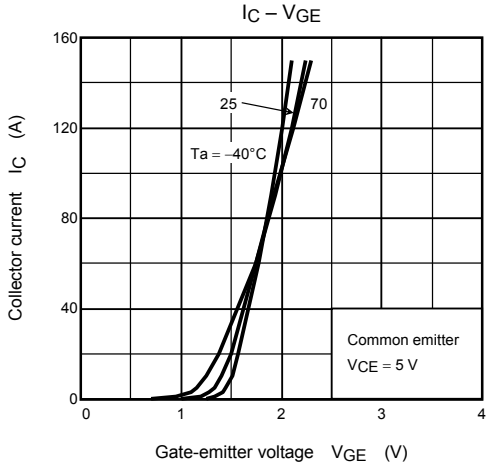
$I_C - V_{CE}$



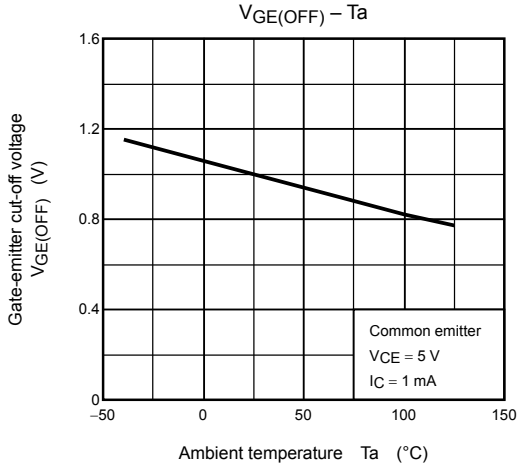
$V_{CE(sat)} - Ta$



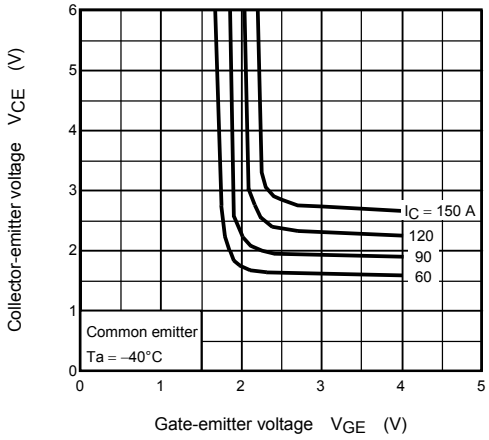
$I_C - V_{GE}$



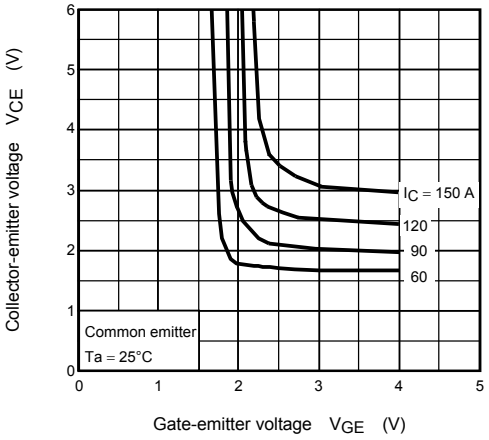
$V_{GE(OFF)} - Ta$



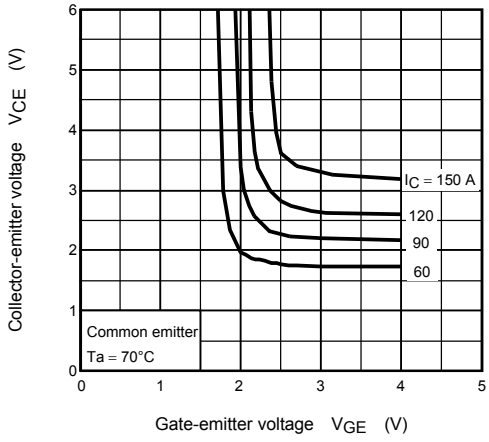
V_{CE} – V_{GE}



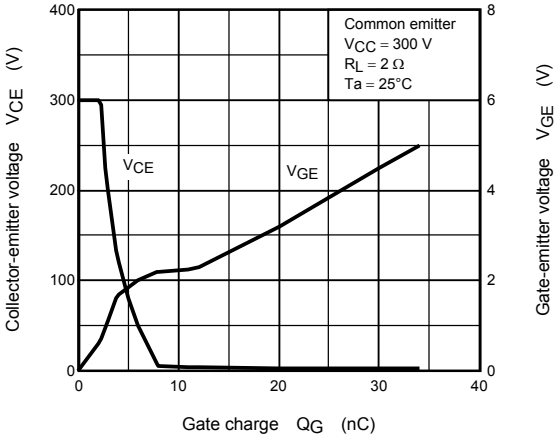
V_{CE} – V_{GE}



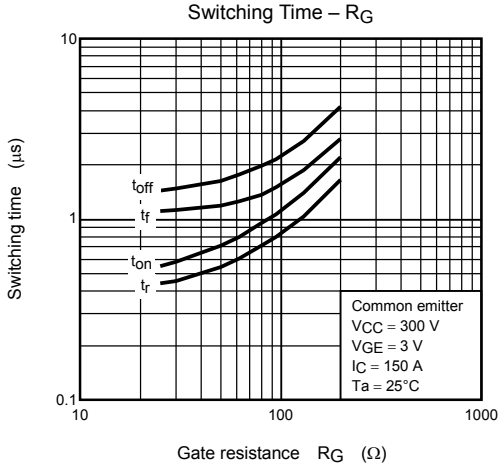
V_{CE} – V_{GE}



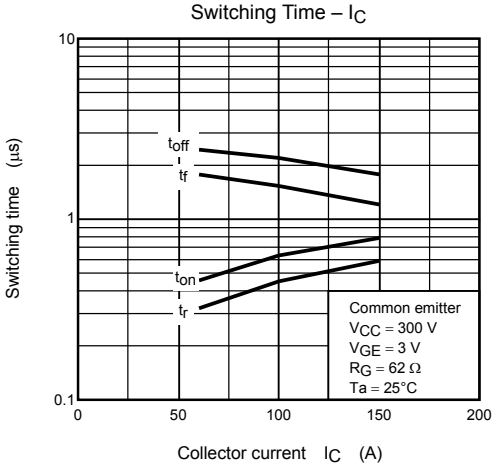
V_{CE}, V_{GE} – Q_G



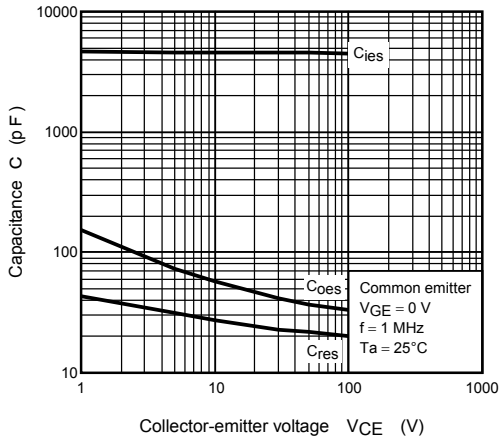
Switching Time – R_G



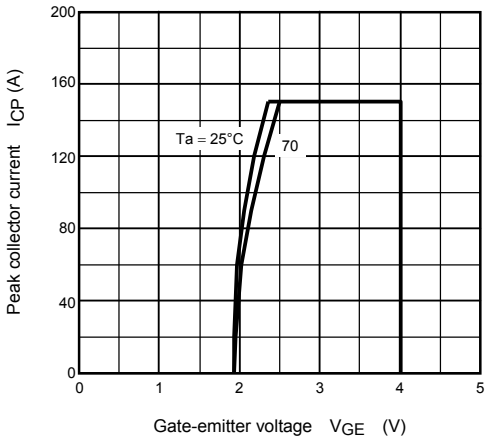
Switching Time – I_C



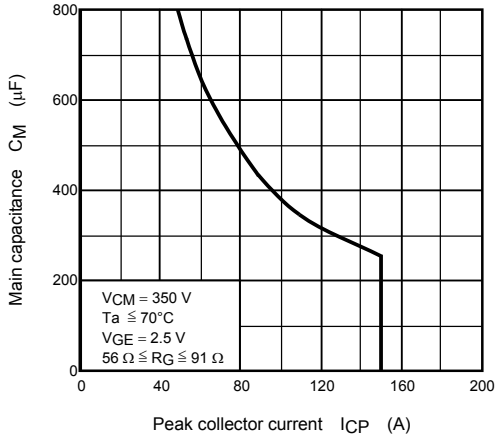
C – V_{CE}



Minimum Gate Drive Area



Maximum Operating Area



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20070701-EN

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