RICOH

Microprocessor Supervisory Circuit

R5109G SERIES

NO. EA-172-071011

OUTLINE

The R5109G Series are CMOS-based µcon supervisory circuit, or high accuracy and ultra low supply current voltage detector with built-in delay and watchdog timer. When the V_{DD} voltage is down across the threshold, or the watchdog timer does not detect the system clock from the µ con, the reset output is generated. The voltage detector circuit is used for the system reset, etc. The detector threshold is fixed internally, and the tolerance is ±1.0%. The released delay time (Power-on Reset Delay) circuit is built-in, and output delay time is adjustable with an external capacitor. When the V_{DD} supply voltage becomes higher than the released voltage, the reset state will be maintained during the delay time. The time out period of the watchdog timer can be also set with an external capacitor. The output type of the reset is selectable, Nch open-drain, or CMOS. The function to stop supervising clock by the watchdog timer (INH function) and the function to supervise two different clocks are built in this IC. The package is small SSOP-8G.

FEATURES

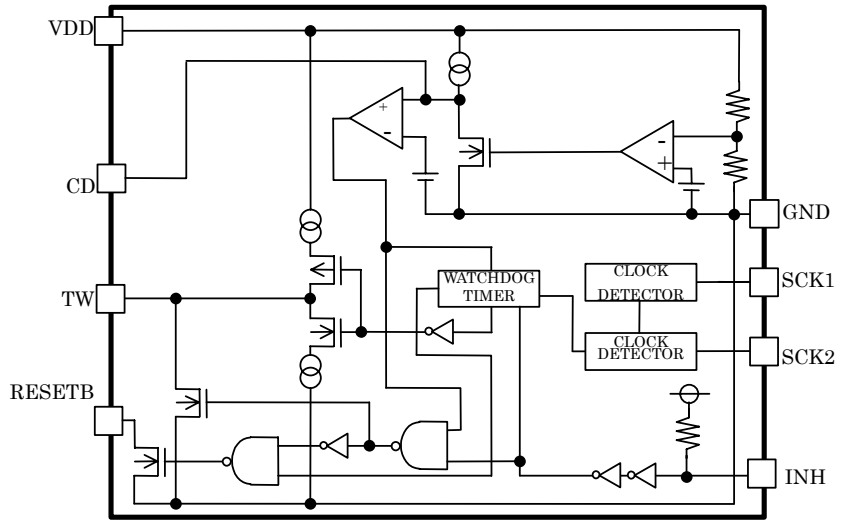
- Built-in a watchdog timer's time out period accuracy ±30%
- Timeout period for watchdog and generating a reset signal can be set by an external capacitor
- Detector Threshold Voltage ····· 0.1V stepwise setting in the range from 1.5V to 5.5V
- Supply current ····· Typ. 11.5µA
- Operating Voltage ····· 0.9V to 6.0V
- High Accuracy Output Voltage of Detector Threshold ····· ±1.0%
- Power-on Reset Delay Time accuracy····· ±20%
- Power-on reset delay time of the voltage detector can be set with an external capacitor.
- Small Package ····· SSOP-8G (0.65mm pitch)

APPLICATION

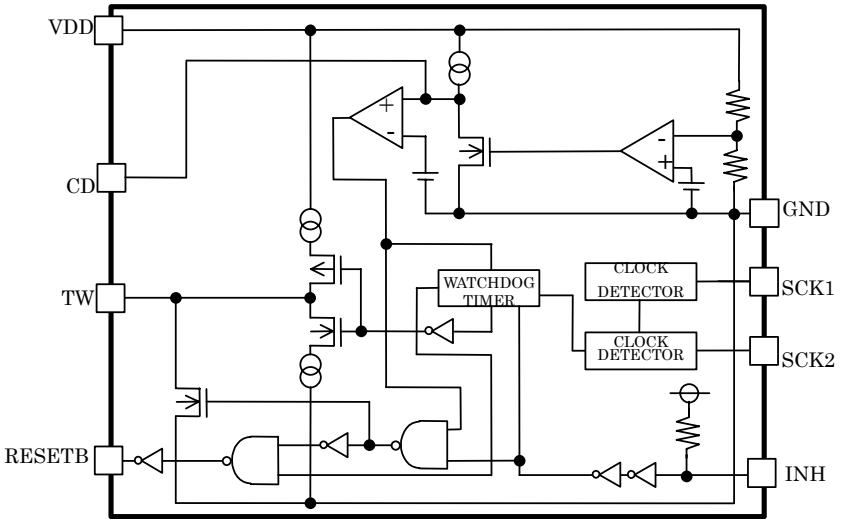
- Supervisory circuit for equipment with using microprocessors.

BLOCK DIAGRAMS

R5109Gxx1A



R5109Gxx1C



SELECTION GUIDE

The selection can be made with designating the part number as shown below:

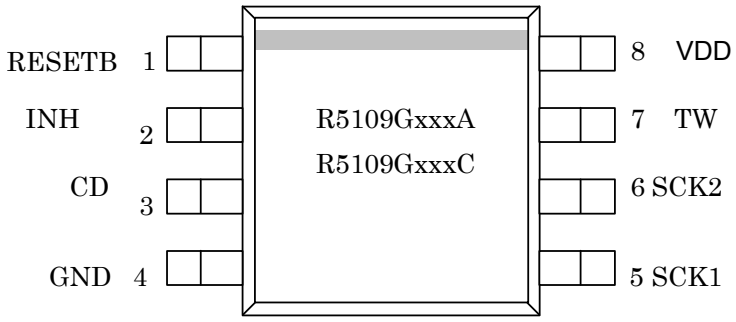
R5109Gxx1x-TR ←part Number

↑↑ ↑ ↑

ab c d

Code	Descriptions
a	Designation of Package Type; G: SSOP8G (2.9mmx4.0mm)
b	Designation of Detector Threshold Voltage (-V_{DET}) 0.1V stepwise setting is possible in the range from 1.5V to 5.5V
c	Designation of the output type of RESETB A: Nch Open-drain C: CMOS Output
d	Designation of Taping Type

PIN CONFIGURATION



SSOP8G (0.65mm pitch)

PIN DESCRIPTION

Pin No	Symbol	Pin Description
1	RESETB	Output Pin for Reset signal of Watchdog timer and Voltage Detector. (Output “L” at detecting Detector Threshold and Watchdog Timer Reset.)
2	INH	Inhibit Pin ("L": Inhibit the watchdog timer)
3	C_D	External Capacitor Pin for Setting Delay Time of Voltage Detector
4	GND	Ground Pin
5	SCK1	Clock Input Pin 1 from Microprocessor
6	SCK2	Clock Input Pin 2 from Microprocessor
7	TW	External Capacitor Pin for Setting Reset and Watchdog Timeout Periods
8	V_{DD}	Power supply Pin

ABSOLUTE MAXIMUM RATINGS

Topt=25°C, Vss=0V

Symbol	Item		Rating	Unit
V_{IN}	Supply Voltage		-0.3~7.0	V
V_{CD}	Output Voltage	Voltage of C_D Pin	-0.3~V_{IN}+0.3	V
V_{TW}		Voltage of TW Pin	-0.3~V_{IN}+0.3	V
V_{RESETB}		Voltage of RESETB Pin	-0.3~7.0	V
VSCK	Input Voltage	Voltage of SCK1, SCK2 Pin	-0.3~7.0	V
V_{INH}		Voltage of INH Pin	-0.3~7.0	V
I_{RESETB}	Output Current	Current of RESETB Pin	20	mA
P_D	Power Dissipation		300	mW
Topt	Operating Temperature Range		-40~+105	°C
Tstg	Storage Temperature Range		-55~+125	°C

ELECTRICAL CHARACTERISTICS

R5109GxxxA/C Unless otherwise specified, V_{IN}=6.0V, C_{TW}=0.1uF, C_D=0.1uF, Rpull-up=100kΩ(R5109GxxxA)

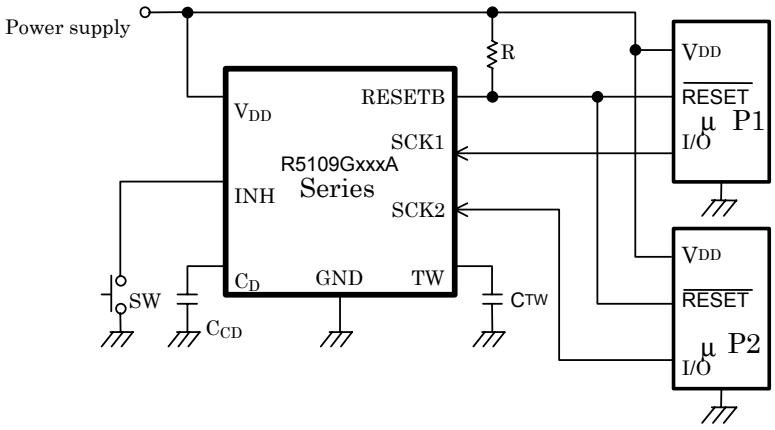
The number of Bold font applied to the temperature range from -40°C to 105°C (Topt=25°C)

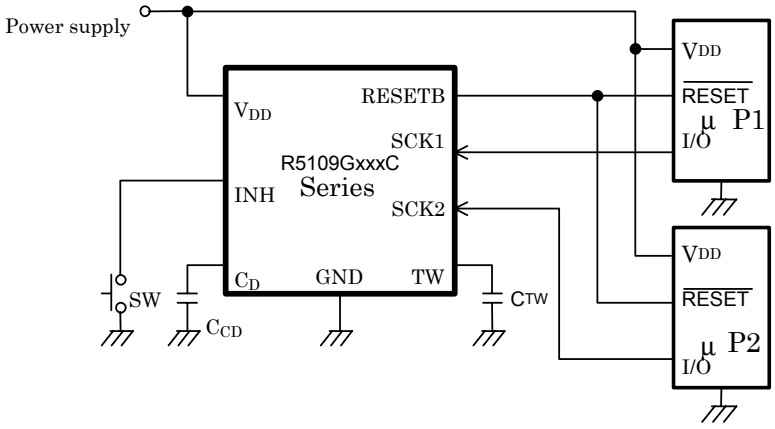
Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Voltage		**0.9**		**6.0**	V
Iss	Supply Current	V_{IN}=(-V_{DET})+0.5V Clock Pulse Input		11.5	**15.5**	µA
Voltage Detector						
-VDET	Detector Threshold	SENSE pin Threshold	x0.990 **x0.972**		x1.010 **x1.015**	V
Δ-V_{DET}/ ΔTopt	Detector Threshold Temperature Coefficient	-40°C≤Topt≤105°C		±100		ppm/ °C
V_{HYS}	Detector Threshold Hysteresis		**(-V_{DET}) x0.03**	(-V_{DET}) x0.05	**(-V_{DET})x 0.07**	V
t_{pLH}	Output Delay Time	C_D=0.1µF	**340**	370	**467**	ms
V_{INL}	Minimum Operating Voltage	RESETB≤0.1V, pull-up=100kΩ		0.6	0.9	V
I_{DOUTN}	Output Current (RESETB Output pin)	Nch, V_{DD}=1.2V, V_{DS}=0.1V	**0.38**	0.80		mA
I_{DOUTP}	Output Current (RESETB Output pin)	Nch, V_{DD}=6.0V, V_{DS}=0.5V(R5108GxxxC)	**0.65**	0.90		mA
Watchdog Timer						
T_{WD}	Watchdog Timeout period	C_{TW}=0.1uF	**230**	310	**450**	ms
T_{WR}	Reset Hold Time of WDT	C_{TW}=0.1uF	**29**	34	**48**	ms
V_{SCKH}	SCK Input "H"	SCK1, SCK2	**V_{IN}x0.8**		**6.0**	V
V_{SCKL}	SCK Input "L"	SCK1, SCK2	**0.0**		**V_{IN}x0.**2	V
V_{INHH}	INH Input "H"		**1.0**		**6.0**	V
V_{INHL}	INH Input "L"		**0.00**		**0.35**	V

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
R_{INH}	INH pull-up Resistance		**60**	110	**164**	kΩ
T_{SCKW}	SCK Input Pulse Width	V_{SCKL}=V_{IN}x0.2, V_{SCKH}=V_{IN}x0.8	**500**			ns

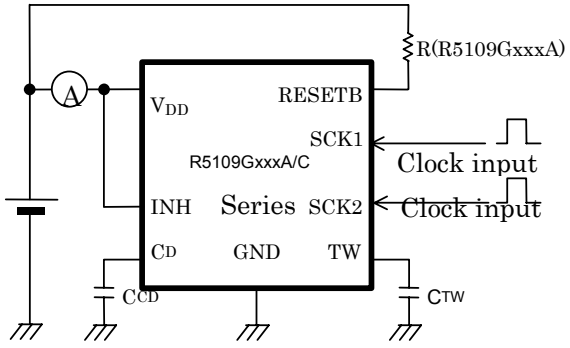
*Bold Type value is guaranteed by design.

TYPICAL APPLICATIONS





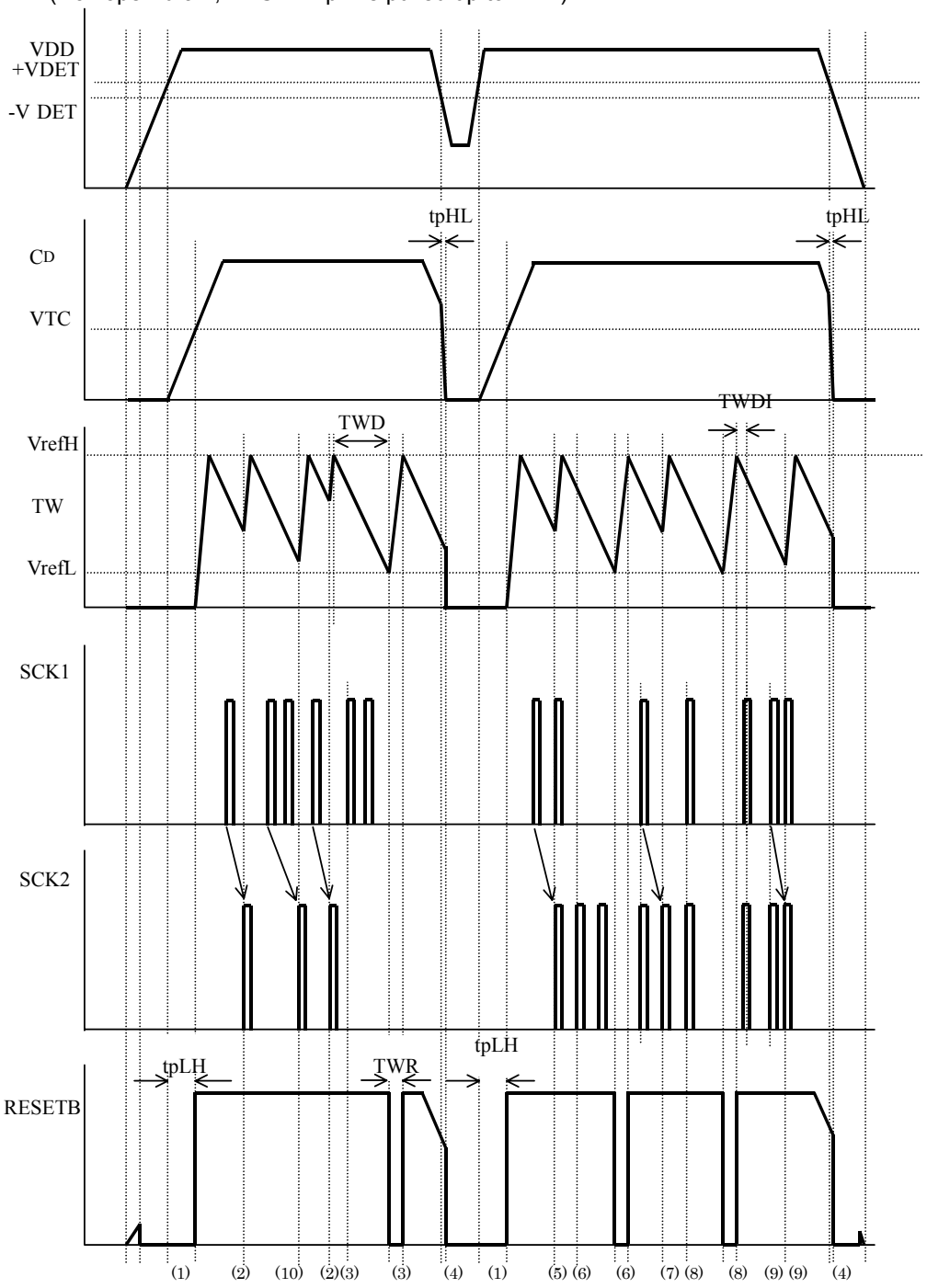
TEST CIRCUIT



Supply Current Test Circuit

TIMING DIAGRAM (R5109GxxxA/R5109GxxxC)

(Nch open-drain, RESETB pin is pulled up to V_{DD}.)



OPERATION

① When the VDD pin voltage becomes more than the released voltage (+V_{DET}), after the released delay time (or the power on reset time tpLH), the output of RESETB becomes “H” level.

② After the SCK1 pulse is input, when the SCK2 is input, the watchdog timer is cleared, and TW pin mode changes from discharge mode to charge mode. When the TW pin voltage becomes higher than VREFH, the mode will change into discharge, and next watchdog time count starts.

③ After the SCK1 pulse is input, unless the SCK2 pulse is input, WDT will not be cleared, and during the charging period of TW pin, RESETB="L".

④ When the VDD pin becomes lower than the detector threshold voltage, RESETB outputs "L".

⑤ After the SCK1 pulse is input, when the SCK2 is input, the WDT will be cleared.

⑥ Without the input of SCK1 pulse input, even if the SCK2 pulse is input, the WDT will not be cleared.

⑦ After the SCK1 pulse is input, when the SCK2 is input, the WDT will be cleared.

⑧ If SCK1 pulse and SCK2 pulse are input at the same time, the WDT will not be cleared.

⑨ After the SCK1 pulse is input, when the SCK2 is input, the WDT will be cleared.

⑩ The WDT supervises SCK1 pulse and SCK2 pulse by turns, therefore, for example, if only SCK1 pulse is input twice or more without SCK2 pulse, the second or later consecutive SCK1 pulse will be ignored. After the SCK1 pulse is input, and when the SCK2 pulse is input, the WDT will be cleared. In the same way, if only SCK2 pulse is input twice or more without SCK1 pulse, the second or later consecutive SCK2 pulse will be ignored.

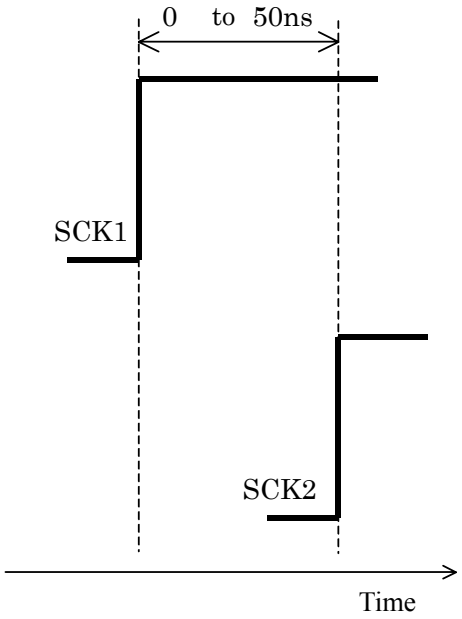
Too close timing of SCK1 pulse input and SCK2 pulse input means the rising edge interval time range from 0ns to 50ns. (Guaranteed by design, not mass production tested.)

Even if the SCK1 and SCK2 are input at almost the same time as above, the WDT will still try to supervise these two clock by turns.

Therefore, after the SCK1 pulse is input, if SCK1 pulse and SCK2 pulse are input at almost the same time, the WDT will be cleared. (as the status ⑤)

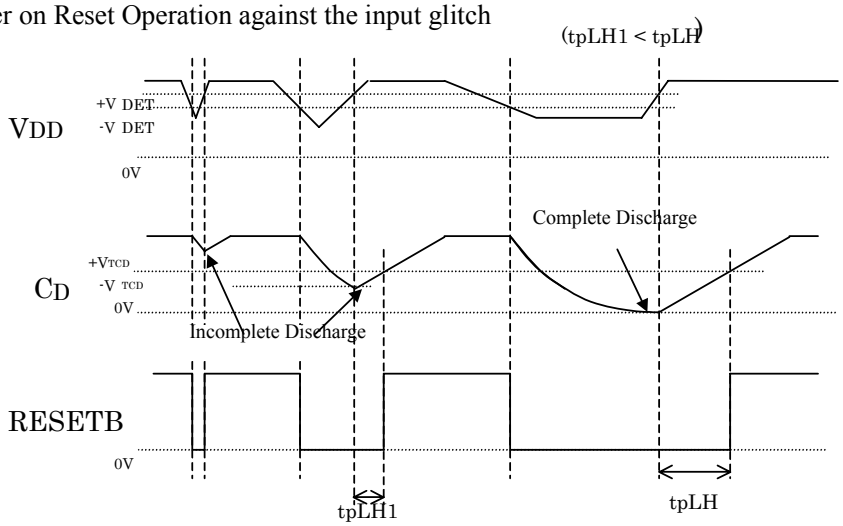
Likewise, after the SCK1 pulse and SCK2 pulse are input at almost the same time, when the SCK2 pulse is input, the WDT will be cleared. (as the status ⑦)

If the almost same timing input of SCK1 and SCK2 continues twice, the WDT will be cleared. (as the status ⑨)



Example timing of too close input pulses (This pattern will be recognized the clock timing is same by the WDT)

Power on Reset Operation against the input glitch



* Watchdog Timeout period/Reset hold time

The watchdog timeout period and reset hold time can be set with an external capacitor to TW pin.

The next equations describe the relation between the watchdog timeout period and the external capacitor value, or the reset holding time and the external capacitor value.

$t_{WD(s)} = 3.1*10^{6} \times C\,(F)$

tWR(s)=tWD/9

The watchdog timer (WDT) timeout period is determined with the discharge time of the external capacitor.

During the watchdog timeout period, if the clock pulse from the system is detected, WDT is cleared and the

capacitor is charged. When the charge of the capacitor completes, another watchdog timeout period starts again. During the watchdog timeout period, if the clock pulse from the system is not detected, during the next reset hold time RESETB pin outputs "L".

After starting the watchdog timeout period, (just after from the discharge of the external capacitor) even if the clock pulse is input during the time period "TWDI", the clock pulse is ignored.
TWDI[s]=TWD/10

Released Delay Time (Power-on Reset delay time)
The released delay time can be set with an external capacitor connected to the CD pin. The next equation describes the relation between the capacitance value and the released delay time (tpLH).
$tpLH(s)=3.7\times10^{6}\times C(F)$
Note that the temperature dependence graph in the typical characteristics does not contain the temperature characteristics of the external capacitor.

When the V_{DD} voltage becomes equal or less than ($-V_{DET}$), discharge of an external capacitor connected to the CD pin starts. In case that the discharge is not enough, if the V_{DD} voltage returns equal or more than ($+V_{DET}$), the delay time as tpLH will be shorter than expected.

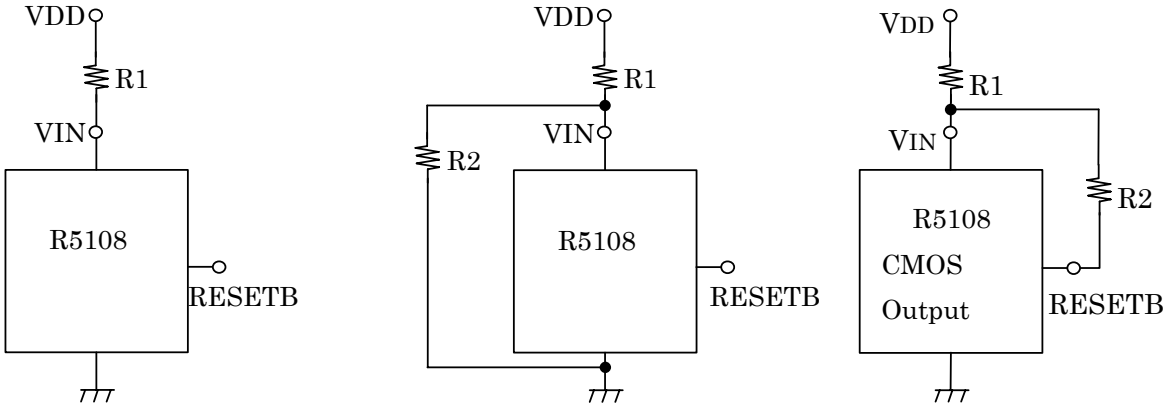
Minimum Operating Voltage (VINL)
We specified the minimum operating voltage as the minimum input voltage in which the condition of RESETB pin being 0.1V or lower than 0.1V. (Herein, pull-up resistance is set as 100kΩ in the case of the Nch open-drain output type.

Inhibit (INH) Function
If INH pin is set at "L", the watchdog timer stops monitoring the clock, and the RESETB output will be dominant by the voltage detector's operation. Therefore, if the equal or more than the detector threshold level is input, RESETB outputs "H" regardless the clock pulse. INH pin is pulled up with a resistor (TYP. 110kΩ) internally.

RESETB Output
RESETB pin's output type is selectable either the Nch open-drain output or CMOS output. If the Nch open-drain type output is selected, the RESETB pin is pulled up with an external resistor to an appropriate voltage source.

Clock Pulse Input
Built-in watchdog timer is cleared with the SCK clock pulse within the watchdog timeout period.
After the SCK1 clock pulse is input, when the SCK2 pulse is input, the watchdog timer will be cleared. If the system requires only one clock supervise, SCK1pin and SCK2pin must connect each other. In this case, the watchdog timer is cleared with every other clock pulse. Depending on the timing of these two clock pulses, SCK1 pulse and SCK2 pulse are recognized at almost the same time by the watchdog timer, during the watchdog timeout period, after the SCK1 clock pulse, two or more SCK2 clock pulses are desirable to put into.

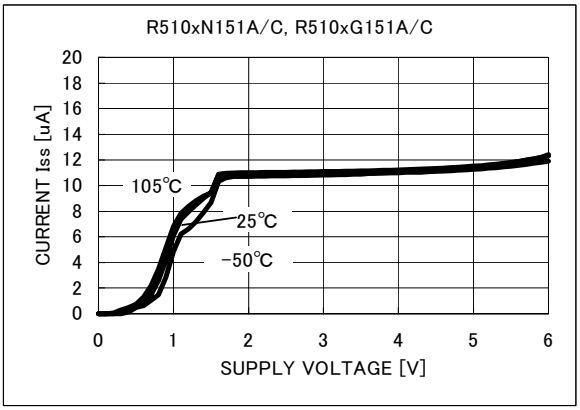
APPLICATION NOTES
If a resistor is connected to the VDD pin, the operation might be unstable with the supply current of IC itself.

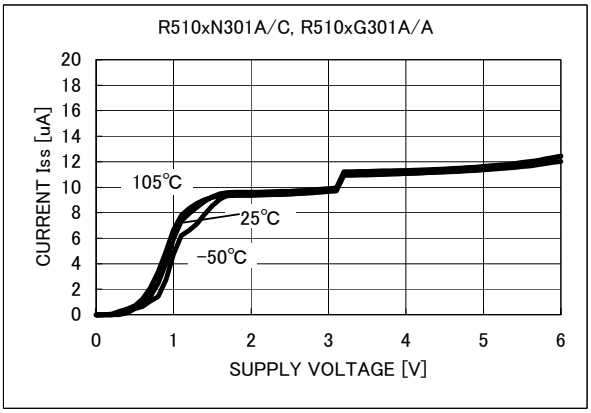


Connection examples affected by the conduction current

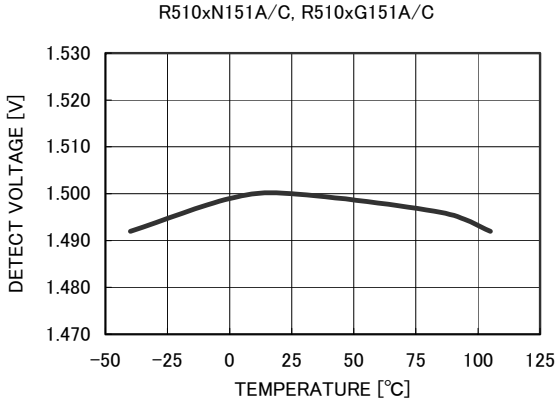
TYPICAL CHARACTERISTICS

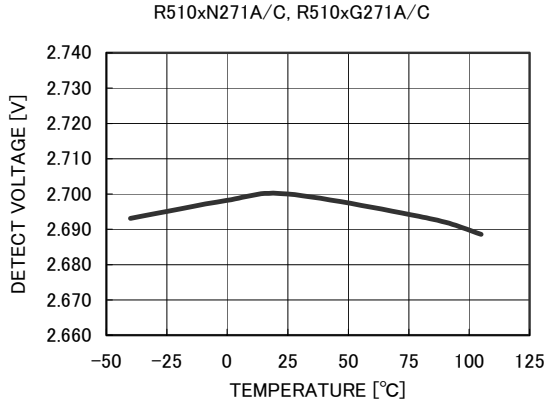
1) Supply Current vs. Input Voltage



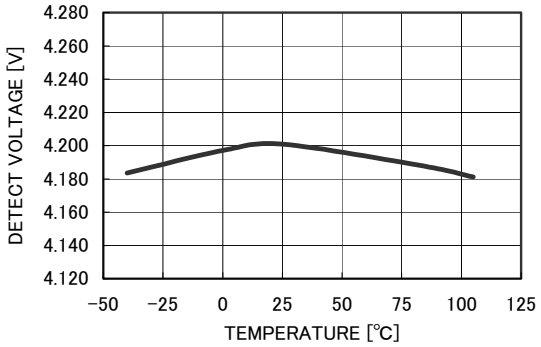


2) Detector Threshold vs. Temperature



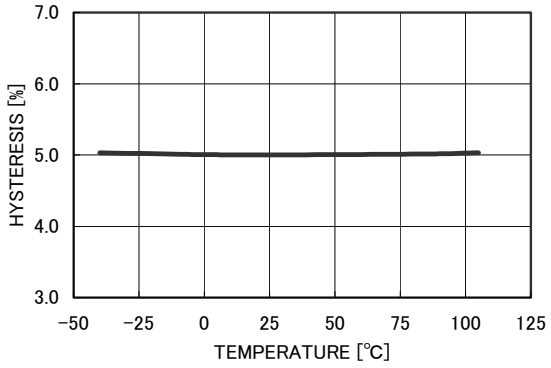


R510xN421A/C R510xG421A/C

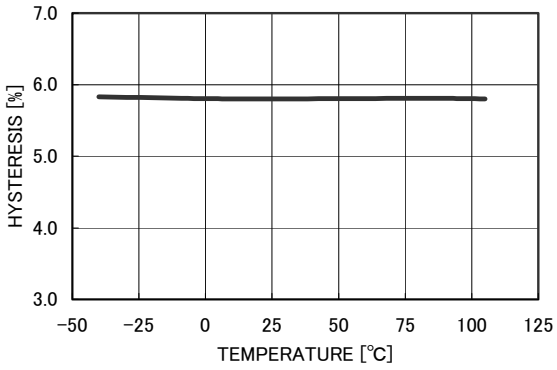


3) Detector Threshold Hysteresis vs. Temperature

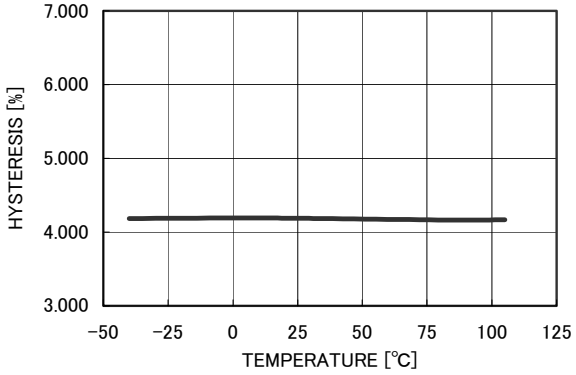
R510xN151A/C R510xG151A/C



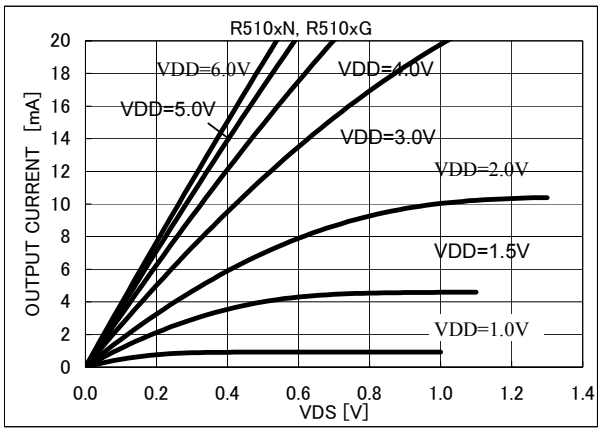
R510xN271A/C R510xG271A/C



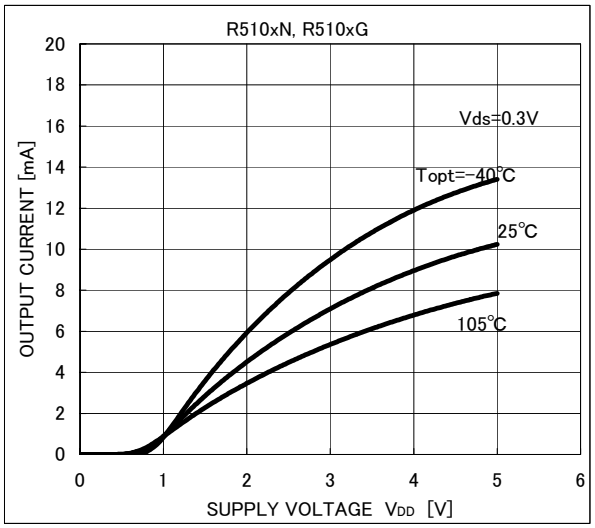
R510xN421A/C R510xG421A/C

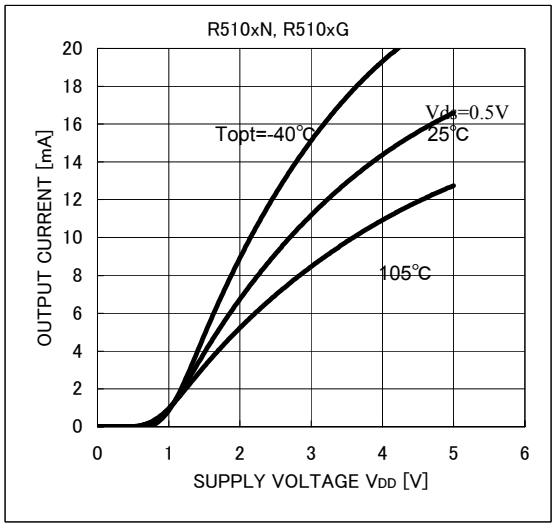


4) Nch Driver Output Current vs. VDS Topt=25°C

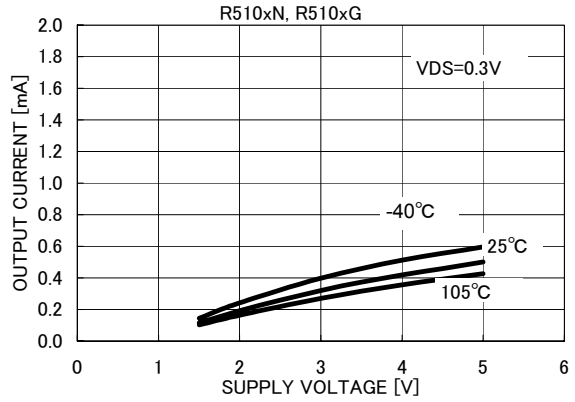


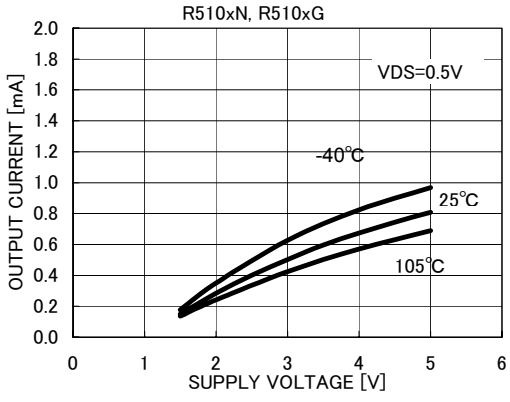
5) Nch Driver Output Current vs. VDD

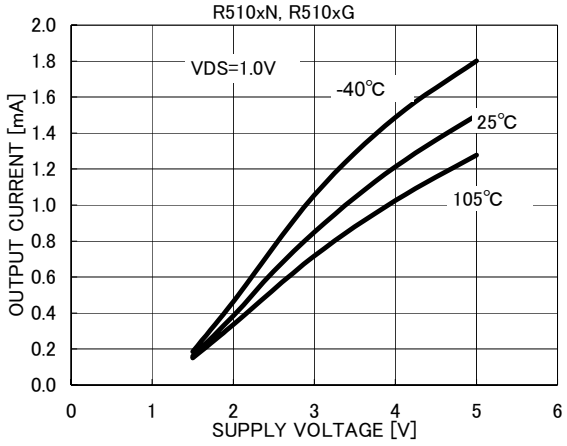




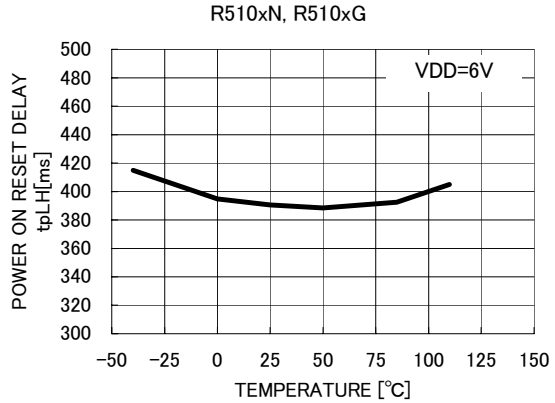
6) Pch Driver Output Current vs. VDD



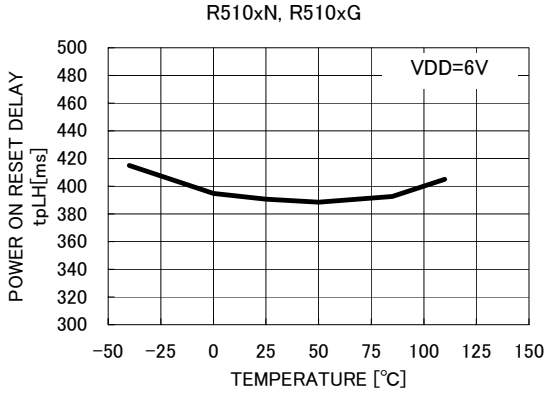




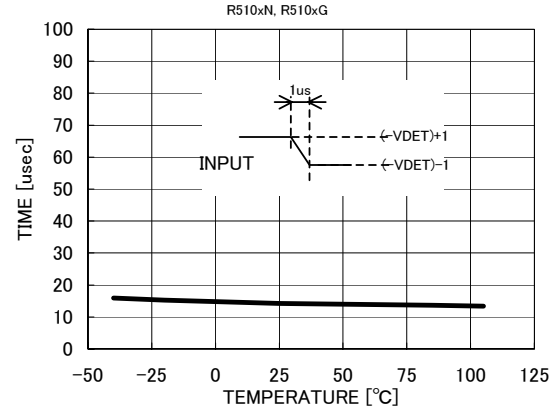
7) Released Delay Time vs. Input Voltage



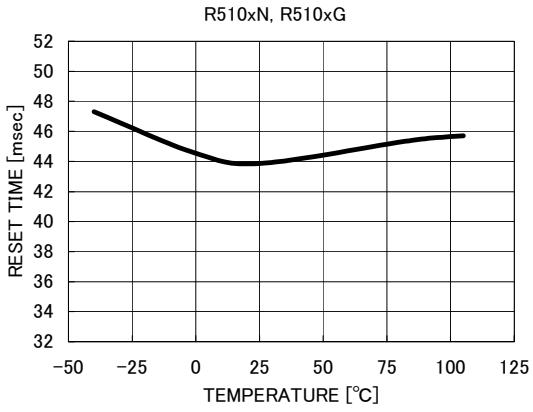
8) Released Delay Time vs. Temperature



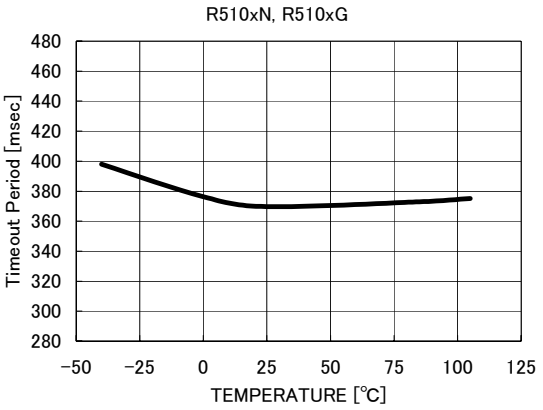
9) Detector Output Delay Time vs. Temperature



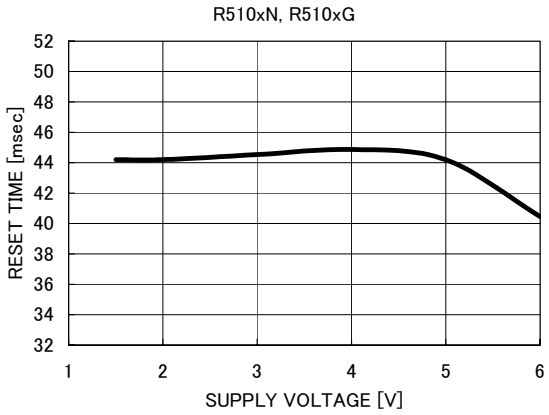
10) WDT Reset Timer vs. Temperature



11) WDT Timeout Period vs. Temperature



12) WDT Reset Timer vs. Input Voltage



13) WDT Timeout Period vs. Input Voltage