RICOH

Microprocessor Supervisory Circuit

R5105N SERIES

NO. EA-159-070908

OUTLINE

The R5105N Series are CMOS-based µ con supervisory circuit, or high accuracy and ultra low supply current voltage detector with built-in delay circuit and watchdog timer. When the supply voltage is down across the threshold, or the watchdog timer does not detect the system clock from the µ con, the reset output is generated. The voltage detector circuit is used for the system reset, etc. The detector threshold is fixed internally, and the tolerance is ±1.0%. The released delay time (Power-on Reset Delay) circuit is built-in, and output delay time is adjustable with an external capacitor. When the supply voltage becomes the released voltage, the reset state will be maintained during the delay time. The time out period of the watchdog timer can be also set with an external capacitor. The output type of the reset is selectable, Nch open-drain, or CMOS. The package is small SOT-23-6.

FEATURES

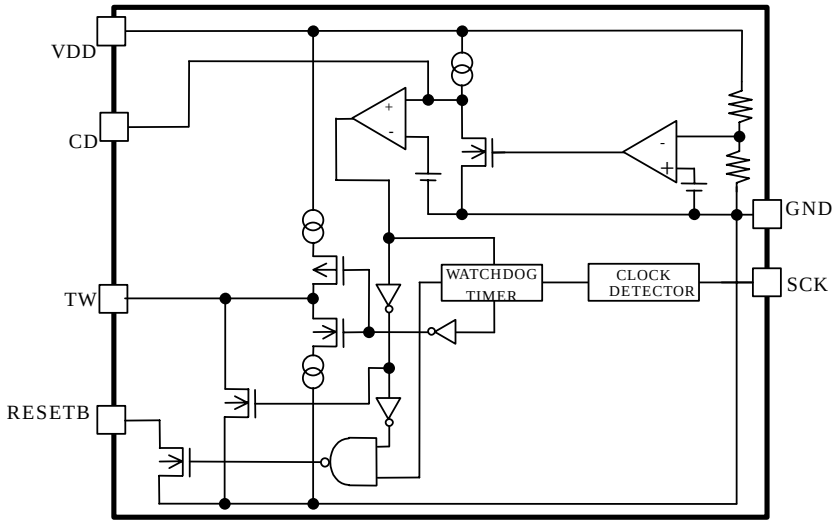
- Built-in a watchdog timer's time out period accuracy ±30%
- Timeout period for watchdog and generating a reset signal can be set by an external capacitor
- Detector Threshold Voltage ····· 0.1V stepwise setting in the range from 1.5V to 5.5V
- Supply current ····· Typ. 11µA
- Operating Voltage ····· 0.9V to 6.0V
- High Accuracy Output Voltage of Detector Threshold ····· ±1.0%
- Power-on Reset Delay Time accuracy····· ±20%
- Power-on reset delay time of the voltage detector can be set with an external capacitor.
- Small Package ····· SOT-23-6

APPLICATION

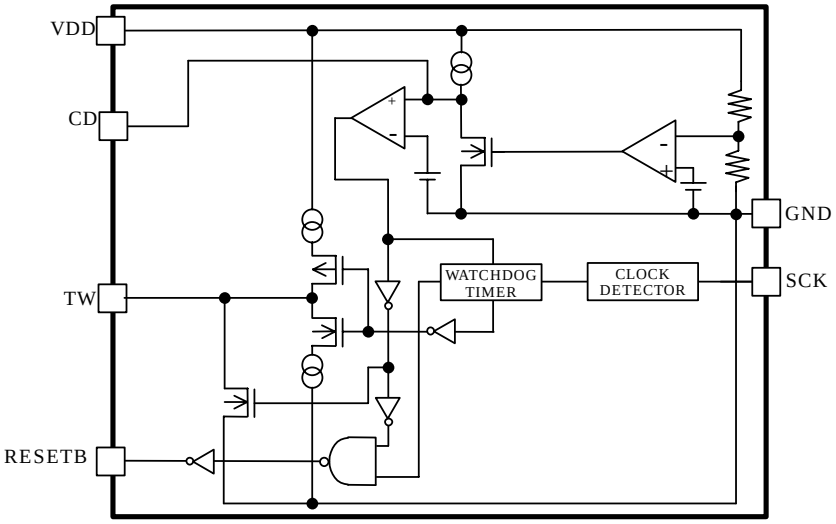
- Supervisory circuit for equipment with using microprocessors.

BLOCK DIAGRAMS

R5105Nxx1A



R5105Nxx1C



SELECTION GUIDE

The selection can be made with designating the part number as shown below:

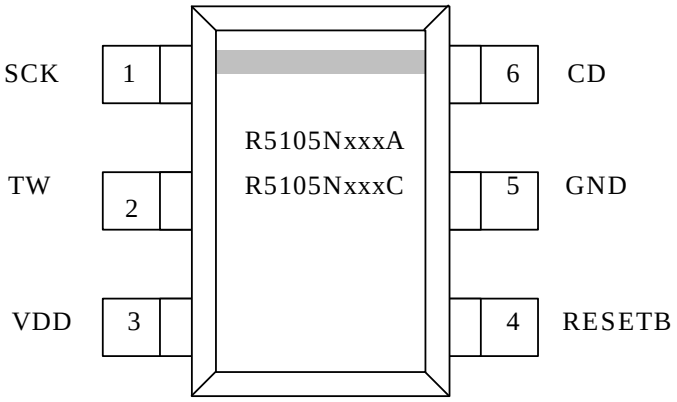
R5105Nxx1x-TR ←part Number

↑ ↑↑ ↑

a b c d

Code	Descriptions
a	Designation of Package Type; N: SOT-23-6 (2.8mmx2.9mm)
b	Designation of Detector Threshold Voltage (-V_{DET}) 0.1V stepwise setting is possible in the range from 1.5V to 5.5V
c	Designation of the output type of RESETB A: Nch open-drain output C: CMOS output
d	Designation of Taping Type

PIN CONFIGURATION



SOT-23-6

PIN DESCRIPTION

Pin No	Symbol	Pin Description
1	SCK	Clock Input Pin from Microprocessor
2	TW	External Capacitor Pin for setting Reset and Watchdog Timer Timeout Period
3	V_{DD}	Power supply Pin
4	RESETB	Output Pin for Reset signal of Watchdog timer and Voltage Detector. (Output “L” at detecting Detector Threshold and Watchdog Timer Reset.)
5	GND	Ground Pin
6	CD	External Capacitor Pin for Setting delay time of Voltage Detector

ABSOLUTE MAXIMUM RATINGS

Topt=25°C, Vss=0V

Symbol	Item		Rating	Unit
V_{IN}	Supply Voltage		-0.3~7.0	V
V_{CT}	Output Voltage	Voltage of C_D Pin	-0.3~V_{IN}+0.3	V
V_{TW}		Voltage of TW Pin	-0.3~V_{IN}+0.3	V
V_{RESETB}		Voltage of RESETB Pin	-0.3~7.0	V
VSCK	Input Voltage	Voltage of SCK Pin	-0.3~7.0	V
I_{RESETB}	Output Current	Current of RESETB Pin	20	mA
P_D	Power Dissipation		250	mW
Topt	Operating Temperature Range		-40~+105	°C
Tstg	Storage Temperature Range		-55~+125	°C

ELECTRICAL CHARACTERISTICS

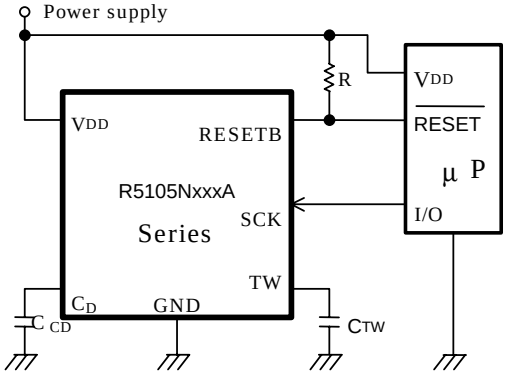
R5105NxxxA/C Unless otherwise specified, V_{IN}=6.0V, C_T=0.1uF, Rpull-up=100kΩ Topt=25°C

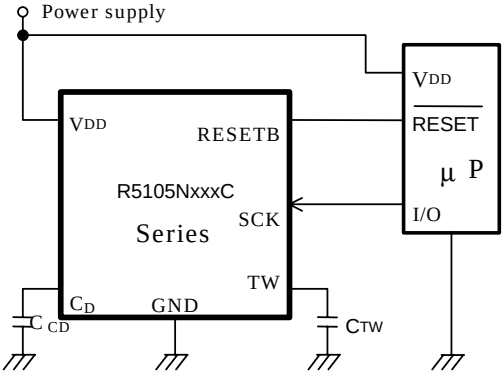
The number written in bold font is applied to the temperature range from -40°C to 105°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Voltage		**0.9**		**6.0**	V
Iss	Supply Current	V_{IN}=(-V_{DET})+0.5V Clock pulse input		11	**15**	µA
		Voltage Detector				
-VDET	Detector Threshold	V_{IN} pin Threshold	x0.990 **x0.972**		x1.010 **x1.015**	V
Δ-V_{DET}/ ΔTopt	Detector Threshold Temperature Coefficient	-40°C≤Topt≤105°C		±100		ppm/ °C
V_{HYS}	Detector Threshold Hysteresis		**(-V_{DET}) x0.03**	(-V_{DET}) x0.05	**(-V_{DET}) x0.07**	V
tp_{LH}	Output Delay Time	C_D=0.1µF	**340**	370	**467**	ms
I_{DOUTN}	Output Current (RESETB Output pin)	Nch, V_{DD}=1.2V, V_{DS}=0.1V	**0.38**	0.80		mA
I_{DOUTP}	Output Current (RESETB Output pin)	Pch, V_{DD}=6.0V, V_{DS}=0.5V (R5105NxxxC)	**0.65**	0.90		mA
		Watchdog Timer				
T_{WD}	Watchdog Timeout period	C_{TW}=0.1uF	**230**	310	**450**	ms
T_{WR}	Reset Hold Time of WDT	C_{TW}=0.1uF	**29**	34	**48**	ms
V_{SCKH}	SCK Input "H"		**V_{IN}x0.8**		**6.0**	V
V_{SCKL}	SCK Input "L"		**0.0**		**V_{IN}x0.2**	V
T_{SCKW}	SCK Input Pulse Width	V_{SCKL}=V_{IN}x0.2, V_{SCKH}=V_{IN}x0.8	**500**			ns

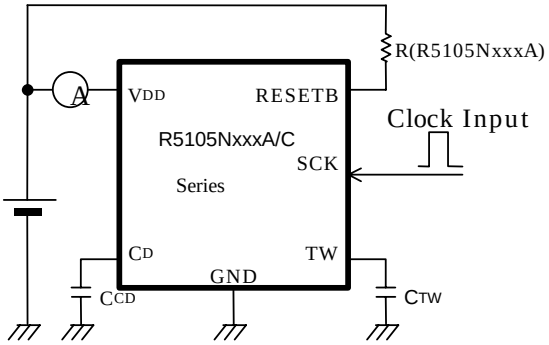
Bold type values are guaranteed by design.

TYPICAL APPLICATIONS





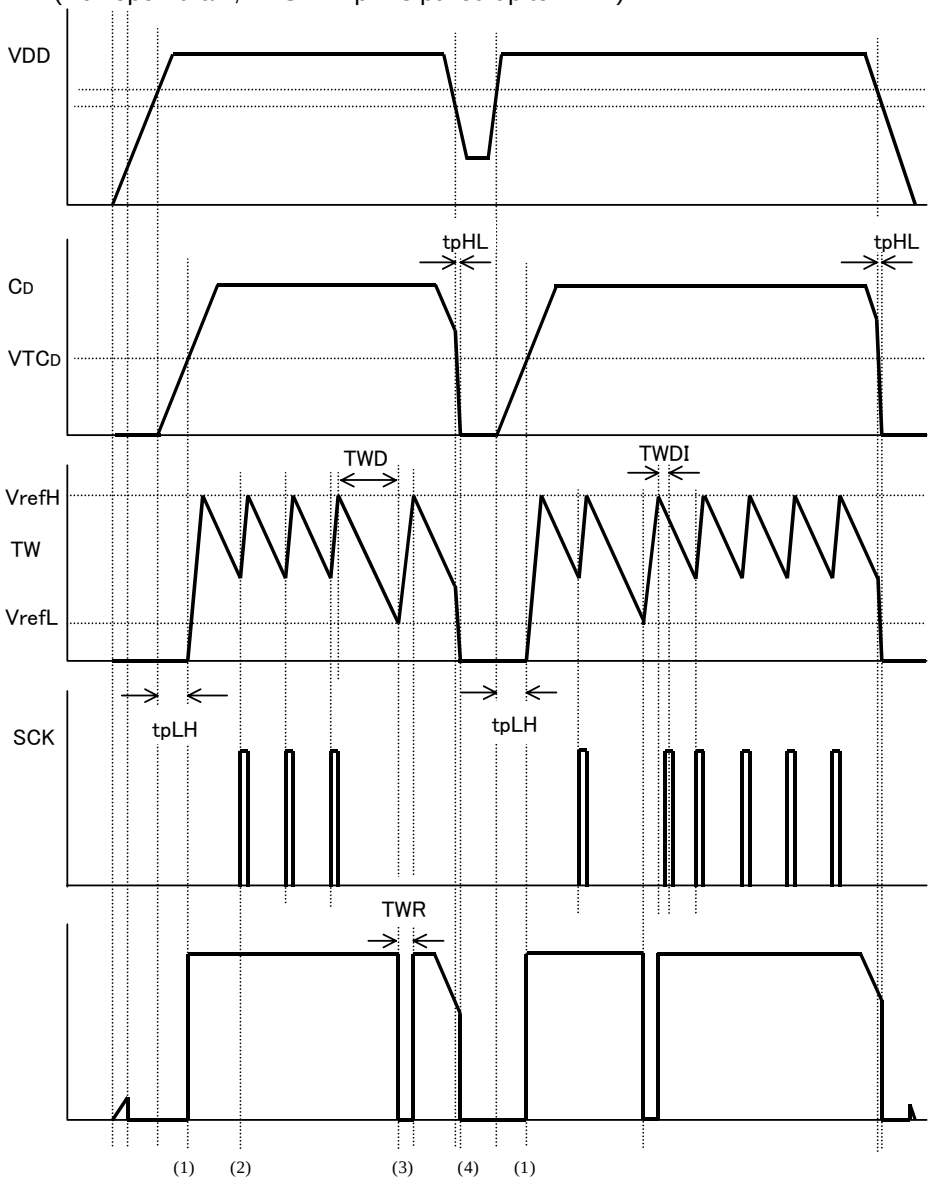
TEST CIRCUIT



Supply Current Test Circuit

TIMING DIAGRAM (R5105NxxxA/R5105NxxxC)

(Nch open-drain, RESETB pin is pulled up to VDD.)



OPERATION

① When the power supply, V_{IN} pin voltage becomes more than the released voltage ($+V_{DET}$), after the released delay time (or the power on reset time tpLH), the output of RESETB becomes “H” level.

② When the SCK pulse is input, the watchdog timer is cleared, and TW pin mode changes from the discharge mode to the charge mode. When the TW pin voltage becomes higher than VREFH, the mode will change into the discharge mode, and next watchdog time count starts.

③ Unless the SCK pulse is input, WDT will not be cleared, and during the charging period of TW pin, RESETB="L".

④ When the VIN pin becomes lower than the detector threshold voltage($-V_{DET}$), RESETB outputs "L".

∗ Watchdog Timeout period/Reset hold time

The watchdog timeout period and reset hold time can be set with an external capacitor to TW pin.

The next equations describe the relation between the watchdog timeout period and the external capacitor value, or the reset hold time and the external capacitor value.

$t_{WD(s)} = 3.1*10^6 \times C\,(F)$

tWR(s)=TWD/9

The watchdog timer (WDT) timeout period is determined with the discharge time of the external capacitor.

During the watchdog timeout period, if the clock pulse from the system is detected, WDT is cleared and the capacitor is charged. When the charge of the capacitor completes, another watchdog timeout period starts again. During the watchdog timeout period, if the clock pulse from the system is not detected, during the next reset hold time RESETB pin outputs "L".

After starting the watchdog timeout period, (just after from the discharge of the external capacitor) even if the clock pulse is input during the time period "TWDI", the clock pulse is ignored.
TWDI[s]=TWD/10

Released Delay Time (Power-on Reset delay time)
The released delay time can be set with an external capacitor connected to the CD pin. The next equation describes the relation between the capacitance value and the released delay time (tpLH).
$tpLH(s)=3.7\times10^6\times C(F)$
When the VDD voltage becomes equal or less than (-VDET), discharge of the capacitor connected to the CD pin starts. Therefore, if the discharge is not enough and VDD voltage returns to (+VDET) or more, thereafter the delay time will be shorter than tpLH which is expected.

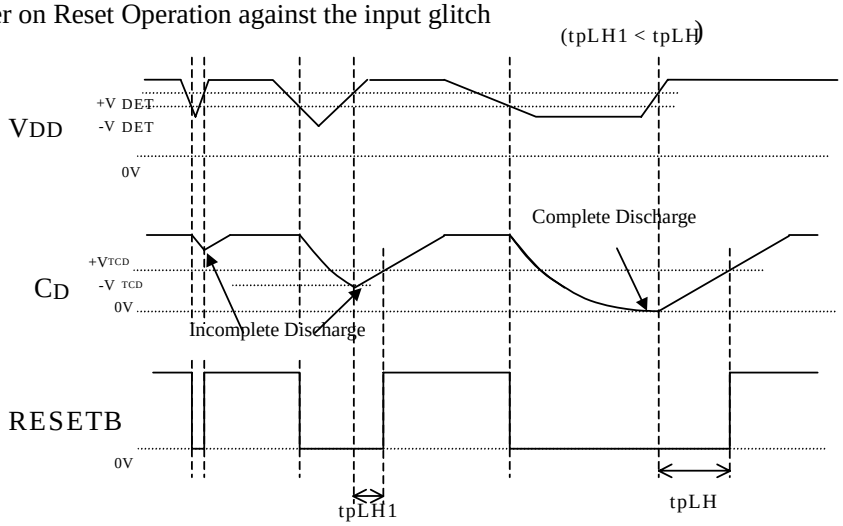
Minimum Operating Voltage
We specified the minimum operating voltage as the minimum input voltage in which the condition of RESETB pin being 0.1V or lower than 0.1V. (Herein, pull-up resistance is set as 100kΩ in the case of the Nch open-drain output type.

RESETB Output

RESETB pin's output type is selectable either the Nch open-drain output or CMOS output. If the Nch open-drain type output is selected, the RESETB pin is pulled up with an external resistor to an appropriate voltage source.

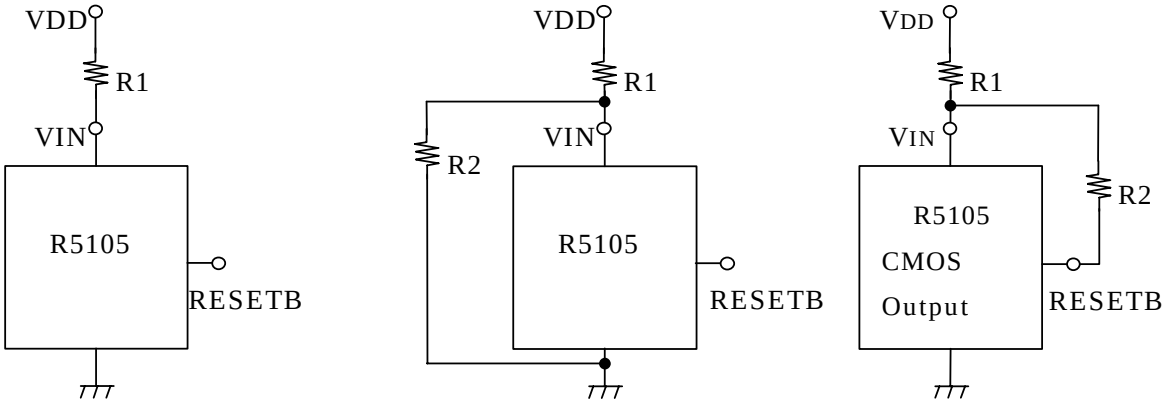
Clock Pulse Input
Built-in watchdog timer is cleared with the SCK clock pulse within the watchdog timeout period.

Power on Reset Operation against the input glitch



APPLICATION NOTES

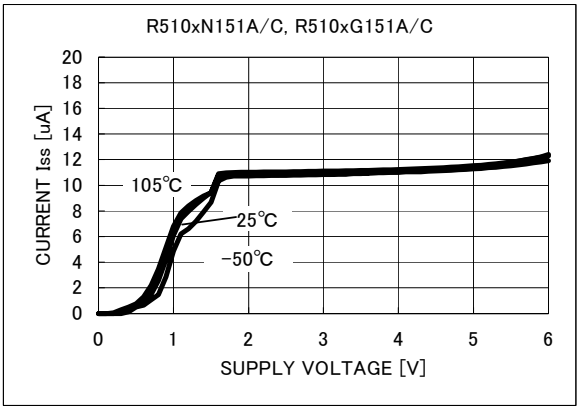
If a resistor is connected to the VDD pin, the operation might be unstable with the supply current of IC itself.

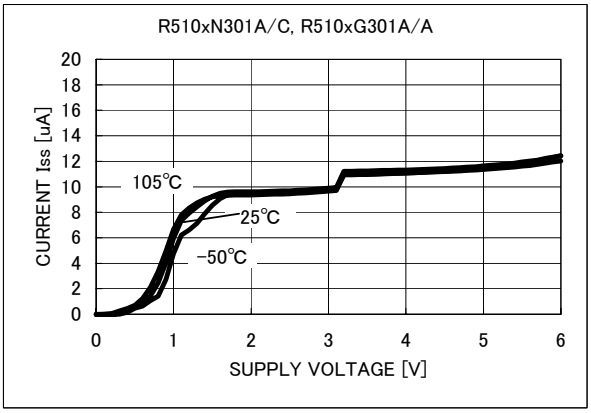


Connection examples affected by the conduction current

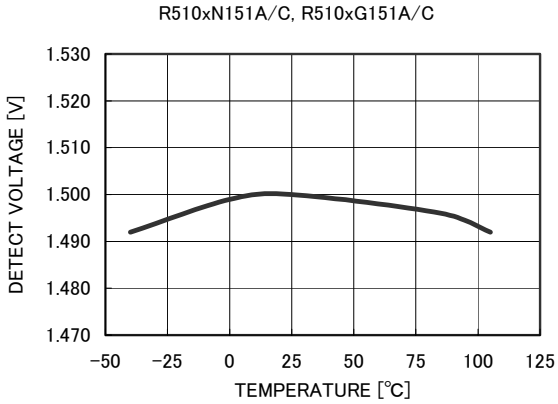
TYPICAL CHARACTERISTICS

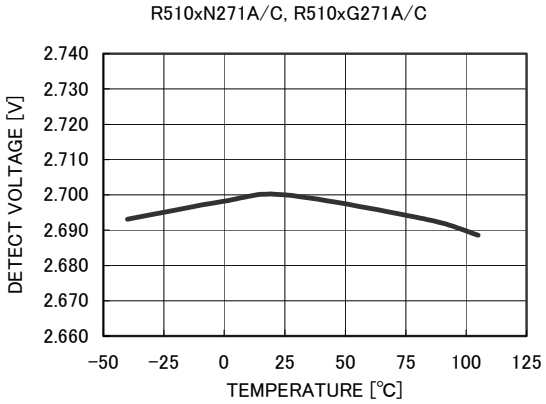
1) Supply Current vs. Input Voltage

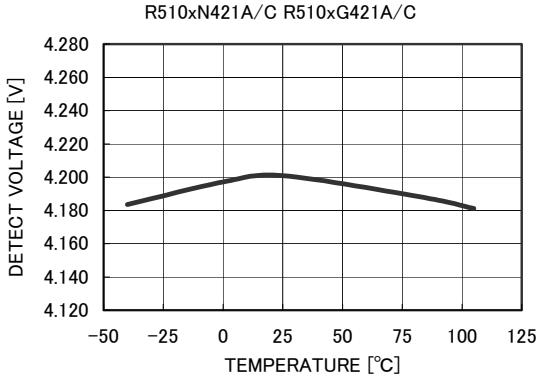




2) Detector Threshold vs. Temperature

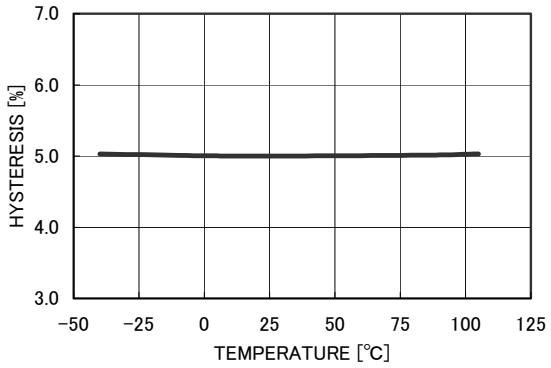




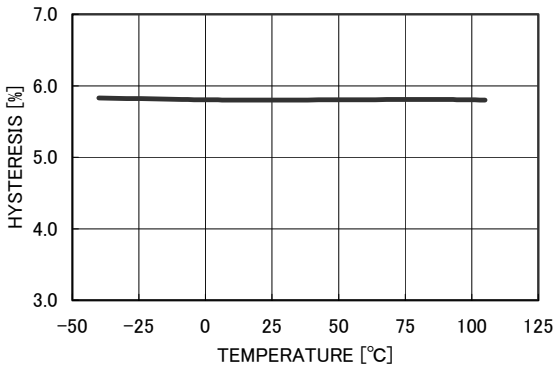


3) Detector Threshold Hysteresis vs. Temperature

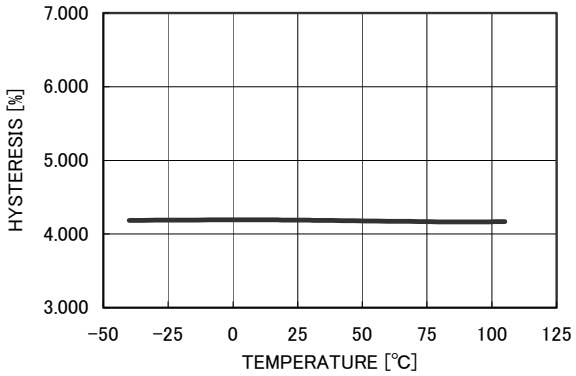
R510xN151A/C R510xG151A/C



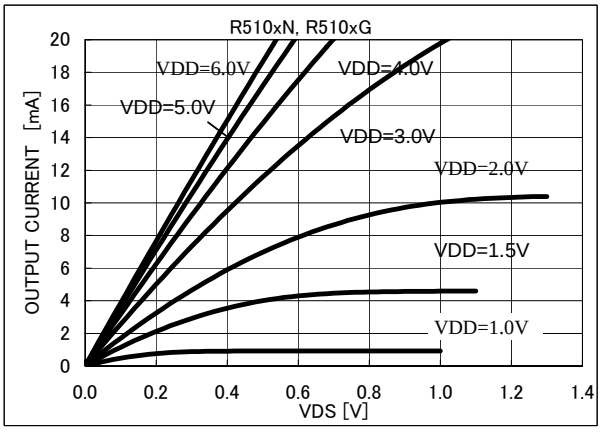
R510xN271A/C R510xG271A/C



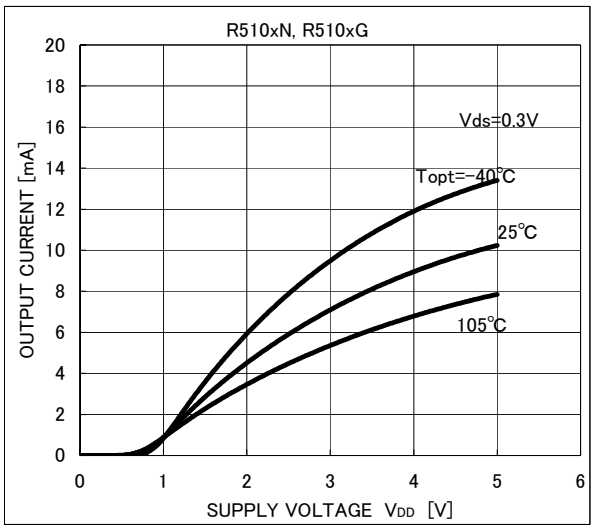
R510xN421A/C R510xG421A/C

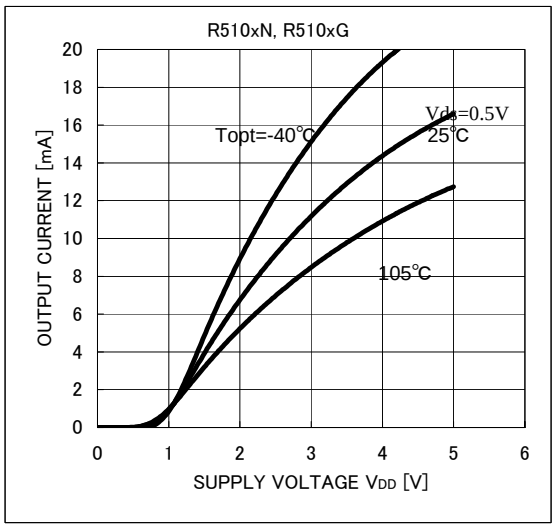


4) Nch Driver Output Current vs. V_{DS} Topt=25°C

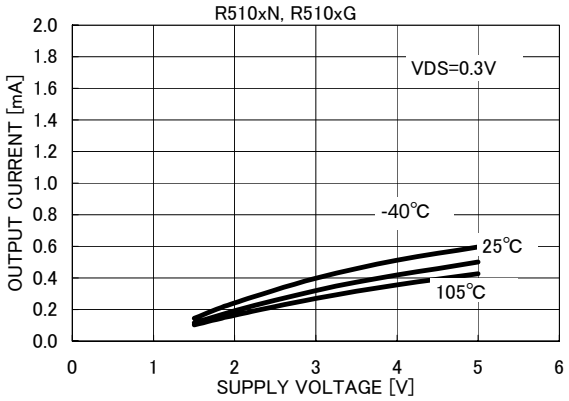


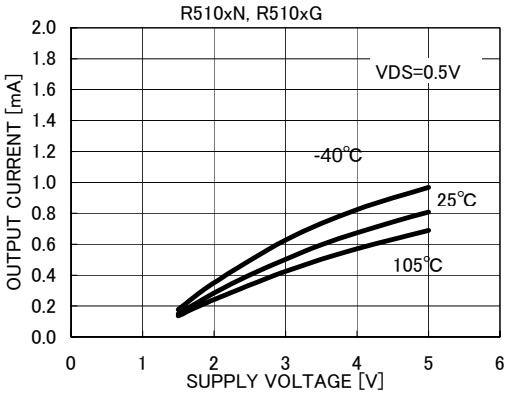
5) Nch Driver Output Current vs. V_{DD}

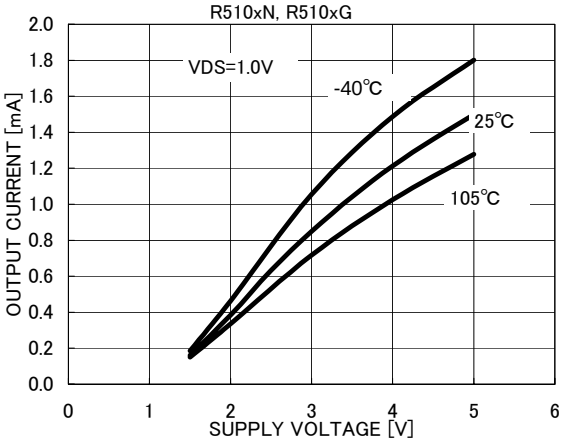




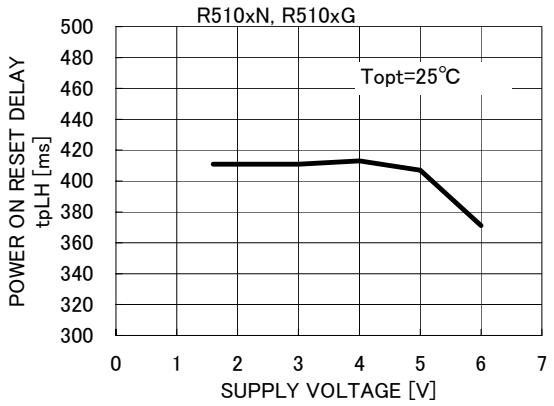
6) Pch Driver Output Current vs. V_{DD}



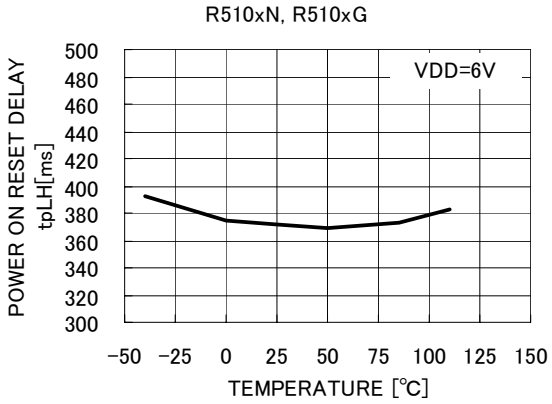




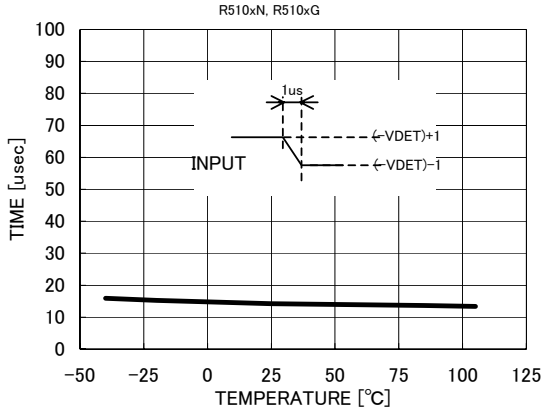
7) Released Delay Time vs. Input Voltage



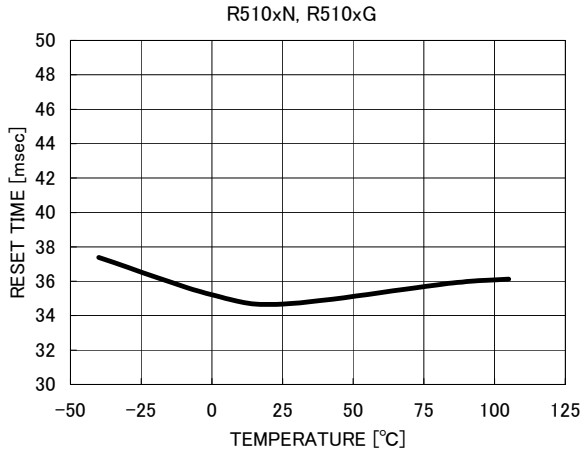
8) Released Delay Time vs. Temperature



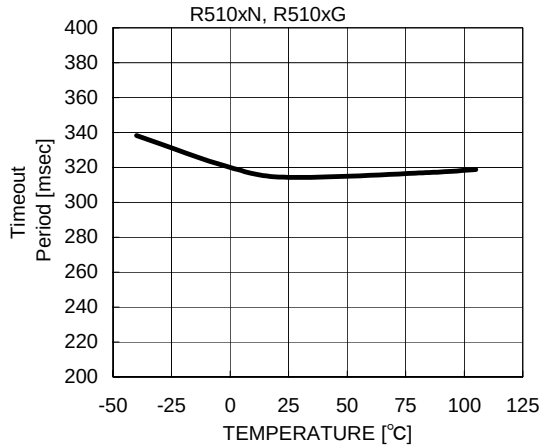
9) Detector Output Delay Time vs. Temperature



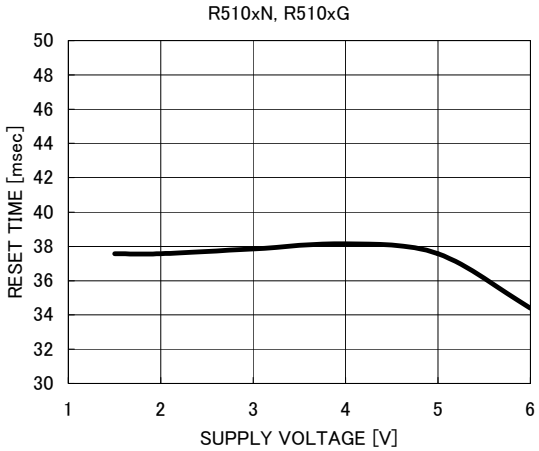
10) WDT Reset Timer vs. Temperature



11) WDT Timeout Period vs. Temperature



12) WDT Reset Timer vs. Input Voltage



13) WDT Timeout Period vs. Input Voltage