STRUCTURE : Silicon Monolithic Integrated Circuit
PRODUCT NAME : 3channels Synchronous Rectification DC/DC Converter controller IC
MODEL NAME : **BD8601FV**

◎FEATURES:
- 3ch Synchronous Rectification Step-down System DC/DC Converter controller IC
- 3ch can independently control ON/OFF.
- Soft start, Soft OFF function
- Building in low voltage and over voltage protection function
- Building in over current protection function
- Building in terminal RT OPEN/Short protection
- Building in Duty Clamp(90%ON)function
- Concentrated protection control with built-in sequencer
- Building in external reset output function
- The frequency can be set by external resistance.
- Building in Off latch signal output function
- SSOP-B40 package

◎ABSOLUTE MAXIMUM RATING : (Ta=25℃)

Parameter	Symbol	Limits	Unit
VCC supply voltage	VCC	20	V
VIN*1 supply voltage	VIN	20	V
Input terminal voltage	VINP	VCC	V
Output terminal voltage	VOUT	VCC	V
Power dissipation	Pd	0.9*2	W
Operating temperature	Topr	-40～85	℃
Storage temperature	Tstg	-55～150	℃

＊1 VIN=VIN1, VIN2, VIN3
＊2 70mm×70mm, thickness1.6mm, less than 3% share of copper foil when implementing glass epoxy board.
Operating at higher than Ta=25℃, 7.2mW shall be reduced per 1

◎OPERATION CONDITION (Please set the power-supply voltage in consideration of a power dissipation.)

Parameter	Symbol	MIN	TYP	MAX	Unit
VCC supply voltage	VCC	6.0	9.0	15	V
VIN*3 supply voltage	VIN	6.0	9.0	15	V

＊3 VIN=VIN1, VIN2, VIN3

This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

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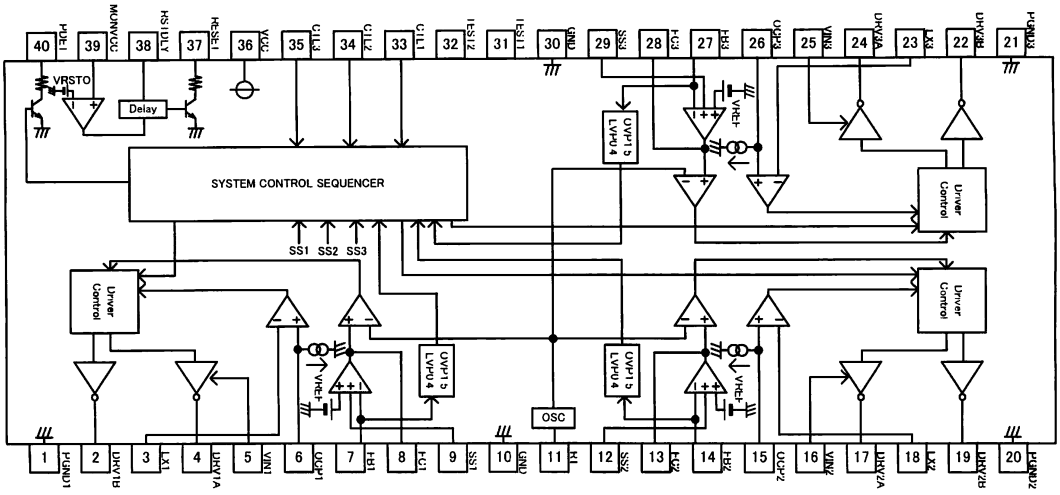
◎ELECTRICAL CHARACTERISTICS

(Unless otherwise noted Ta=25℃, VIN1,VIN2,VIN3=9.0V, VCC=9.0V, GND=0V)

Parameter	Symbol	specification value			UNIT	Condition
		MIN	TYP	MAX		
Circuit current 1	I_{Q1}	-	3.5	8	mA	CTL1,2,3=0V
Circuit current 2	I_{Q2}	-	7	15	mA	CTL1,2,3=VCC
<Error amplifier part Ch1,Ch2,Ch3>						
Standard voltage (VREF)	V_{REF}	0.792	0.8	0.808	V	Terminal FB and FC terminal short
Terminal FB Input bias current	I_{FBB}	-1	-	1	μA	V_{FB}=0.9V
Terminal FC Clamping voltage H	V_{FCH}	1.8	-	-	V	V_{FB}=0.7V
Terminal FC Clamping voltage L	V_{FCL}	-	-	0.2	V	V_{FB}=0.9V
Terminal FC Sink current	I_{FCSINK}	0.5	-	-	mA	V_{FB}=0.9V、V_{FC}=0.4V
Terminal FC Source current	$I_{FCSOURCE}$	-	-	-70	μA	V_{FB}=0.7V、V_{FC}=1.6V
Open loop gain	A_{VERR}	-	100	-	dB	
<OSC part >						
Oscillation frequency	F_{OSC}	100	-	600	kHz	
<Duty clamping part Ch1,Ch2,Ch3>						
Max ON duty ratio	F_{ONDUTY}	70	85	95	%	V_{FB}=0.7V
<Soft start part Ch1,Ch2,Ch3>						
Charging current	I_{SS}	-4.0	-2.5	-1.0	μA	V_{SS}=1.0V
Terminal SS Threshold voltage	V_{SSTH}	1.0	1.1	1.2	V	V_{SS} voltage、V_{FC}=0.8V
Terminal SS Clamping voltage	V_{SSCLM}	1.6	1.9	2.2	V	
Terminal SS Standby voltage	V_{SSSTB}	0.11	0.15	0.19	V	V_{SS} voltage (L→H)
Terminal SS Standby voltage Maximum hysteresis error	V_{SSSTB_HYS}	5	50	100	mV	
Terminal SS Discharge resistance	R_{SS}	49	70	91	kΩ	
Terminal SS Protection circuit start voltage	V_{SSPON}	1.0	1.1	1.2	V	V_{SS} voltage (L→H)
Terminal SS Protection circuit start voltage Maximum hysteresis error	V_{SSPON_HYS}	10	100	200	mV	V_{SS} voltage
<Low voltage, over voltage detection part Ch1,Ch2,Ch3>						
Terminal FB Low voltage detection voltage	V_{LVP}	0.27	0.32	0.37	V	V_{FB} voltage
Terminal FB Low voltage detection Maximum hysteresis error	V_{LVP_HYS}	10	100	200	mV	V_{FB} voltage
Terminal FB Overvoltage detection voltage	V_{OVP}	1.08	1.2	1.32	V	V_{FB} voltage
<Over current detection part Ch1,Ch2,Ch3>						
Terminal LX input bias current	I_{LXB}	−1	0	1	uA	
Terminal OCP input bias current	I_{OCPB}	20	50	80	uA	
<Reset detection part>						
Terminal MONVCC reset detection voltage	V_{RSTO}	0.98	1.0	1.02	V	V_{MONVCC} voltage (H→L)
Terminal MONVCC input bias current	$I_{MONVCCB}$	-1	-	1	uA	
Terminal RSTDLY charging current	I_{RSTDLY}	-15	-10	-5	uA	
Terminal RESET L output voltage	V_{OL_RST}	-	-	0.4	V	I_{OL}=100uA
<Others>						
Terminal PDET L output voltage	V_{OL_RDET}	-	-	0.4	V	I_{OL}=100uA
Terminal CTL input voltage H level voltage	V_{IH_CTL}	2.0	-	VCC	V	Terminal CTL1,2,3
Terminal CTL input voltage L level voltage	V_{IL_CTL}	-	-	0.5	V	Terminal CTL1,2,3
Terminal CTL input current	I_{I_CTL}	-	85	120	uA	Terminal CTL1,2,3、CTL=VCC
Terminal DRV H output voltage	V_{OH_DRV}	8.5	-	-	V	Terminal DRV1A,2A,3A,1B,2B,3B
Terminal DRV L output voltage	V_{OL_DRV}	-	-	0.5	V	Terminal DRV1A,2A,3A,1B,2B,3B

- V_{FB}:Terminal FB voltage、V_{FC}:Terminal FC voltage、V_{SS}:Terminal SS voltage、V_{MONVCC}:Terminal MONVCC voltage
- This product is not designed for protection against radioactive rays.
- The current ability must not exceed Pd.

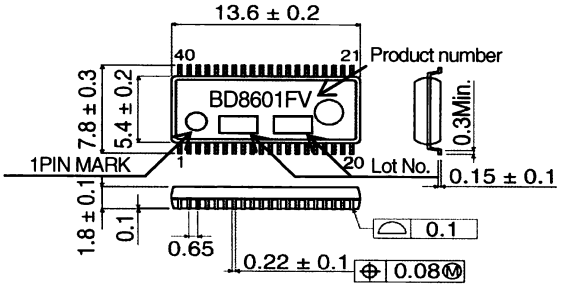
◎BLOCK DIAGRAM



◎PIN ASSIGNMENT

No.	Symbol	Description	No.	Symbol	Description
1	PGND1	Ch1 Power GND (The same electric potential as terminal GND)	21	PGND3	Ch3 Power GND (The same electric potential as terminal GND)
2	DRV1B	Ch1 N channel driving output terminal	22	DRV3B	Ch3 N channel drive output terminal
3	LX1	Ch1 Overcurrent detection terminal	23	LX3	Ch3 Overcurrent detection terminal
4	DRV1A	Ch1 P channel drive output terminal	24	DRV3A	Ch3 P channel drive output terminal
5	VIN1	Ch1 Power supply input terminal	25	VIN3	Ch3 Power supply input terminal
6	OCP1	Ch1 Over current detection level resistance connection terminal	26	OCP3	Ch3 Over current detection level resistance connection terminal
7	FB1	Ch1 Voltage detection terminal	27	FB3	Ch3 Voltage detection terminal
8	FC1	Ch1 Phase amends terminal	28	FC3	Ch3 Phase amends terminal
9	SS1	Ch1 Soft start adjustment capacity connection terminal	29	SS3	Ch3 Soft start adjustment capacity connection terminal
10	GND	GND (0V connection)	30	GND	GND (0V connection)
11	RT	Frequency adjustment resistance connection terminal	31	TEST1	Test terminal(Connect it with GND.)
12	SS2	Ch2 Soft start adjustment capacity connection terminal	32	TEST2	Test terminal(Connect it with GND.)
13	FC2	Ch2 Phase amends terminal	33	CTL1	Ch1 Control terminal
14	FB2	Ch2 Voltage detection terminal	34	CTL2	Ch2 Control terminal
15	OCP2	Ch2 Over current detection level resistance connection terminal	35	CTL3	Ch3 Control terminal
16	VIN2	Ch2 Power supply input terminal	36	VCC	Power supply input terminal
17	DRV2A	Ch2 P channel drive output terminal	37	RESET	Reset output terminal
18	LX2	Ch2 Overcurrent detection terminal	38	RSTDLY	Reset Delay adjustment capacity connection terminal
19	DRV2B	Ch2 N channel drive output terminal	39	MONVCC	VCC monitor terminal
20	PGND2	Ch2 Power GND (The same electric potential as terminal GND)	40	PDET	Off latch output terminal

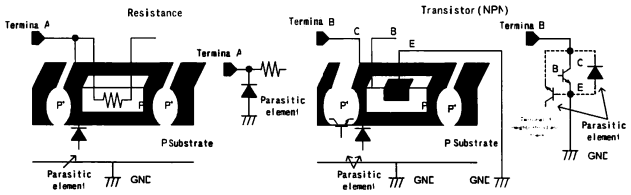
◎PACKAGE OUTLINE



SSOP-B40(UNIT : mm)

◎NOTE ON USE

1. About the absolute maximum rating
   Attention is brushed off enough to the quality control, it is likely to destroy when the absolute maximum rating such as impressed voltages (VCC_IN,DCIN) and ranges (Topr) of the operating temperature as it is exceeded, the mode of breakings of the short or the opening, etc. cannot be specified, and examine it in this IC to give physical measures for safety such as fuses when a special mode that exceeds the absolute maximum rating is assumed.
2. About the reverse-connection of the power supply connector
   IC might destroy it by reversely connecting the power supply connector. Give measures such as putting the diode between power supply terminals of power supply and IC outside for the reverse-touching destruction protection.
3. Power supply line
   Please do measures such as putting the bypass capacitor in power supply-GND nearest pin of this IC as the route of the resurrection current to cause the return of the current in which it resurrected it by the counter electromotive force of the coil.
   Please confirm the characteristic of the electrolytic capacitor enough as the capacity omission etc. at the low temperature never happen, and decide it.
4. About grand potential
   Any state of operation must become the lowest potential about the potential of the terminal GND. Moreover, confirm whether there is terminal that is actually the voltage of GND or less including transients.
5. About the heat design
   Think about permissible loss (Pd) in an actual state of use, and do the heat design with the margin enough.
6. About the short and the miss-installation between terminals
   Note the direction and the miss-registration of IC enough when you install it in the set substrate. IC might destroy it as well as reversely connecting the power supply connector when installing it by mistake. Moreover, there is fear of destruction when the foreign body enters between terminals, the terminal, the power supply, and grandeur and it is short-circuited.
7. About operation in strong electromagnetic field
   In use in strong electromagnetic field, note that there is a possibility of malfunctioning.
8. About the capacitor during output-GND
   The current charged the capacitor with when VCC is 0V or is GND and is short-circuited when a big capacitor is connected between GND output by some factors flows into the output and it is likely to destroy it. Give the capacitor between GND output to 0.1μF or less.
9. About the inspection by the set substrate
   It is likely to suffer stress to IC and discharge electricity every one process when you connect the capacitor with the pin with low impedance when inspecting it in the set substrate. Moreover, detach it after connecting after the power supply is turned off without fail when detaching it to G in the inspection process, inspecting, and turning off the power supply. n addition, be give the earth to the assembly process as a static electricity measures, and careful enough when it transports and you preserve it.
10. About each input terminal
    This IC is a monolithic IC which has a P^+ isolations and P substrate to isolate elements each other.
    This P layer and an N layer in each element form a PN junction to construct various parasitic elements.
    For instance, the potential difference operates in resistance as shown in the figure below when resistance and the transistor connect it with the terminal and the playground (GND) >(terminal B) joint of PN operates as a parasitic diode in playground (GND) >(terminal A) transistor (NPN). In addition, the NPN transistor of parasitism works with N layer of the element of the above-mentioned parasitic diode and the neighborhood and others in transistor (NPN). A parasitic element in IC composition is inevitably formed because of the potential relation.
    A parasitic element can operate, the interference with the circuit operation be caused, it malfunction, and, consequently, it cause destruction. Therefore, do not do the usage that a parasitic element operates as a voltage that is lower than the playground (GND;P substrate) is impressed to the input terminal enough. Moreover, do not impress the voltage to the input terminal when you do not impress the power-supply voltage to IC. Give each input terminal to me the voltage below the power-supply voltage or in the guarantee value of an electric characteristic when you similarly impress the power-supply voltage.



Example of IC of simple structure

11. Earth wiring pattern
    If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.

12. Thermal Shut-Down
    When a thermal shutdown operates, the DC/DC converter controller of all Ch is turned off. When a thermal shutdown is released, the DC/DC converter controller of all Ch becomes an operation beginning from turning off.

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