

STRUCTURE : Silicon Monolithic Integrated Circuit
 PRODUCT NAME : 1channels Synchronous Rectification DC/DC Converter IC for TV processor
 MODEL NAME : **B D 8 6 2 8 E F V**

- ◎FEATURES:
- 1ch Synchronous Rectification Step-down System DC/DC Converter
 - Soft start, Soft OFF function
 - Building in low voltage and over voltage protection function
 - Building in over current protection function
 - The frequency can be set by external resistance. (Terminal RT)
 - It is possible to set by external resistance at the protection time. (Terminal RSET)
 - Building in terminal RT/RSET OPEN/Short protection
 - Concentrated protection control with built-in sequencer
 - With built-in adjustment function time of off latch
 - With built-in abnormal state detection signal output function
 - For protecting bus
 - Load current 3A or less
 - HTSSOP – B24 package

◎ABSOLUTE MAXIMUM RATING: (Ta=25°C)

Parameter	Symbol	Limits	Unit
VCC supply voltage	VCC	10	V
BOOT voltage	VBOOT	18 *1	V
Input terminal voltage	VINP	VCC	V
Output terminal voltage	VOUT	VCC	V
Power dissipation	Pd	3.99*2	W
Operating temperature	Topr	-20 ~ 85	°C
Storage temperature	Tstg	-55 ~ 150	°C

*1 Voltage of terminal SW 9V Voltage of terminal GND 18V

*2 Ta=25°C or more is reduced with 32mW/°C 70mm×70mm, thickness 1.6mm, and four layer glass epoxy substrate is mounted.

◎OPERATION CONDITION (Please set the power-supply voltage in consideration of a power dissipation.)

Parameter	Symbol	MIN	TYP	MAX	Unit
VCC supply voltage	VCC	4.5	6.5	8.0	V

This product is not designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

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◎ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted Ta=25°C, VCC=6.5V, GND=0V, CTL=6.5V)

Parameter	Symbol	specification value			UNIT	Condition
		MIN	TYP	MAX		
Circuit current 1	I _{Q1}	-	0	10	μA	CTL=0V
Circuit current 2	I _{Q2}	-	3.4	-	mA	CTL=VCC
< Error amplifier part >						
Standard voltage (VREF)	V _{REF}	0.792	0.8	0.808	V	Terminal FB and FC terminal short
Terminal FB Input bias current	I _{FBB}	-1	0	1	μA	V _{FB} =0.9V
Terminal FC Clamping voltage H	V _{FCH}	1.8	-	-	V	V _{FB} =0.7V
Terminal FC Clamping voltage L	V _{FCL}	-	-	0.2	V	V _{FB} =0.9V
Terminal FC Sink current	I _{FC} SINK	0.5	-	-	mA	V _{FB} =0.9V, V _{FC} =0.4V
Terminal FC Source current	I _{FC} SOURCE	-	-	-70	μA	V _{FB} =0.7V, V _{FC} =1.6V
Open loop gain	A _{VERR}	-	100	-	dB	
< OSC part >						
Oscillation frequency	F _{OSC}	400	500	600	kHz	When terminal RT 27KΩ is connected
< Soft start part >						
Charging current	I _{SS}	-3	-2.5	-2	μA	V _{SS} =1.0V
Terminal SS Threshold voltage	V _{SS} TH	0.98	1.08	1.18	V	V _{SS} voltage
Terminal SS Clamping voltage	V _{SS} CLM	2.2	2.4	-	V	
Terminal SS Standby voltage	V _{SS} STB	0.1	0.15	-	V	V _{SS} voltage (L→H)
Terminal SS Discharge resistance	R _{SS}	49	70	91	kΩ	CTL=0V
Terminal SS Protection circuit start voltage	V _{SS} SPON	1.0	1.1	1.2	V	V _{SS} voltage (L→H)
Terminal SS Protection circuit start voltage Maximum hysteresis error	V _{SS} SPON_HYS	10	100	200	mV	V _{SS} voltage
< Low voltage, over voltage detection part >						
Terminal FB Low voltage detection voltage	V _{LVP}	0.51	0.56	0.61	V	V _{FB} voltage
Terminal FB Overvoltage detection voltage	V _{OVP}	0.86	0.96	1.06	V	V _{FB} voltage
< Over current detection part >						
Output current limitation sresshold	I _{Int}	VCC-0.9	VCC-0.7	VCC-0.5	V	V _{SW} voltage
< PowMOS >						
Upper side MOS ON resistance	R _{ONU}	-	110	-	mΩ	V _{BOOT} -V _{SW} =5V
Lower side MOS ON resistance	R _{ONL}	-	110	-	mΩ	V _{VREG5} =5V
< Others >						
Terminal PDET L output voltage	V _{OL} PDET	-	-	0.4	V	I _{OL} =100uA
Terminal CTL input voltage H level voltage	V _{IH} CTL	2.0	-	VCC	V	Terminal CTL
Terminal CTL input voltage L level voltage	V _{IL} CTL	-	-	0.5	V	Terminal CTL
Terminal CTL input current	I _I CTL	-	60	90	μA	Terminal CTL, CTL=VCC

- V_{FB} : Terminal FB voltage, V_{FC} : Terminal FC voltage, V_{SS} : Terminal SS voltage
V_{VREG5} : Terminal VREG5 voltage, V_{BOOT} : Terminal BOOT voltage, V_{SW} : Terminal SW voltage
- This product is not designed for protection against radioactive rays.
- The current ability must not exceed Pd.

©BLOCK DIAGRAM

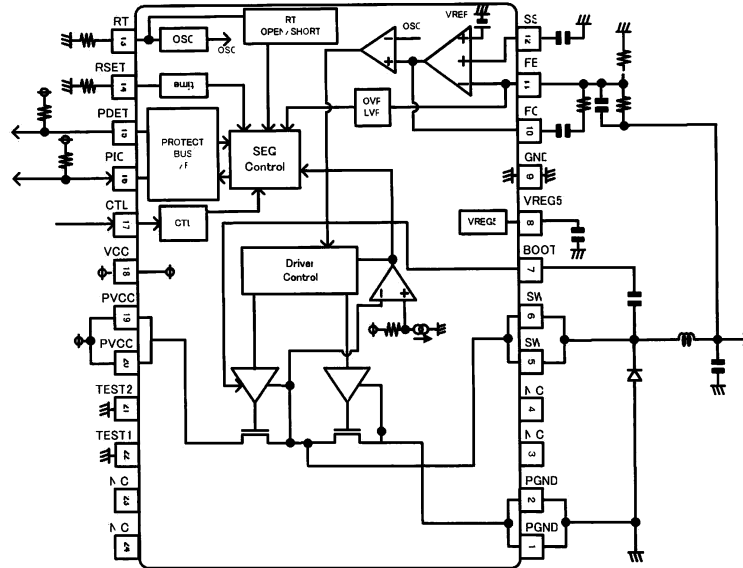


Figure - 1 Block chart and application chart

©PIN ASSIGNMENT

No.	Symbol	Description	No.	Symbol	Description
1	PGND	Power GND terminal	13	RT	Frequency adjustment resistance connection terminal
2	PGND	Power GND terminal	14	RSET	Adjustment resistance terminal of off latch effective time
3	N.C.	No wire connection (Connect it with GND)	15	PDET	Abnormal state notification terminal
4	N.C.	No wire connection (Connect it with GND)	16	PIO	Abnormal state notification and external IC abnormality detection terminal
5	SW	Terminal SW	17	CTL	Enable input
6	SW	Terminal SW	18	VCC	VCC supply terminal
7	BOOT	High side PowMOS gate mechanical power source terminal	19	PVCC	Power VCC terminal
8	VREG5	Internal supply (5.0V) output terminal	20	PVCC	Power VCC terminal
9	GND	GND	21	TEST2	Test terminal (Connect it with GND)
10	FC	Phase amends terminal	22	TEST1	Test terminal (Connect it with GND)
11	FB	Feedback terminal	23	N.C.	No wire connection (Connect it with GND)
12	SS	Soft start adjustment capacity connection terminal	24	N.C.	No wire connection (Connect it with GND)

©PACKAGE OUTLINE

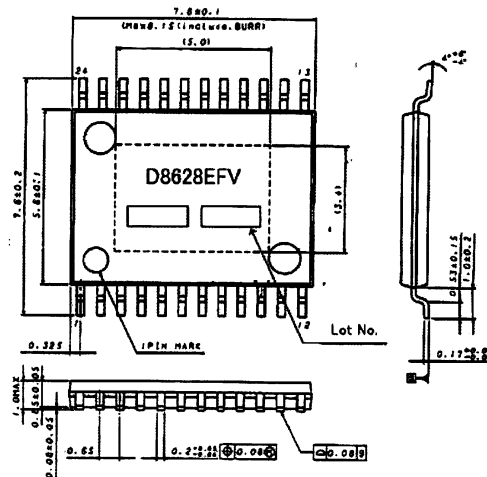
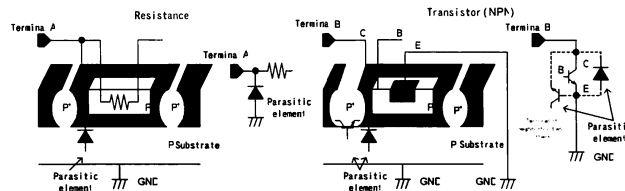


Figure-2 HTSSOP-B24(UNIT:mm)

◎NOTE ON USE

1. About the absolute maximum rating
 Attention is brushed off enough to the quality control, it is likely to destroy when the absolute maximum rating such as impressed voltages (VCC_IN,DCIN) and ranges (Topr) of the operating temperature as it is exceeded, the mode of breakings of the short or the opening, etc. cannot be specified, and examine it in this IC to give physical measures for safety such as fuses when a special mode that exceeds the absolute maximum rating is assumed.
2. About the reverse-connection of the power supply connector
 IC might destroy it by reversely connecting the power supply connector. Give measures such as putting the diode between power supply terminals of power supply and IC outside for the reverse-touching destruction protection.
3. Power supply line
 Please do measures such as putting the bypass capacitor in power supply-GND nearest pin of this IC as the route of the resurrection current to cause the return of the current in which it resurrected it by the counter electromotive force of the coil.
 Please confirm the characteristic of the electrolytic capacitor enough as the capacity omission etc. at the low temperature never happen, and decide it.
4. About grand potential
 Any state of operation must become the lowest potential about the potential of the terminal GND. Moreover, confirm whether there is terminal that is actually the voltage of GND or less including transients.
5. About the heat design
 Think about permissible loss (Pd) in an actual state of use, and do the heat design with the margin enough.
6. About the short and the miss-installation between terminals
 Note the direction and the miss-registration of IC enough when you install it in the set substrate. IC might destroy it as well as reversely connecting the power supply connector when installing it by mistake. Moreover, there is fear of destruction when the foreign body enters between terminals, the terminal, the power supply, and grandeur and it is short-circuited.
7. About operation in strong electromagnetic field
 In use in strong electromagnetic field, note that there is a possibility of malfunctioning.
8. About the capacitor during output-GND
 The current charged the capacitor with when VCC is 0V or is GND and is short-circuited when a big capacitor is connected between GND output by some factors flows into the output and it is likely to destroy it. Give the capacitor between GND output to 0.1μF or less.
9. About the inspection by the set substrate
 It is likely to suffer stress to IC and discharge electricity every one process when you connect the capacitor with the pin with low impedance when inspecting it in the set substrate. Moreover, detach it after connecting after the power supply is turned off without fail when detaching it to G in the inspection process, inspecting, and turning off the power supply. n addition, be give the earth to the assembly process as a static electricity measures, and careful enough when it transports and you preserve it.
10. About each input terminal
 This IC is a monolithic IC which has a P⁺ isolations and P substrate to isolate elements each other.
 This P layer and an N layer in each element form a PN junction to construct various parasitic elements.
 For instance, the potential difference operates in resistance as shown in the figure below when resistance and the transistor connect it with the terminal and the playground (GND) >(terminal B) joint of PN operates as a parasitic diode in playground (GND) >(terminal A) transistor (NPN).
 In addition, the NPN transistor of parasitism works with N layer of the element of the above-mentioned parasitic diode and the neighborhood and others in transistor (NPN). A parasitic element in IC composition is inevitably formed because of the potential relation.
 A parasitic element can operate, the interference with the circuit operation be caused, it malfunction, and, consequently, it cause destruction.
 Therefore, do not do the usage that a parasitic element operates as a voltage that is lower than the playground (GND;P substrate) is impressed to the input terminal enough. Moreover, do not impress the voltage to the input terminal when you do not impress the power-supply voltage to IC.
 Give each input terminal to me the voltage below the power-supply voltage or in the guarantee value of an electric characteristic when you similarly impress the power-supply voltage.



Example of IC of simple structure

11. Earth wiring pattern

If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.

12. Thermal Shut-Down

When a thermal shutdown operates, the DC/DC converter is turned off. When a thermal shutdown is released, the DC/DC converter becomes an operation beginning from turning off.

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