

STRUCTURE : Silicon Monolithic Integrated Circuit
 PRODUCT NAME : Synchronous rectification with built-in FET type DC/DC converter IC for TV processor
 MODEL NAME : **B D 8 6 2 7 E F V**

- FEATURES :
- Synchronous rectification with built-in FET type DC/DC converter
 - Output current 3A
 - Standard voltage accuracy FB 0.8V±1%
 - Range of operation power-supply voltage VIN 4.5V~6.0V
 - Switching frequency 250kHz~1MHz
 - Over current protection circuit
 - Thermal shutdown
 - Output voltage watch function (PDET)
 - Input low voltage detection UVLO4.0V
 - Soft start / Start delay circuit
- (The external analog voltage synchronization is also possible because of an external circuit.)

◎ABSOLUTE MAXIMUM RATING (Ta=25°C)

Parameter	Symbol	Limits	Unit
Input supply voltage	V _{IN}	7	V
Input terminal voltage	V _{INP} ^{*1}	V _{IN}	V
Output terminal voltage	V _{OUT} ^{*2}	V _{IN}	V
Output current	I _{OUT}	4	A
Power dissipation	Pd	3.2 ^{*3}	W
Operating temperature	Topr	-10 ~ 85	°C
Storage temperature	Tstg	-55 ~ 150	°C

*1 V_{INP} Application terminal : EN, SS/DELAY, TEST, FB

*2 V_{OUT} Application terminal : SW, PDET, FC, RT, REG

*3 (70mm×70mm, thickness 1.6mm, and four layer glass epoxy substrates)When mounting substrate and the package back exposure part are connected with solder.

Operating at higher than Ta=25°C, 25.6mW shall be reduced per 1

◎Operation condition

Parameter	Symbol	MIN	TYP	MAX	Unit
Input supply voltage	V _{IN}	4.5	-	6.0	V
Output current	I _{OUT}	-	-	3.0	A

This product is not designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

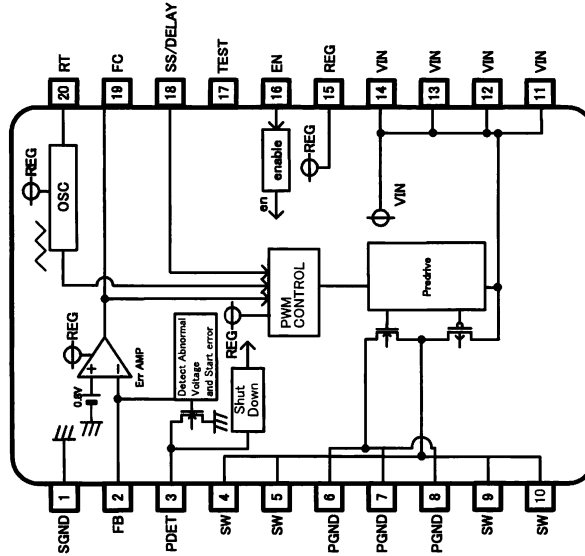
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©ELECTRICAL CHARACTERISTICS (Unless otherwise noted Ta=25°C, V_{IN}=5.6V)

Parameter	Symbol	specification value			UNIT	Condition
		MIN	TYP	MAX		
Circuit current when operating	I _{Q_active}	-	1.3	2.0	mA	V _{FB} = 0.83V, V _{FC} = 1V
Circuit current at standby	I _{Q_sby}	-	350	700	μA	V _{EN} = 0V
Standard voltage (V _{REF})	V _{REF}	0.792	0.8	0.808	V	
Output rise detection voltage	V _{OVP}	30	60	90	mV	V _{REF} Standard
Output decrease detection voltage	V _{LVP}	-90	-60	-30	mV	V _{REF} Standard
Terminal PDET output current ability	I _{PDET}	1	-	-	mA	V _{PDET} < 0.5V
Oscillation frequency	f _{OSC}	500	550	600	kHz	R _{OSC} = 220kΩ
Pch FET ON resistance	R _{PFET}	-	85	120	mΩ	I _{SW} = 1A
Nch FET ON resistance	R _{NFET}	-	65	100	mΩ	I _{SW} = -1A
UVLO voltage	V _{UVLO}	3.8	4.0	4.2	V	
SW leake current	I _{LSW}	-	0	1	μA	V _{EN} = 0V, V _{IN} = 6V
Terminal EN H sreshold voltage	V _{ENH}	2.0	-	-	V	
Terminal EN L sreshold voltage	V _{ENL}	-	-	0.5	V	
Terminal SS/DELAY source current	I _{SSSO}	2	4	6	μA	

- V_{FB}: Terminal FB voltage, V_{EN} : Terminal EN voltage, V_{FC} : Terminal FC voltage, V_{PDET}: Terminal PDET voltage
- The current ability must not exceed Pd.

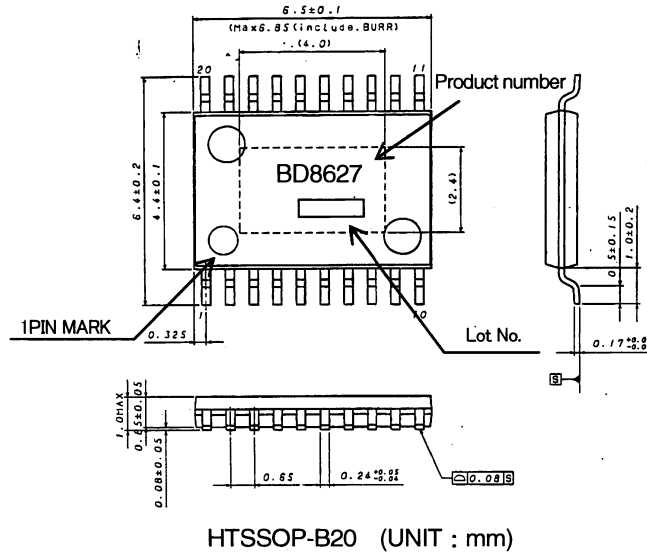
◎BLOCK DIAGRAM



◎PIN ASSIGNMENT

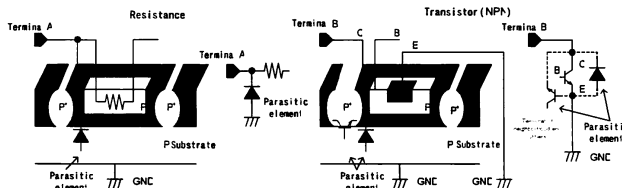
No.	Symbol	Description	No.	Symbol	Description
1	SGND	Signal GND terminal	11	VIN	Power supply input terminal
2	FB	Feedback terminal	12	VIN	Power supply input terminal
3	PDET	Output abnormality detection terminal	13	VIN	Power supply input terminal
4	SW	Switching output terminal	14	VIN	Power supply input terminal
5	SW	Switching output terminal	15	REG	Internal regulator output terminal
6	PGND	Power GND terminal	16	EN	Enable input
7	PGND	Power GND terminal	17	TEST	Test terminal
8	PGND	Power GND terminal	18	SS/DELAY	Soft start adjustment capacity connection terminal
9	SW	Switching output terminal	19	FC	Phase amends terminal
10	SW	Switching output terminal	20	RT	Frequency adjustment resistance connection terminal

◎PACKAGE OUTLINE



◎NOTE ON USE

1. About the absolute maximum rating
Attention is brushed off enough to the quality control, it is likely to destroy when the absolute maximum rating such as impressed voltages (VCC_IN,DCIN) and ranges (Topr) of the operating temperature as it is exceeded, the mode of breakings of the short or the opening, etc. cannot be specified, and examine it in this IC to give physical measures for safety such as fuses when a special mode that exceeds the absolute maximum rating is assumed.
2. About the reverse-connection of the power supply connector
IC might destroy it by reversely connecting the power supply connector. Give measures such as putting the diode between power supply terminals of power supply and IC outside for the reverse-touching destruction protection.
3. Power supply line
Please do measures such as putting the bypass capacitor in power supply-GND nearest pin of this IC as the route of the resurrection current to cause the return of the current in which it resurrected it by the counter electromotive force of the coil.
Please confirm the characteristic of the electrolytic capacitor enough as the capacity omission etc. at the low temperature never happen, and decide it.
4. About grand potential
Any state of operation must become the lowest potential about the potential of the terminal GND. Moreover, confirm whether there is terminal that is actually the voltage of GND or less including transients.
5. About the heat design
Think about permissible loss (Pd) in an actual state of use, and do the heat design with the margin enough.
6. About the short and the miss-installation between terminals
Note the direction and the miss-registration of IC enough when you install it in the set substrate. IC might destroy it as well as reversely connecting the power supply connector when installing it by mistake. Moreover, there is fear of destruction when the foreign body enters between terminals, the terminal, the power supply, and grandeur and it is short-circuited.
7. About operation in strong electromagnetic field
In use in strong electromagnetic field, note that there is a possibility of malfunctioning.
8. About the capacitor during output-GND
The current charged the capacitor with when VCC is 0V or is GND and is short-circuited when a big capacitor is connected between GND output by some factors flows into the output and it is likely to destroy it. Give the capacitor between GND output to 0.1μF or less.
9. About the inspection by the set substrate
It is likely to suffer stress to IC and discharge electricity every one process when you connect the capacitor with the pin with low impedance when inspecting it in the set substrate. Moreover, detach it after connecting after the power supply is turned off without fail when detaching it to G in the inspection process, inspecting, and turning off the power supply. n addition, be give the earth to the assembly process as a static electricity measures, and careful enough when it transports and you preserve it.
10. About each input terminal
This IC is a monolithic IC which has a P⁺ isolations and P substrate to isolate elements each other.
This P layer and an N layer in each element form a PN junction to construct various parasitic elements.
For instance, the potential difference operates in resistance as shown in the figure below when resistance and the transistor connect it with the terminal and the playground (GND) >(terminal B) joint of PN operates as a parasitic diode in playground (GND) >(terminal A) transistor (NPN). In addition, the NPN transistor of parasitism works with N layer of the element of the above-mentioned parasitic diode and the neighborhood and others in transistor (NPN). A parasitic element in IC composition is inevitably formed because of the potential relation.
A parasitic element can operate, the interference with the circuit operation be caused, it malfunction, and, consequently, it cause destruction. Therefore, do not do the usage that a parasitic element operates as a voltage that is lower than the playground (GND;P substrate) is impressed to the input terminal enough. Moreover, do not impress the voltage to the input terminal when you do not impress the power-supply voltage to IC. Give each input terminal to me the voltage below the power-supply voltage or in the guarantee value of an electric characteristic when you similarly impress the power-supply voltage.



Example of IC of simple structure

11. Earth wiring pattern
If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.
12. Thermal Shut-Down
When a thermal shutdown operates, the DC/DC converter controller of all Ch is turned off.

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