IC Card Interface ICs

Built-in DC/DC converter IC card interface ICs

BD8904F, BD8904FV, BD8905F, BD8906F, BD8906FV, BD8907F

- Overview

This is an interface IC for a 3V or 5V smart card.
It works as a bidirectional signal buffer between a smart card and a controller. Also, it supplies 3V or 5V power to a smart card. With electrostatic breakdown voltage of more than HBM: ±6000V, it protects the card contact pins.

- Features

1) 3 half duplex bidirectional buffers
2) Protection against short-circuit for all the card contact pins
3) Card power source (VREG) of 3V or 5V
4) Overcurrent protection for card power source
5) Built-in thermal shutdown circuit
6) Built-in supply voltage detector
7) Automatic start-up/shutdown sequence function for card contact pin
   Start-up sequence: driven by a signal from controller (CMDVCCB↓)
   Shutdown sequence: driven by a signal from controller (CMDVCCB↑) and fault detection (card removal, short circuit of card power, IC overheat detection, VDD or VDDP drop)
8) Card contact pin ESD voltage □ ±6000V
9) 2MHz - 26MHz integrated crystal oscillator
10) Programmable for clock division of output signal by 1, 1/2, 1/4, and 1/8
11) RST output control by RSTIN input signal (positive output)
12) One multiplexed card status output by OFFB signal

Device differences

	Resistor to set VDD voltage detector	Input Voltage		Operating temperature	Package
		VDD	VDDP		
BD8904F	External	2.7V - 5.5V	3.0V - 5.5V	-40°C - +85°C	SOP28
BD8904FV	External	2.7V - 5.5V	3.0V - 5.5V	-40°C - +85°C	SSOP-B28
BD8905F	External	2.7V - 5.5V	3.0V - 5.5V	-25°C - +85°C	SOP28
BD8906F	Built-in	3.0V - 5.5V	3.0V - 5.5V	-25°C - +85°C	SOP28
BD8906FV	Built-in	3.0V - 5.5V	3.0V - 5.5V	-25°C - +85°C	SSOP-B28
BD8907F	Built-in	3.0V - 5.5V	3.0V - 5.5V	-40°C - +85°C	SOP28

- Application

Interface for smart cards
Interface for B-CAS cards

Dec. 2008

- Absolute maximum ratings (Ta=25°C)
- This product is not designed to be radiation tolerant. •Absolute maximum ratings are not meant for guarantee of operation.

Parameter		Symbol	Rating	Unit	Note	
VDD Input Voltage		V_{DD}	-0.3 - 6.5	V		
VDDP Input Voltage		V_{DDP}	-0.3 - 6.5	V		
I/O Pin Voltage		V_{IN} V_{OUT}	-0.3 - +6.5	V	Pin: XTAL1, XTAL2, VSEL, RSTIN, AUX1C, AUX2C, IOC, CLKDIV1, CLKDIV2, CMDVCCB, OFFB, PORADJ, S2	
Card Contact Pin Voltage		V_{REG}	-0.3 - +6.5	V	Pin: PRES, PRESB, CLK, RST, IO, AUX1, AUX2	
Charge Pump Pin Voltage		V_n	-0.3 - +14.0	V	Pin: VCH, S1	
Junction Temperature		T_{jmax}	+150	°C		
Storage Temperature		T_{stg}	-55 - +150	°C		
Power Dissipation	BD8904F	P_{tot}	750	mW	Ta=-40 - +85°C	* Refer to the following package power dissipation
	BD8905F				Ta=-25 - +85°C	
	BD8906F				Ta=-25 - +85°C	
	BD8907F				Ta=-40 - +85°C	
	BD8904FV		1060		Ta=-40 - +85°C	
	BD8906FV				Ta=-25 - +85°C	

- Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Operating temperature	T_{opr}	-40	-	+85	°C	BD8904F, BD8904FV, BD8907F
		-25	-	+85	°C	BD8905F,BD8906F, BD8906FV
VDD Input Voltage	V_{DD}	2.7	-	5.5	V	BD8904F, BD8904FV, BD8905F
		3.0	-	5.5	V	BD8906F,BD8906FV, BD8907F
VDDP Input Voltage	V_{DDP}	4.5	5.0	5.5	V	VREG=5V; Ivreg ≤ 60mA
		3.0	-	4.5	V	VREG=5V; Ivreg ≤ 20mA, Except BD8904FV
		3.1	-	4.5	V	VREG=5V; Ivreg ≤ 25mA, Application to BD8904FV
		3.0	-	3.1	V	VREG=5V; Ivreg ≤ 20mA, Application to BD8904FV
		3.0	5.0	5.5	V	VREG=3V; Ivreg ≤ 60mA

- Package Power Dissipation

The power dissipation of the package will be as follows in case that ROHM standard PCB is used.
Use of this device beyond the following the power dissipation may cause permanent damage.

BD8904F, BD8905F, BD8906F, BD8907F: Pd=750mW; however, reduce 6mW per 1°C when used Ta≥25°C.
BD8904FV, BD8906FV : Pd=1060mW; however, reduce 8.5mW per 1°C when used Ta≥25°C.

ROHM standard PCB: Size: 70×70×1.6 (mm^3), Material: FR4 glass epoxy board (copper plate area of 3% or less)

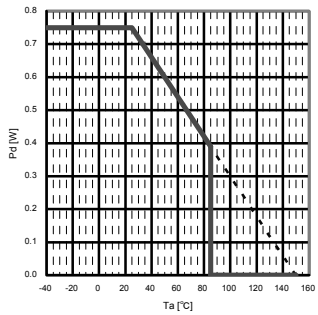


Fig. 1-1 Power Dissipation of BD8904F, BD8905F, BD8906F, BD8907F

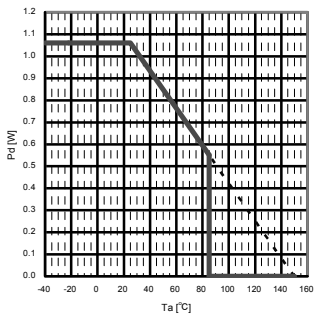


Fig. 1-2 Power Dissipation of BD8904FV, BD8906FV

- Block Diagram

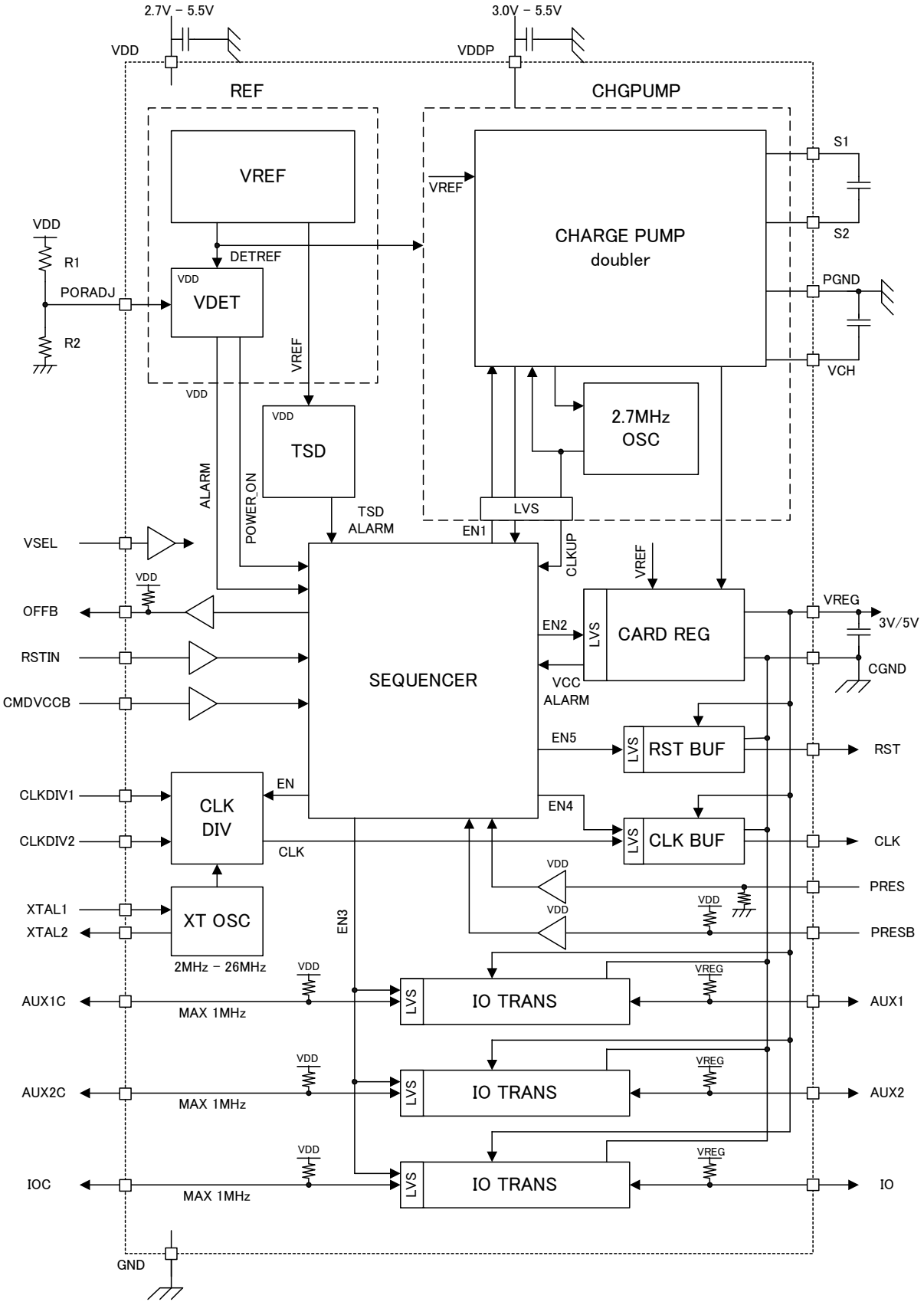
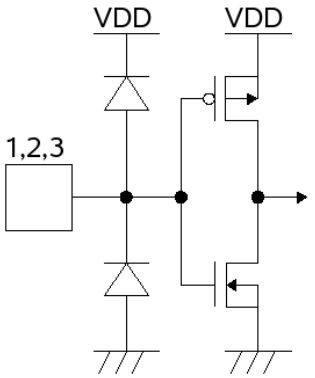
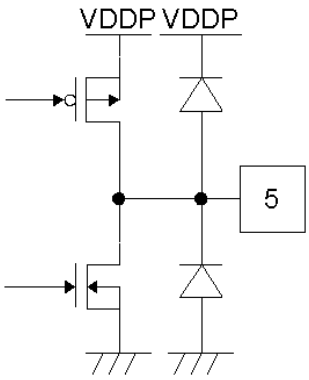
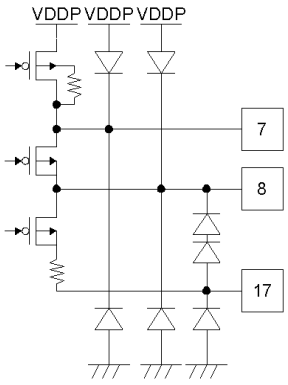
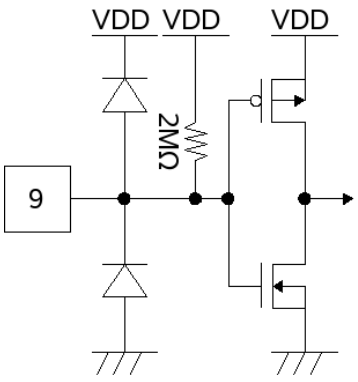


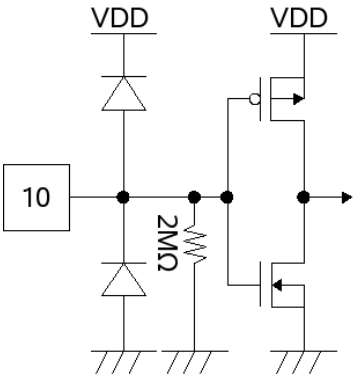
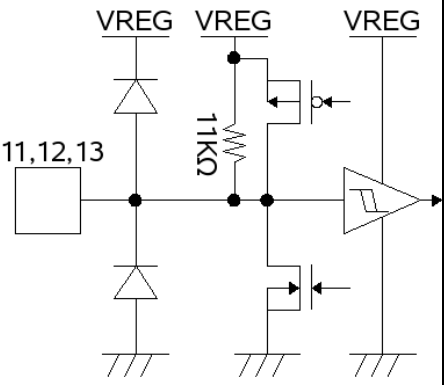
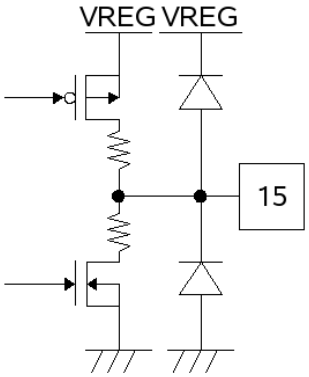
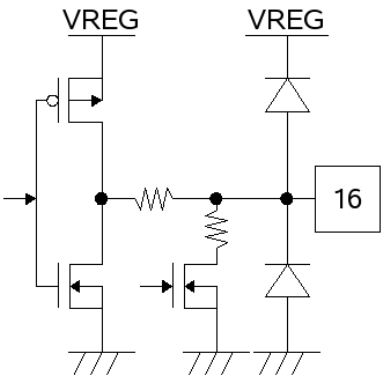
Fig. 3

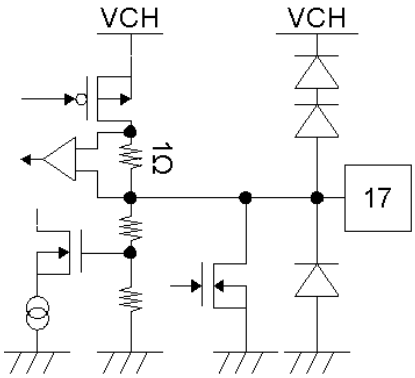
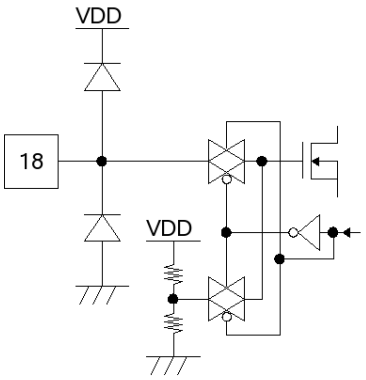
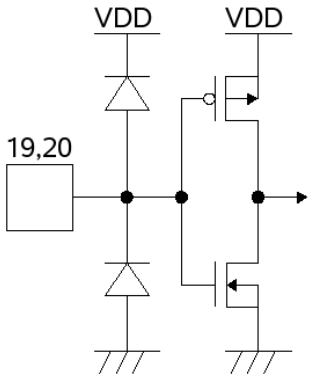
- Pin Description

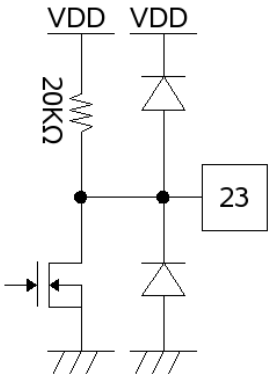
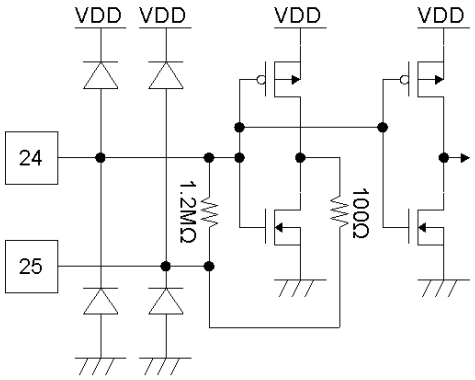
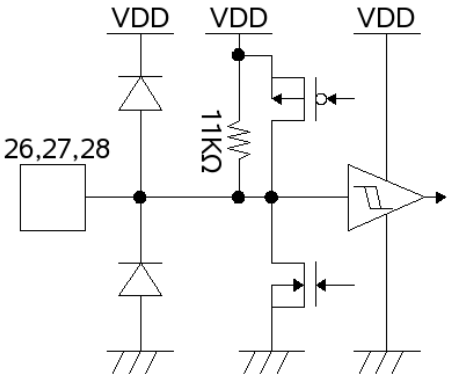
Pin No.	Pin Name	I/O	Signal Level	Pin Function
1	CLKDIV1	I	VDD	Clock frequency selection input 1
2	CLKDIV2	I	VDD	Clock frequency selection input 2
3	VSEL	I	VDD	Card supply voltage selection input; “H”: VREG=5V, “L”: VREG=3V
4	PGND	S	GND	GND for charge pump
5	S2	I/O	-	Capacitor connection for charge pump (between S1/S2): C = 100nF (ESR < 100mΩ)
6	VDDP	S	VDDP	Power supply for charge pump
7	S1	I/O	-	Capacitor connection for charge pump (between S1/S2): C = 100nF (ESR < 100mΩ)
8	VCH	I/O	-	Charge pump output: Decoupling capacitor; Connect C = 100nF (ESR < 100mΩ) between VCH and PGND
9	PRESB	I	VDD	Card presence contact input (active “L”) When PRES or PRESB is active, the card is considered ‘present’ and a built-in debounce feature of 8ms (typ.) is activated. Pulled up to VDD with a 2MΩ resistor.
10	PRES	I	VDD	Card presence contact input (active “H”) When PRES or PRESB is active, the card is considered ‘present’ and a built-in debounce feature of 8ms (typ.) is activated. Pulled down to GND with a 2MΩresistor.
11	IO	I/O	VREG	Card contact I/O data line; Pulled up to VREG with a 11kΩ resistor
12	AUX2	I/O	VREG	Card contact I/O data line; Pulled up to VREG with a 11kΩ resistor
13	AUX1	I/O	VREG	Card contact I/O data line; Pulled up to VREG with a 11kΩ resistor
14	CGND	S	GND	GND
15	CLK	O	VREG	Card clock output
16	RST	O	VREG	Card reset output
17	VREG	O	VREG	Card supply voltage; Connect a capacitor (ESR < 100mΩ) of 100nF - 220nF between VREG and CGND
18 (BD8904F) (BD8904FV) (BD8905F)	PORADJ	I	-	Power-on reset threshold adjustment voltage input ; set with an external resistor bridge
18 (BD8906F) (BD8906FV) (BD8907F)	TEST			Normally used OPEN. Input voltage range: 0V - VDD voltage Can also be used at VDD or GND potential.
19	CMDVCCB	I	VDD	Activation sequence command input; The activation sequence starts by signal input (H→L) from the host
20	RSTIN	I	VDD	Card reset signal input
21	VDD	S	VDD	Input power source pin
22	GND	S	GND	GND
23	OFFB	O	VDD	Alarm output pin (active “L”) NMOS output pulled up to V_{DD} with a 20kΩ resistor
24	XTAL1	I	VDD	Crystal connection or input for external clock
25	XTAL2	O	VDD	Crystal connection (leave open pin when external clock source is used)
26	IOC	I/O	VDD	Host data I/O line; Pulled up to VDD with a 11kΩ resistor
27	AUX1C	I/O	VDD	Host data I/O line; Pulled up to VDD with a 11kΩ resistor
28	AUX2C	I/O	VDD	Host data I/O line; Pulled up to VDD with a 11kΩ resistor

- Pin Function Diagram

Pin No.	Pin Name	Pin Function Diagram
1	CLKDIV1	
2	CLKDIV2	
3	VSEL	
4	PGND	----------
5	S2	
6	VDDP	----------
7	S1	
8	VCH	
9	PRESB	

Pin No.	Pin Name	Pin Function Diagram
10	PRES	
11	IO	
12	AUX2	
13	AUX1	
14	CGND	----------
15	CLK	
16	RST	

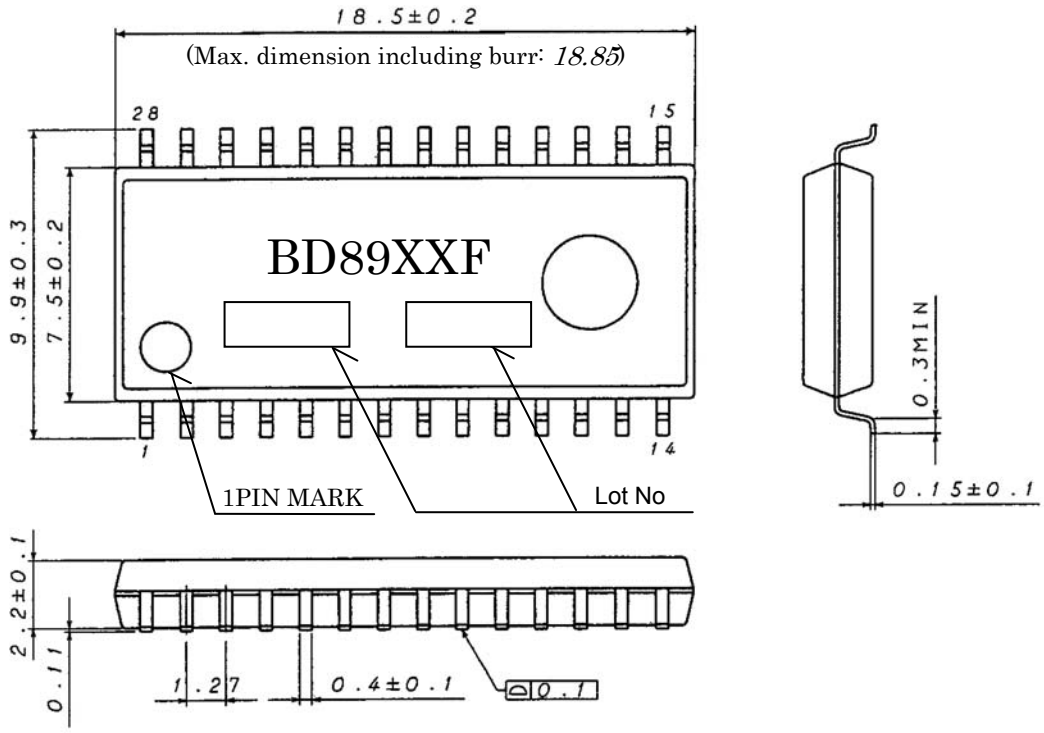
Pin No.	Pin Name	Pin Function Diagram
17	VREG	
18	PORADJ	
	TEST	
19	CMDVCC B	
20	RSTIN	
21	VDD	----------
22	GND	----------

Pin No.	Pin Name	Pin Function Diagram
23	OFFB	
24	XTAL1	
25	XTAL2	
26	IOC	
27	AUX1C	
28	AUX2C	

- Package

For “XX” in the product name below, substitute 04 for BD8904, 05 for BD8905, 06 for BD8906 and 07 for BD8907.

Package Name: SOP28



(UNIT : mm)

Fig. 4-1 SOP28 Package Outer Dimension

Package Name: SSOP-B28

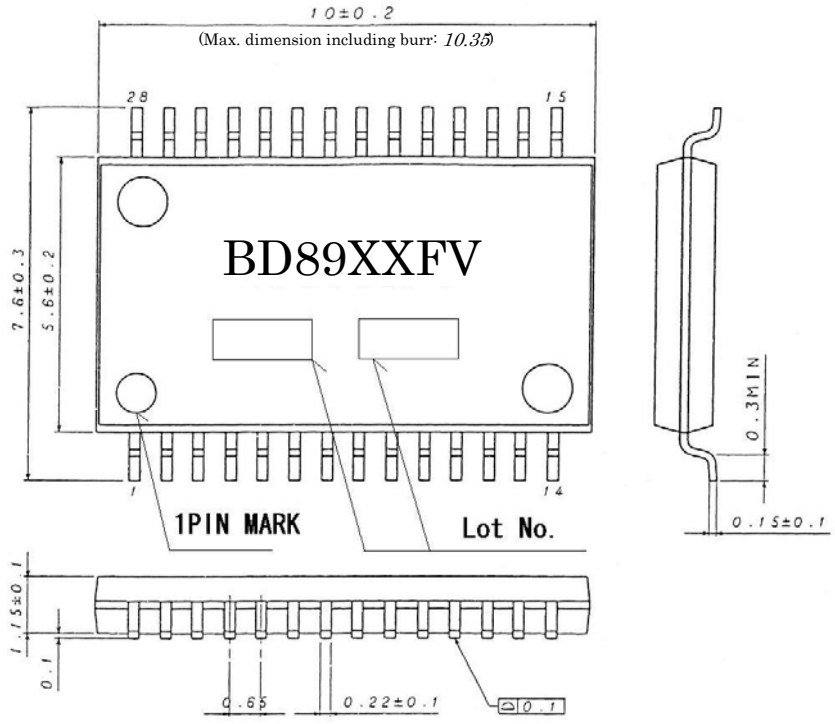


Fig. 4-2 SSOP-B28 Package Outer Dimension

- Function

1) Power Supply

Power supply pins are VDD and VDDP. Set VDD at the same voltage as the signal from the system controller.
VDDP and PGND are the power source and GND for the charge pump circuit, respectively, and the power source for the card.
The VSEL pin setting determines the supply voltage of 3V (VSEL: L) or 5V (VSEL: H) from the VREG pin to the card.

2) VDD input voltage detector

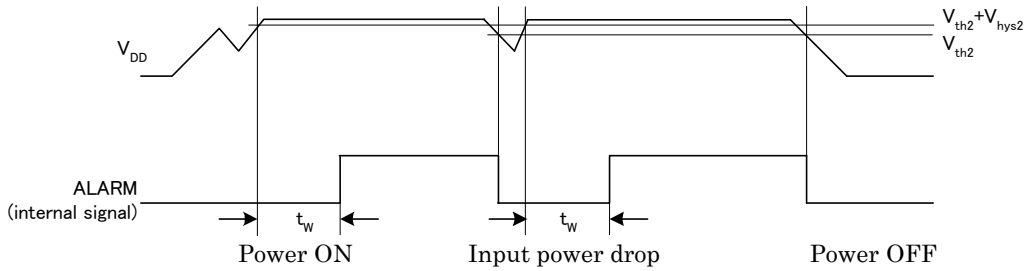
By connecting the resistance bridge (R1, R2: Fig. 3) to the PORADJ pin, you can set the VDD supply voltage detector (V_{DETR}, V_{DETF}: Fig.5). Approximately 16ms (BD8904F/FV, BD8905F) or 8ms (BD8906F/FV, BD8907F) after VDD voltage becomes higher than V_{DETR} (internal reset), power-on reset (alarm) will be cancelled and the IC will go into sleep mode until the CMDVCCB signal turns from H to L.
The IC will initiate the shutdown sequence toward the card contact pin if VDD voltage is decreased below V_{DETF}.

◆ Calculating resistance bridge R1 and R2 for supply voltage detector
(Applicable to BD8904F, BD8904FV and BD8905F; excludes BD8906F, BD8906FV and BD8907F)

The following equations can be used to calculate the alarm reset voltage (V_{DETR}) and low voltage detection voltage (V_{DETF}):
Please ensure that V_{DETF} is set at over 2.3V.

PORADJ pin voltage at VDD startup: VDD_{THR}
PORADJ pin voltage at VDD shutdown: VDD_{THF}

$$V_{DETR} = \left(\frac{R1}{R2} + 1\right) \times VDD_{THR} \qquad V_{DETF} = \left(\frac{R1}{R2} + 1\right) \times VDD_{THF}$$



tw = (BD8904F/FV, BD8905F): 16ms, (BD8906F/FV, BD8907F): 8ms

Fig. 5 VDD Input Voltage Detection

3) Operation sequence

3-1) Wait mode

When VDD voltage becomes higher than V_{DTER}, power-on reset (alarm) is released and the IC will be in wait mode until the CMDVCCB signal turns from H to L.
In this mode, the VDD supply voltage detector (VDET), thermal shutdown circuit (TSD), reference circuit (VREF), crystal oscillation circuit (XT OSC) and internal oscillator circuit (OSC) are activated.
IOC, AUX1C and AUX2C are pulled up to VDD with an 11kΩ resistor and all the card contact pins are at Lo level.

3-2) Card insertion

Card presence is detected by PRES pin or PRESB pin. When either of the PRES pin or PRESB pin is active, a card is assumed to be present.

Table 1

PRES	“High” active
PRESB	“Lo” active

When a card is present in sleep mode, either one of the card presence identification pins, PRES (“H” active) or PRESB (“L” active) becomes active. OFFB will become “H” after approximately 8ms (debounce time).
If a card is present before the VDD power source is applied and the internal reset is released, it is internally reset and OFFB becomes “H” after the debounce time.
The PRES pin is pulled down to GND with a 2MΩ resistor and the PRESB pin is pulled up to VDD with a 2MΩ resistor.

3-3) Activation sequence

When OFFB is in the “High” state and the CMDVCCB signal from the controller turns from H to L, the activation sequence starts to activate each functional block in the following order:

The RST outputs signals based on the RSTIN input, being reset approximately 200μsec after the CMDVCCB signal turns from H to L. The RSTIN input becomes effective approximately 300ns after I/O TRANS turns ON. If RSTIN becomes Lo after RSTIN becomes effective and before RST output is released, the CLK signal is output. If RSTIN is High when the RST output is released, the CLK signal is output as soon as the RST output is released. (Refer to Fig. 6-1, Fig. 6-2 and Fig. 6-3)

CHARGE PUMP ON (VCH voltage output)

↓

CARDREG ON (VREG output)

↓

I/O TRANS ON (All I/O Bus: Pull-up)

↓

↓ (RSTIN≠Always High)

↓

CLK BUF ON (CLK output)

↓

RST BUF ON (RST release)

↓ When RSTIN remains High until RST is released

↓(RSTIN=Always High)

↓

CLK, RST BUF ON (CLK output, RST release)

[Activation sequence under different RSTIN input timings]

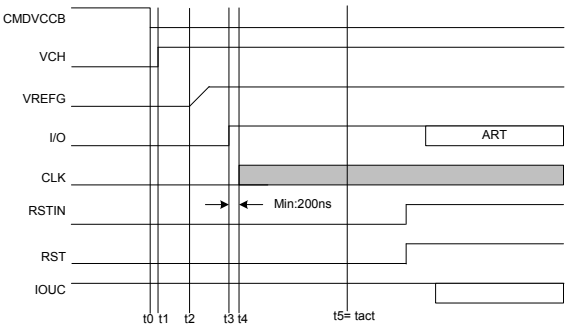


Fig. 6-1 Activation sequence 1

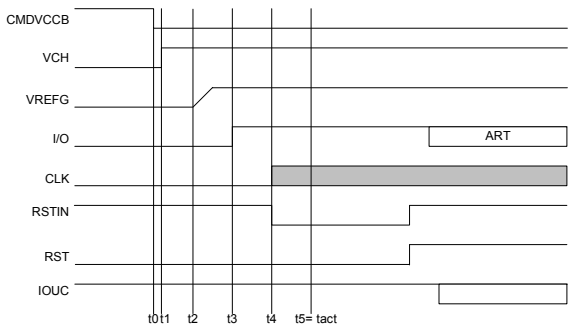


Fig. 6-2 Activation sequence 2

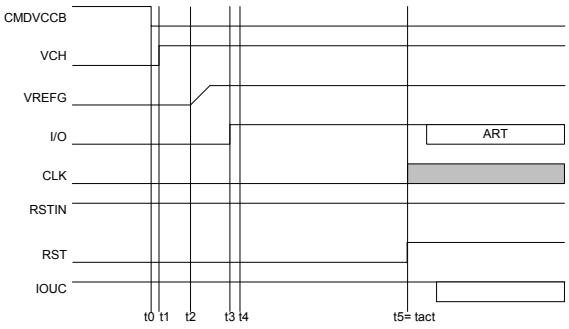


Fig. 6-3 Activation sequence 3 (not supported by ISO7816-3)

t1: VCH startup time = typ 21.4 μ s, (max. 30 μ s)

t2: VREG startup time = typ 57 μ s, (max. 80 μ s)

t3: I/O ON time = typ 116.2 μ s, (max. 150 μ s)

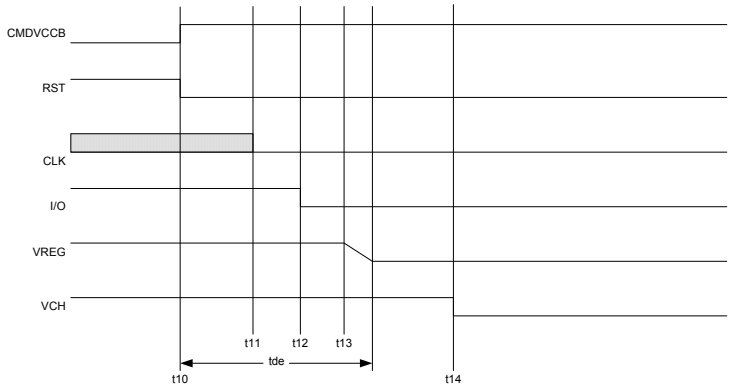
t4: CLK output release time (t4-t3)= Min 200ns, (max. 450 μ s)

t5: RST release time (activation time) = typ 187.4 μ s, (max. 240 μ s)

3-4) Deactivation sequence

When the CMDVCCB input turns from L to H or the alarm signal (described later) is detected, the following deactivation sequence is initiated in the following order transitioning to the wait mode.

RST BUF OFF (RST: Lo)
↓
CLK BUF OFF (CLK: Lo)
↓
I/O TRANS OFF (I/O Bus on the controller side: Pull-up)
↓ (I/O Bus on the card side: Lo)
↓
CARDREG OFF (VREG: Lo)
↓
CHARGE PUMP OFF



t11: CLK OFF time = typ. 11.9 μs
t12: I/O OFF time = typ. 23.7 μs
t13: Start time of VREG fall = typ. 35.6 μs
t14: Start time of VCH fall = typ. 118.5 μs
tde: Operational sequence completion time= Max. 100 μs

Fig. 7 Deactivation sequence

4) CHARGE PUMP

The charge pump circuit is the power supply for CARD REG output. It activates when the CMDVCCB input turns from H to L. It functions as a voltage doubler or voltage follower by the VDDP voltage.

The VCH output becomes a power source for the CARDREG circuit.

As the charge pump circuit takes a high charge current, place two capacitors (one between S1-S2, and the other between VCH-PGND) as close as possible to the IC so that the ESR becomes less than 100mΩ. Also, place a capacitor between VDDP and PGND as close as possible to the IC so that the ESR becomes less than 100mΩ.

5) CARD REG

CARD REG supplies power to the IC card through the VREG pin.

The VREG output voltage can be switched between 3V and 5V by the VSEL pin setting.

Table 2 VSEL pin setting

VSEL	VREG output voltage	VDDP Input Voltage	MAX current	Remark
0	3V	3.0V ≤ VDDP ≤ 5.5V	60mA	
1	5V	3.0V ≤ VDDP < 4.5V	20mA	Except BD8904FV
		3.0V ≤ VDDP < 3.1V	20mA	Application to BD8904FV
		3.1V ≤ VDDP < 4.5V	25mA	
		4.5V ≤ VDDP ≤ 5.5V	60mA	

This regulator has an over-current limiter circuit. It generates an internal alarm with a load current of approximately 140mA or more and enters into the deactivation sequence. Also, the output voltage is regarded as abnormal if it becomes less than 0.6V in the case where VREG is 3V or becomes less than 1V in the case where VREG is 5V, and the output current is shut off. At this point, an internal alarm signal is generated and the deactivation sequence is initiated.

Connect a capacitor of 100nF, 220nF or 330nF between VREG and CGND as close as possible to the VREG pin, in order to reduce the output voltage variation as much as possible. Also, ensure that ESR is kept at less than 100mΩ.

CARD REG output is also a power source for the CLK and RST output. Therefore, the CLK and RST output level is the same as the VREG output level.

6) I/O data transitions

Three data lines, IOC - IO, AUX1C - AUX1 and AUX2C - AUX2 transmit two-way data independently of each other.
Pins for the controller side, IOC, AUX1C and AUX2C are pulled up with an 11kΩ resistor to High (VDD voltage) and card contact pins, IO, AUX1 and AUX2 are set to Lo until I/O TRANS becomes ON during the activation sequence.
When I/O TRANS becomes On, IC becomes idle mode and all the I/O pins are pulled up with an 11kΩ. The IOC, AUX1C and AUX2C pins keep VDD voltage (High) and the IO, AUX1 and AUX2 pins go to' VREG voltage (High).

The pin which turns from H to L first becomes the master and the other output side becomes the slave between the pins on the controller side and card contact pins. Then the data are transferred from the master side to the slave side.
When both signal levels become High, they become idle.
When the signal transits from L to H and it passes over a threshold, an active pull-up (100 ns or less) works to drive the data High at high speed. After the active pull-up is completed, the pin is pulled up with an 11kΩ resistor. This function enables signal transmission up to 1MHz. Also, an over-current limiter of 15mA works in the card contact pins, IO, AUX1 and AUX2.

7) Card clock supply

Card clock is supplied from the CLK pin divides the input frequency of XTAL1 pin by 1, 1/2, 1/4 and 1/8 with the CLKDIV1 and CLKDIV2 pin setting. The clock division switching time is within the 8 clocks of the XTAL1 signal (refer to Table 3).
The input signal to the XTAL1 pin is made by a crystal oscillator (2MHz - 26MHz) between the XTAL1 pin and XTAL2 pin or external pulse signal.
To ensure the duty factor of 45% - 55% at the CLK pin, the duty of the XTAL1 pin should be 48% - 52% and the transition time should be within 5% of the frequency.
To guarantee a 45% - 55% duty, use it with a clock division of 1/2, 1/4 or 1/8 depending on the wiring layout on the PCB.

Table 3 Clock frequency selection (f_{XTAL}: Frequency of XTAL1)

CLKDIV1	CLKDIV2	f_{clk}
0	0	$\frac{f_{XTAL}}{8}$
0	1	$\frac{f_{XTAL}}{4}$
1	1	$\frac{f_{XTAL}}{2}$
1	0	$\frac{f_{XTAL}}{1}$

8) RSTIN input, RST output

The RSTIN input becomes effective after the CMDVCCB signal input turns from H to L, activation sequence is initiated and approximately 300ns after I/O TRANS turns ON. The RST output is released in approximately 200μsec after the CMDVCCB signal turns from H to L to output signal based on the RSTIN input.

9) Fault detection

When the following fault state is detected, the circuit enters the wait mode after it generates an internal alarm signal and is deactivated.
If a card is not present, it remains in the wait mode.

- When the VREG pin becomes less than 1V (VSEL=H) or 0.6V (VSEL=L), or is loaded high current(TYP: 150mA)
- When the VDD voltage is less than the threshold voltage (detected by supply voltage detector)
- When an overheating is detected by the thermal shutdown circuit
- When VCH pin voltage drops to an abnormal level
- When the card is removed during operation or the card is not present from the beginning (PRES=L and PRESB=H)

10) OFFB output

The OFFB output pin indicates that the IC is ready to operate. It is pulled up to VDD with a 20kΩ resistor.
When the IC is in ready state, OFFB is High.
The OFFB outputs OFF state (Lo) when a fault state is detected.
When a card is present, the fault state is released and CMDVCCB becomes High, the internal alarm is released and the OFFB output becomes High.

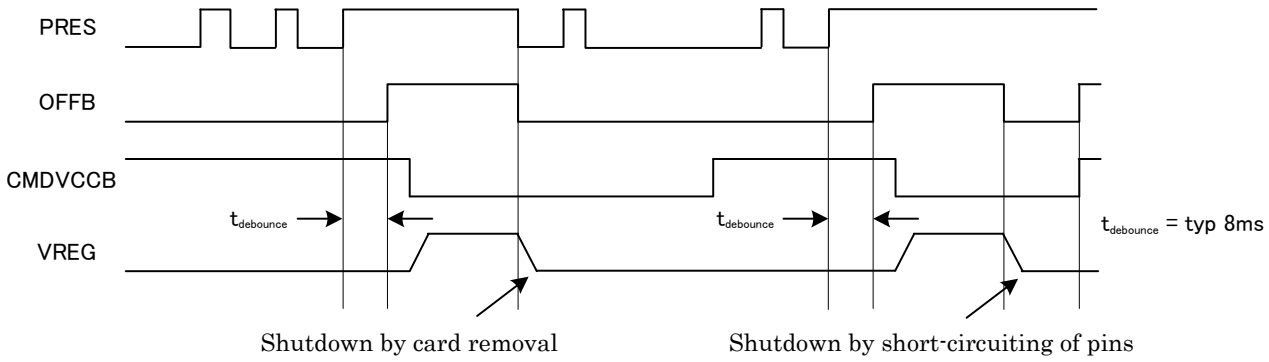


Fig. 8 OFFB, CMDVCCB, PRES, VREG operation

- An example of software control

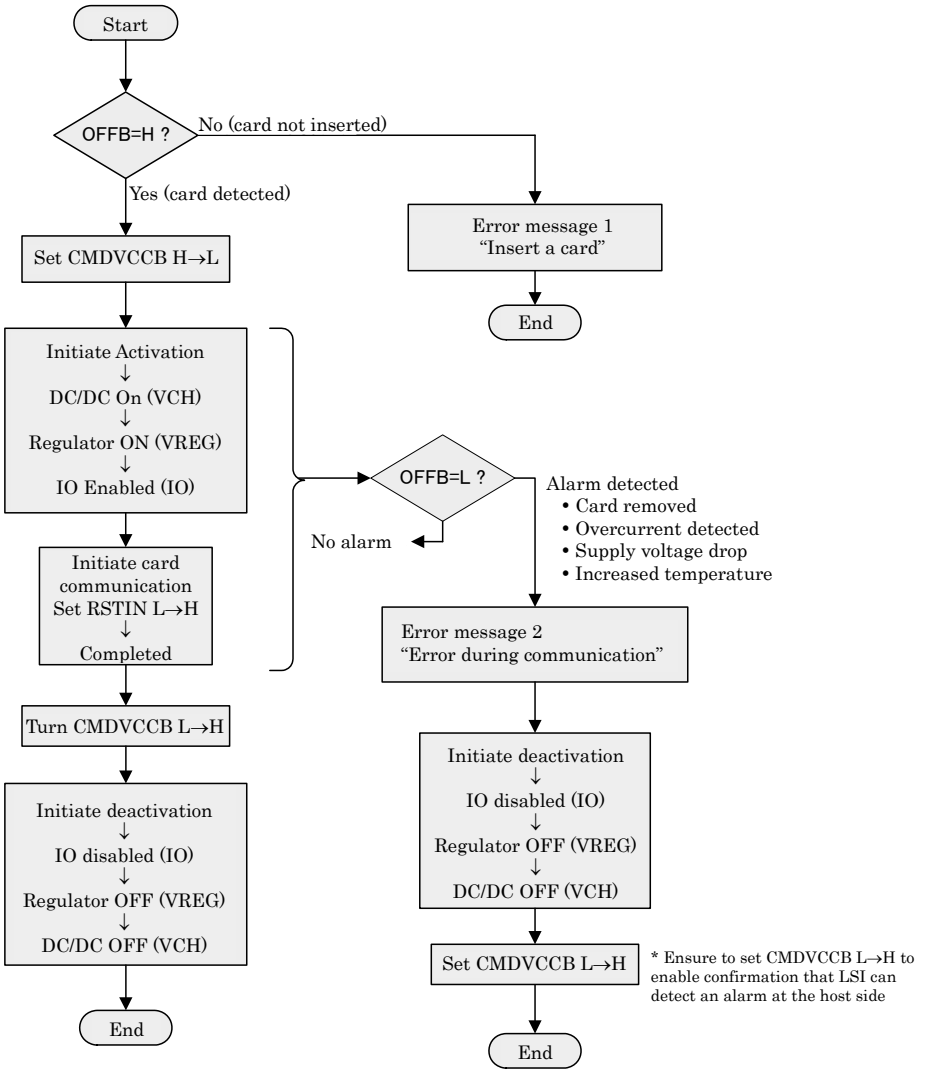
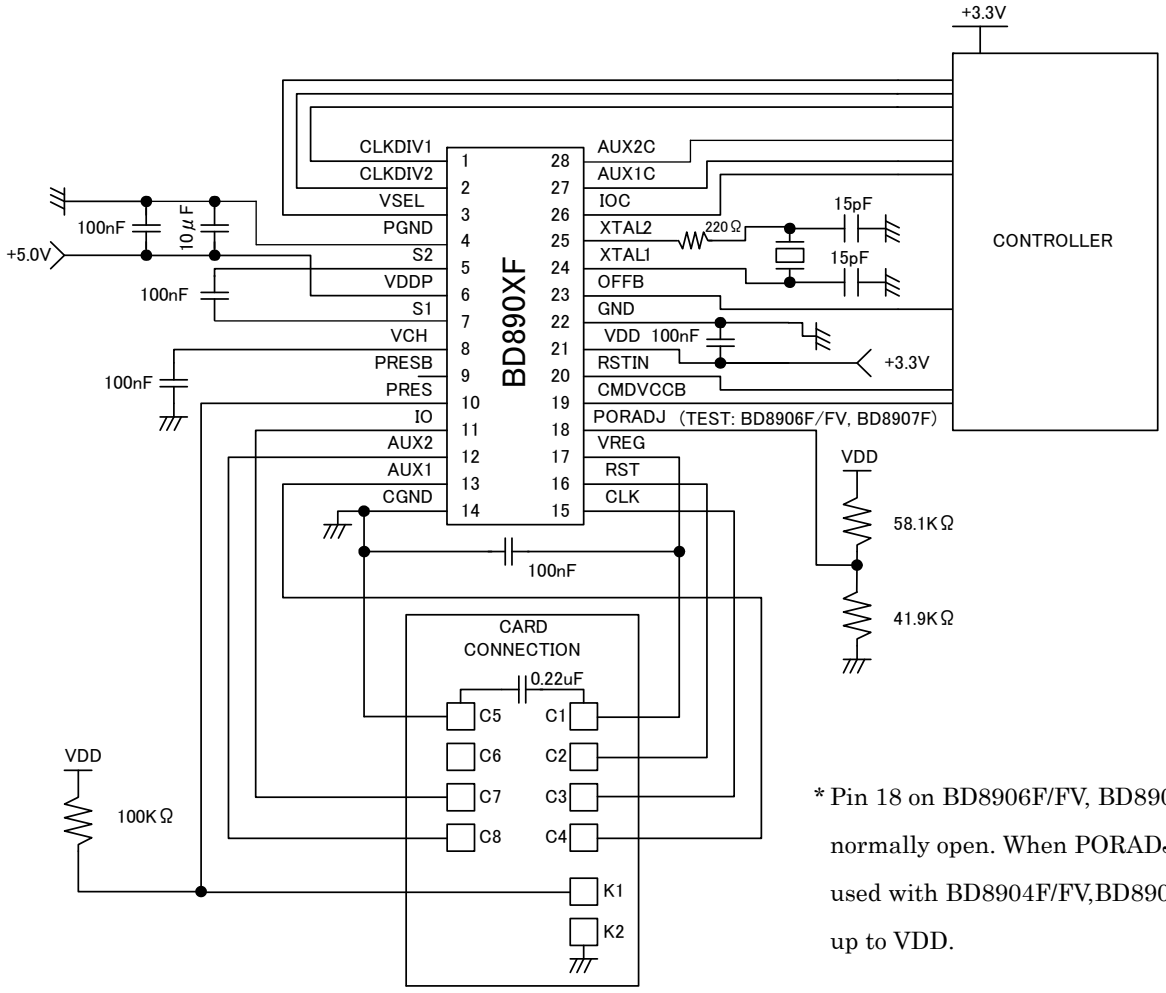


Fig. 9 An example of software control

- Application examples

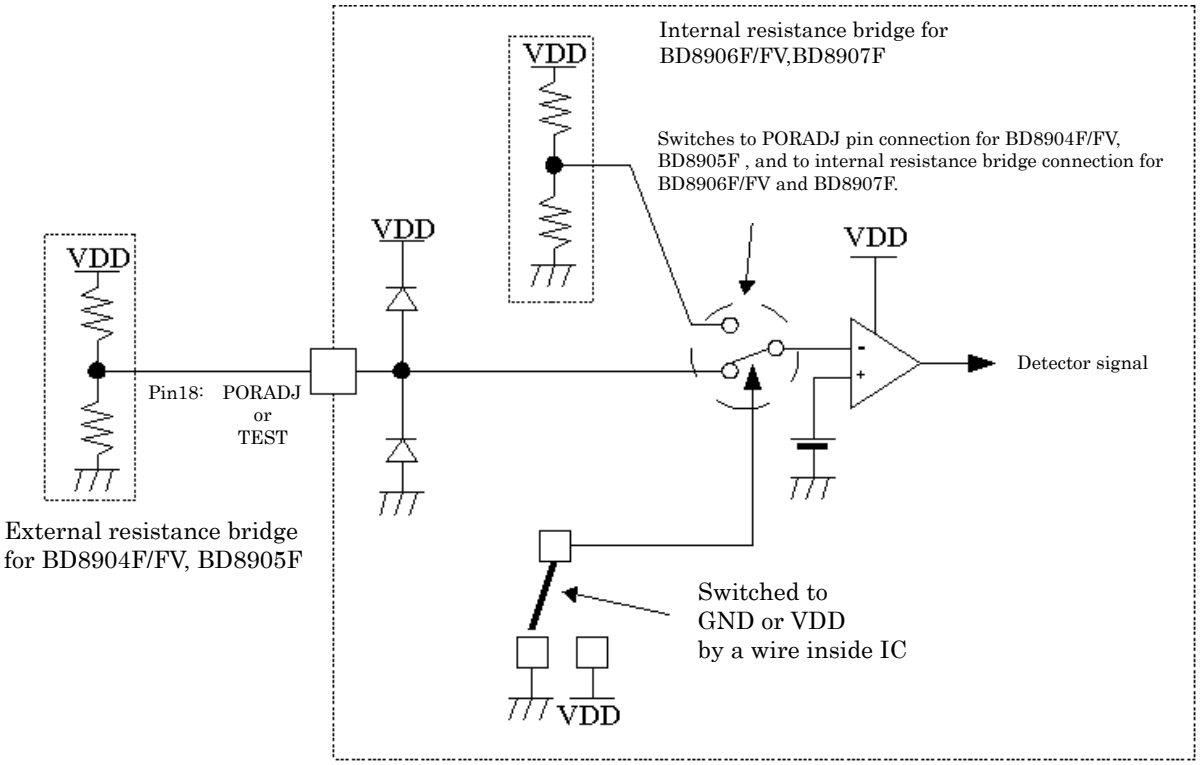


* Pin 18 on BD8906F/FV, BD8907F is normally open. When PORADJ is not used with BD8904F/FV,BD8905F, pull it up to VDD.

Fig. 9

- Function of pin 18 on different devices

  The function of pin 18 (PORADJ/TEST) for BD8904F/FV and BD8905F is different from BD8906F/FV and BD8907F; switched as indicated in the following diagram but the common chip is used.



- Precautions for use

1) Two capacitors for a charge pump should be placed as close as possible to the IC between S1 and S2 and between VCH and PGND so that the ESR becomes less than 100mΩ.
2) The capacitor for the VREG pin should be placed as close as possible to the IC between VREG and CGND so that the ESR becomes less than 100mΩ.
3) Connect capacitors of over 10μF+0.1μF between VDD and GND and between VDDP and GND as close as possible to the IC so that the ESR becomes less than 100mΩ to reduce the power line noise. We recommend the use of capacitors with the largest possible capacitance.

●Selection of order type

B	D	8	9	0	4		F		—	E	2

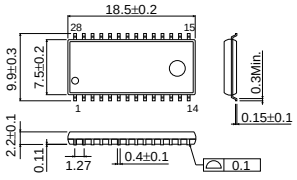
ROHM model name

Package type
F : SOP28
FV : SSOP-B28

Packaging and forming specification
E2 =Reel-shaped emboss taping

SOP28

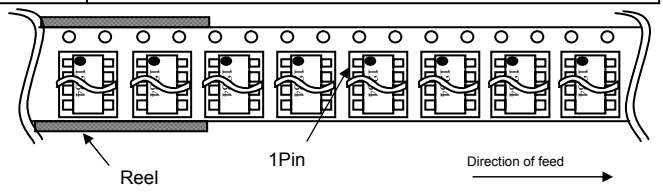
<Dimension>



(Unit:mm)

<Tape and Reel information>

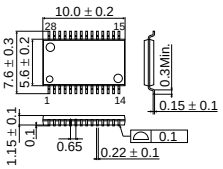
Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

SSOP-B28

<Dimension>



(Unit:mm)

<Tape and Reel information>

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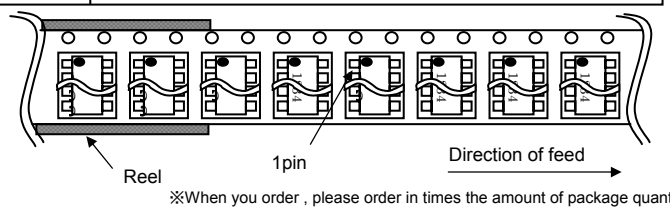
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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