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DC to 12 GHz, CASCADABLE pHEMT MMIC AMPLIFIER

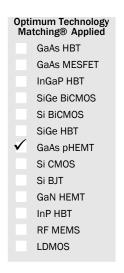
Package: QFN, 16-Pin, 3mmx3mm

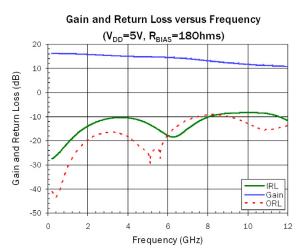




Product Description

RFMD's SUF-8533 is a monolithically matched high IP $_3$ broadband pHEMT MMIC amplifier covering DC to 12GHz. This pHEMT FET based amplifier uses a self-bias Darlington topology featuring a gain and temperature compensating active bias network that operates from a single 5V supply. It offers efficiency, cascadable performance in a compact 3mmx3mm Ceramic QFN package. It is well suited for RF, LO, and IF driver applications.





Features

- Broadband Performance
- Gain = 15.4 dB at 3 GHz
- $P_{1dB} = 16.7 \, dBm$ at $3 \, GHz$
- Low-Noise, Efficient Gain Block
- 5V Single Supply Operation
- Low Gain Variation versus Temperature

Applications

- Broadband Communications
- Test Instrumentation
- Military and Space
- LO and IF Mixer Applications
- High IP₃ RF Driver Applications

Davamatar		Specification		Unit	Condition	
Parameter	Min.	Тур.	Max.	Unit		
Frequency of Operation	DC		12.0	GHz		
Small Signal Power Gain, G _P		15.4		dB	Freq=3GHz	
		14.6		dB	Freq=6GHz	
		11.7		dB	Freq=10GHz	
Output Power at 1dB Compression		16.7		dBm	Freq=3GHz	
		16.8		dBm	Freq=6GHz	
		14.6		dBm	Freq=10GHz	
Output Third Order Intercept Point		27.1		dBm	Freq=3GHz	
		25.7		dBm	Freq=6GHz	
		23.5		dBm	Freq=10GHz	
Input Return Loss		10.7		dB	Freq=3GHz	
Output Return Loss		22.3		dB	18W resistor between V _D and V _{DD} , Freq=3GHz	
Device Operating Voltage		4.0		V		
Current		58		mA		
Noise Figure, NF		4.0		dB	Freq=3GHz	
Thermal Resistance		159		°C/W	Junction to backside	

 $Test\ Conditions: Z_0 = 50\Omega,\ V_S = 5V,\ I_D = 58\,\text{mA},\ R_{BIAS} = 18.0\Omega,\ T = 25\,^{\circ}\text{C},\ OIP_3\ Tone\ Spacing = 1\,\text{MHz}\ with\ P_{OUT/TONE} = 0\,\text{dBm}.\ Circuit\ board\ data\ with\ bias\ tees.$

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Absolute Maximum Ratings

Parameter	Rating	Unit
Total Current (I _D)	90	mA
Device Voltage (V _D)	5.5	V
Power Dissipation	495	mW
RF Input Power	+20	dBm
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range (T _L)	-40 to +85	°C
Operating Junction Temperature (T _J)	+150	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one. Bias Conditions should also satisfy the following expression: $I_DV_D < (T_J - T_L)/R_{TH}, j - I \text{ and } T_L = \text{Backside of die}$



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective 2002/95/EC (at time of this document revision).

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Typical Performance (Circuit Board with Bias Tees) V $_{S}$ = 5V, R $_{BIAS}$ = 18.0 Ω , T = 25 $^{\circ}$ C, Z = 50 Ω

Parameter	Units	500 MHz	1.5 GHz	3.5GHz	6.5GHz	9.5GHz	12GHz
Small Signal Gain	dB	16.2	16.0	15.1	14.5	11.8	10.9
Output 3rd Order Intercept Point (see note 1)	dBm	28.7	28.1	26.3	25.2	23.5	23.5
Output Power at 1dB Compression	dBm	17.3	17.1	16.3	16.3	14.5	13.4
Input Return Loss	dB	25.3	16.7	10.3	17.9	8.4	11.7
Output Return Loss	dB	41.6	23.6	16.8	13.7	11.2	13.9
Reverse Isolation	dB	22.0	22.1	22.4	22.0	22.9	22.8
Noise Figure	dB	4.6	3.6	4.0	4.2	4.8	4.8

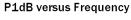
Note 1: OdBm/tone, 1MHz tone spacing

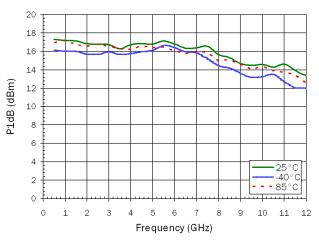


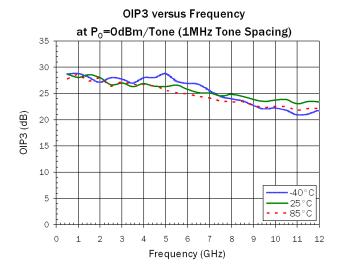
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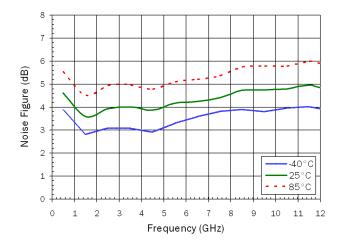
Typical Performance (Probe Data with Bias Tees) V_S =5V, I_D =58mA, R_{BIAS} =18.0 Ω





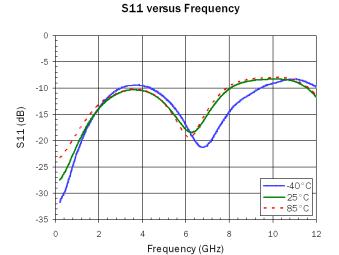


Noise Figure versus Frequency

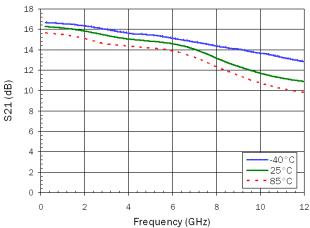




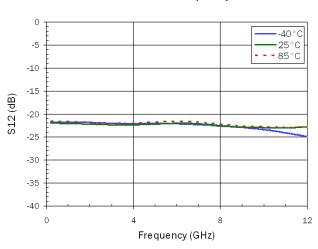
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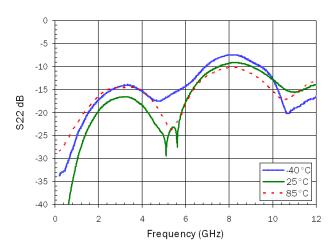
S21 versus Frequency



S12 versus Frequency



S22 versus Frequency



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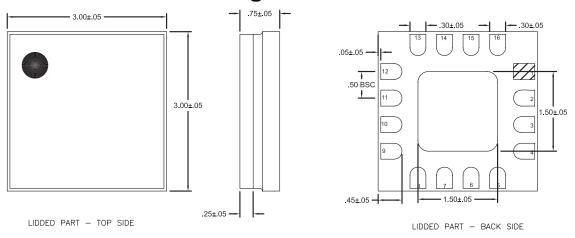
r	f	r	n	d	c	o	n	1

Pin	Function	Description			
2	RF IN	This pad is DC coupled and matched to 50Ω . An external DC block is required.			
11	RF OUT/BIAS	This pad is DC coupled and matched to 50Ω . DC bias is applied through this pad.			
Pkg	GND	Package bottom must be connected to RF/DC ground.			
Bottom					

Notes:

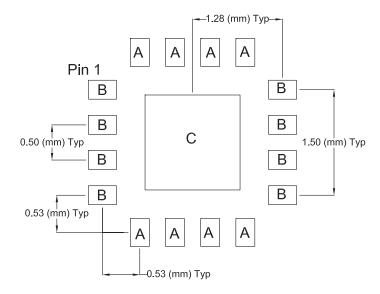
- 1. All dimensions in millimeters.
- 2. Backside is ground.

Package Dimensions



PCB Stencil Drawing

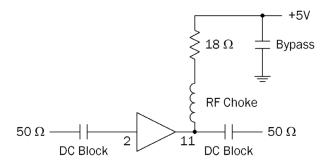
 $A = 0.27 \times 0.40 \text{ (mm) Typ.}$ $B = 0.40 \times 0.27 \text{ (mm) Typ.}$ C = 1.35 (mm) Sq.



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Device Assembly



Ordering Information

Part Number	Description	Devices/Container
SUF-8533	QFN, 16-Pin, 3mmx3mm	
SUF-8533PCBA-410	Evaluation Board	