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SUF-5033

0.1GHZ TO 4.0GHZ, CASCADABLE PHEMT MMIC AMPLIFIER

Package: QFN, 16-Pin, 3mmx3mm

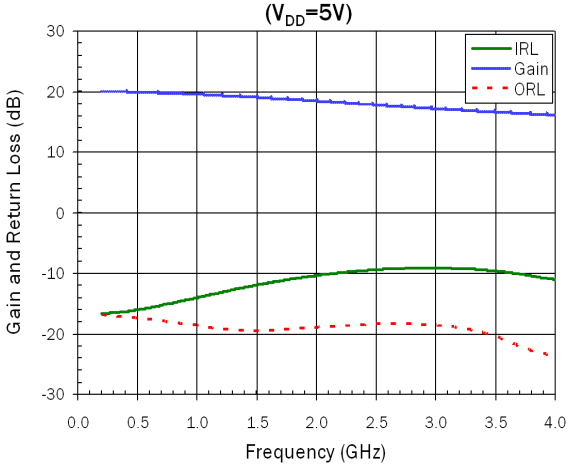
Product Description

The SUF-5033 is a monolithically matched broadband high IP3 gain block covering 0.1GHz to 4.0GHz. This pHEMT FET-based amplifier uses a patented self-bias Darlington topology featuring a gain and temperature compensating active bias network that operates from a single 5V supply. It offers efficient, cascadable performance in a compact 3mmx3mm Ceramic QFN package. It is well-suited for RF, LO, and IF driver applications.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☑ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS

Gain and Return Loss versus Frequency
(V_{DD}=5V)



Features

- Broadband Performance
- High Gain=18.5dB at 2GHz
- P1dB=20.5dBm at 2GHz
- 50Ω I/O Low-Noise, Efficient Gain Block
- 5V Operation, No Dropping Resistor
- Low Gain Variation versus Temperature
- Patented Self-Bias Darlington Circuit

Applications

- Broadband Communications
- Test Instrumentation
- Military and Space
- LO and IF Mixer Applications
- High IP3 RF Driver Applications

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency of Operation	0.1		4.0	GHz	
Small Signal Power Gain	16.0	18.5		dB	2GHz
		16.0		dB	4GHz
Output Power at 1dB Compression		21.0		dBm	2GHz
		21.5		dBm	4GHz
Output Third Order Intercept Point		27.6		dBm	2GHz
		27.9		dBm	4GHz
Noise Figure		3.6		dB	2GHz
		4.0		dB	4GHz
Input Return Loss		-10.3		dB	2GHz
		-11.1		dB	4GHz
Output Return Loss		-19.0		dB	2GHz
		-23.8		dB	4GHz
Reverse Isolation		-24.0		dB	2GHz
		-23.0		dB	4GHz
Device Operating Voltage		5.0		V	
Device Operating Current		90		mA	
Gain Variation vs. Temperature		-0.01		dB/°C	
Thermal Resistance		100		°C/W	junction to backside

Test Conditions: V=5V, I_D=90mA OIP_3 Tone Spacing=1MHz, P_{OUT} per tone=0dBm, Z_S=Z_L=50Ω, 25°C, With Bias Tees

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Absolute Maximum Ratings

Parameter	Rating	Unit
Max Device Current (I_D)	110	mA
Max Device Voltage (V_D)	5.5	V
Max RF Input Power	20	dBm
Max Dissipated Power	605	mW
Max Junction Temperature (T_J)	150	°C
Operating Temperature Range (T_L)	-40 to + 85	°C
Max Storage Temperature	-65 to +150	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L)/R_{TH}$, j-l and T_L = Backside of die

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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Typical Performance (Circuit Board Data with Bias Tees) V_S=5V, R_{BIAS}=20Ω, T=25°C, Z=50Ω

Parameter	Units	200MHz	500MHz	1GHz	2GHz	4GHz
Small SIgnal Gain	dB	20.1	19.9	19.6	18.5	16.2
Output 3rd Order Intercept Point (see note 1)	dBm			28.5	27.6	27.9
Output Power at 1dB Compression	dBm	21.2	21.4	21.5	21.0	21.5
Input Return Loss	dB	16.6	16.0	14.0	10.3	11.1
Output Return Loss	dB	16.9	17.5	18.7	19.0	23.8
Reverse Isolation	dB	24.6	24.6	24.6	24.5	23.2
Noise Figure	dB			3.0	3.6	4.0

Note 1: 0dBm/tone, 1MHz tone spacing

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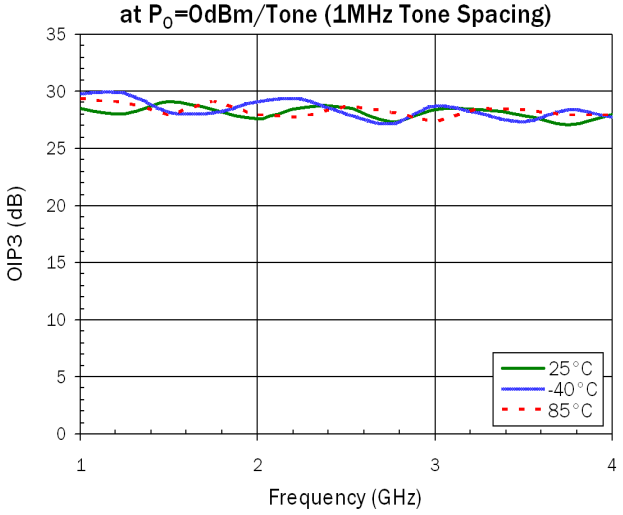
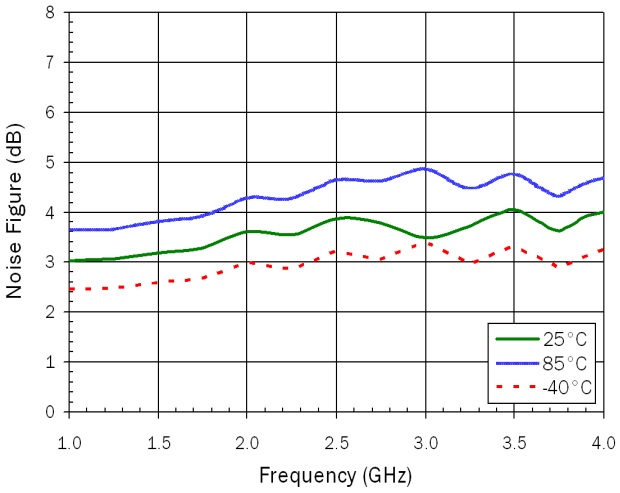
Typical Performance

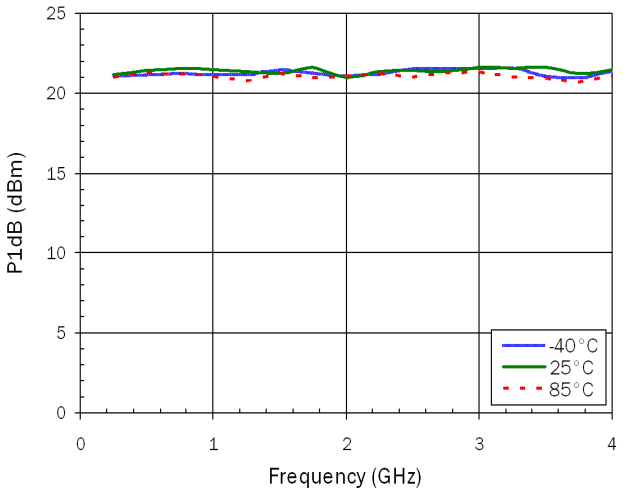
OIP3 versus Frequency
at P_0=0dBm/Tone (1MHz Tone Spacing)



Noise Figure versus Frequency



P1dB versus Frequency



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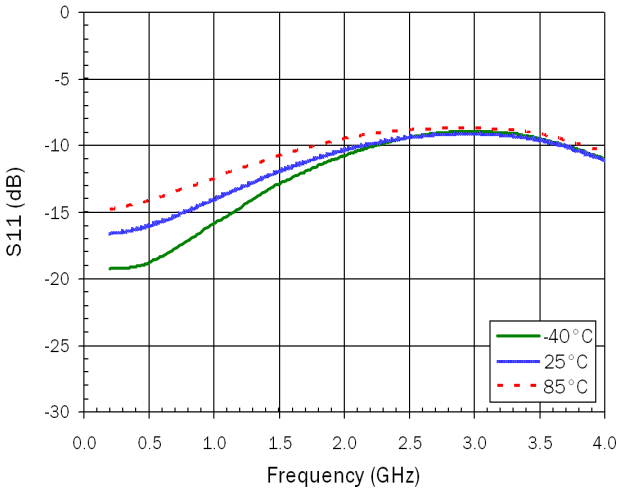
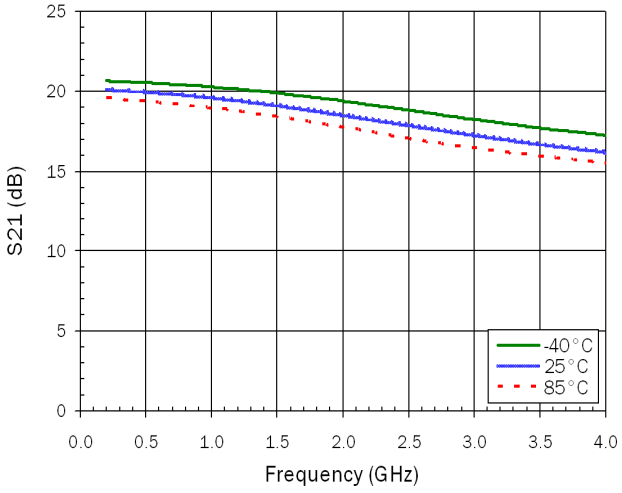
Typical Performance

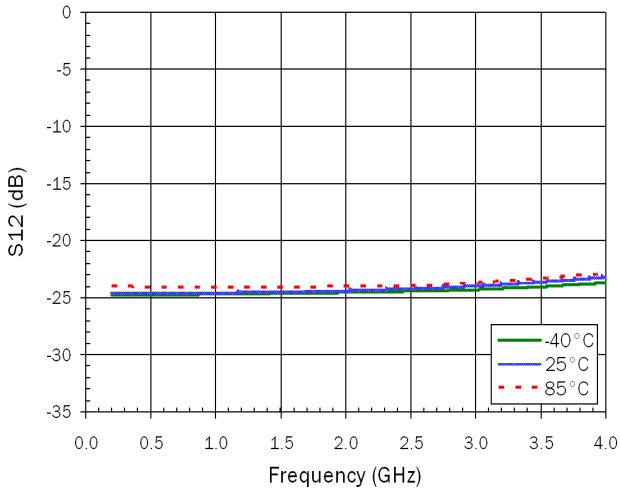
S11 versus Frequency



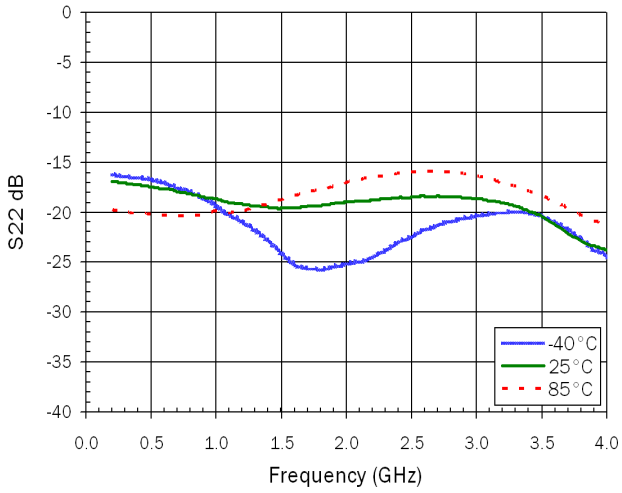
S21 versus Frequency



S12 versus Frequency



S22 versus Frequency



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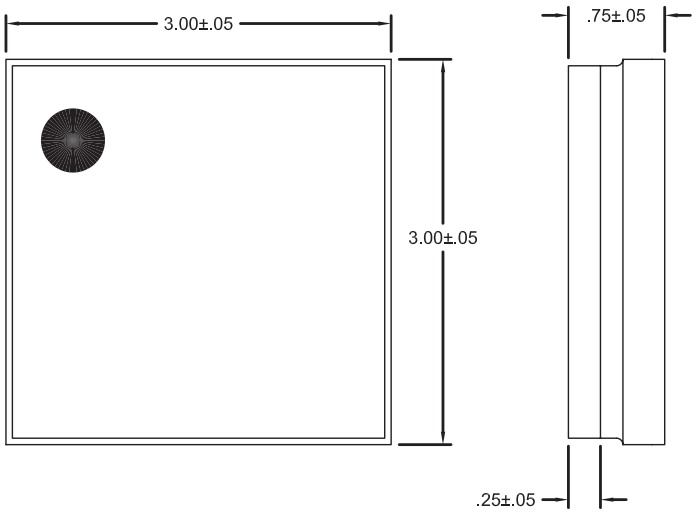
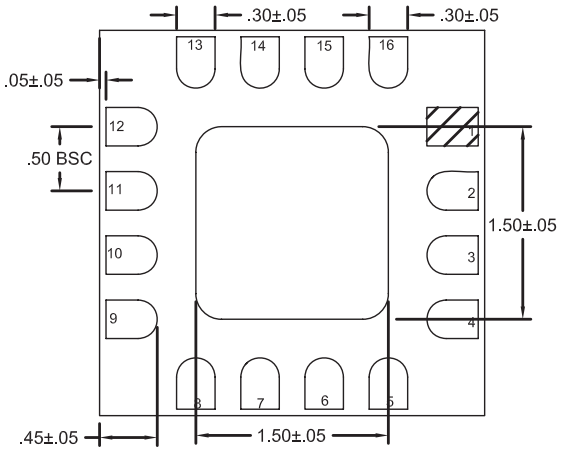
Pin	Function	Description
2	RFIN	This pad is DC coupled and matched to 50Ω. An external DC block is required.
11	RFOUT/BIAS	This pad is DC coupled and matched to 50Ω. Bias is applied through this pad.
Pkg Bottom	GND	Package bottom must be connected to RF/DC ground.

Package Drawing



LIDDED PART – TOP SIDE



LIDDED PART – BACK SIDE

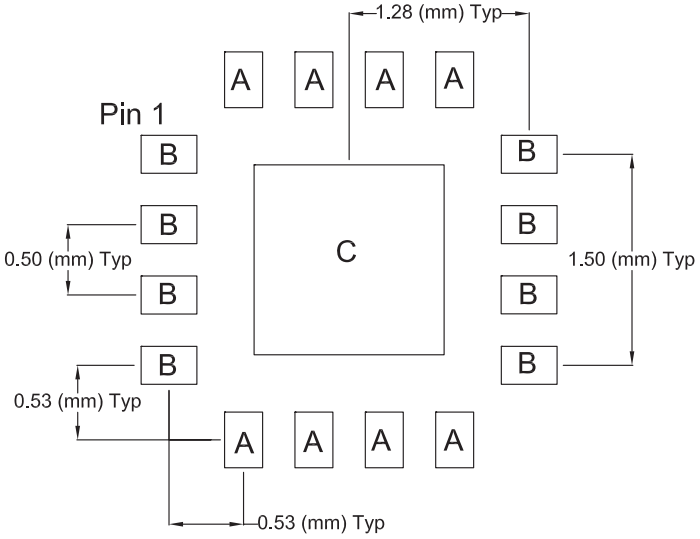
Notes:

1. All dimensions in millimeters.

2. Backside is ground.

PCB Stencil Drawing

A = 0.27 x 0.40 (mm) Typ.
B = 0.40 x 0.27 (mm) Typ.
C = 1.35 (mm) Sq.



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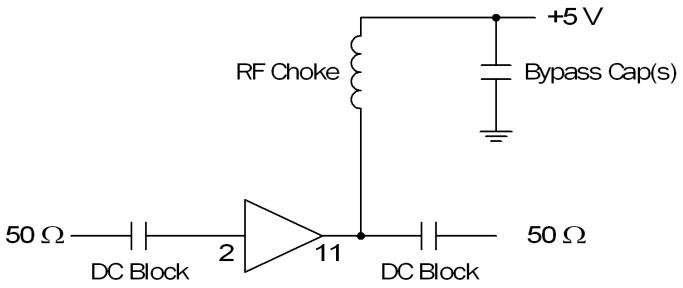
Device Assembly



Ordering Information

Part Number	Description	Devices/Container
SUF-5033	QFN, 16-Pin,3mmx3mm	
SUF-5033PCBA-410	2.45GHz Evaluation Board	N/A

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