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April 1st, 2010
Renesas Electronics Corporation

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MOS Integrated Circuit

RENESAS

μPD78F8056, 78F8057, 78F8058

16-BIT SINGLE-CHIP MICROCONTROLLER

The μ PD78F8056, 78F8057, 78F8058 products are a 16-bit single-chip microcontroller of the 78K0R series. This microcontroller features 2.4 GHz RF transceiver function and many peripherals.

1. FEATURES

- 78K0R 16-bit CPU core
- 2.4 GHz RF transceiver included
- Flash Memory and RAM size

Item / Product Number	Flash Memory	RAM
μ PD78F8056[Note 1]	64 K bytes	8 K bytes[Note 2]
μ PD78F8057[Note 1]	96 K bytes	8 K bytes[Note 2]
μ PD78F8058[Note 1]	128 K bytes	8 K bytes[Note 2]

Notes 1. under development

2. This is 7 KB when the self-programming function is used.

Minimum instruction cycle

0.05μ s (f_{MX} = 20 MHz operation)

61μ s (f_{SUB} = 32.768 KHz operation)

Clock

- HIGH SPEED CLOCK
  - High-speed internal oscillator
    1 MHz (Typ.), 8 MHz (Typ.), 20 MHz (Typ.)
  - Ceramic/Crystal Oscillator/External CLK
    2 MHz to 20 MHz (V_{DD} = 2.7 V to 3.6 V)
    2 MHz to 5 MHz (V_{DD} = 1.8 V to 3.6 V)
- LOW SPEED CLOCK
  - Low-speed internal oscillator for WDT
    Clock speed : 30 KHz (Typ.)
- SUBSYSTEM CLOCK
  - Crystal oscillator
    32.768 KHz (TYP.): V_{DD} = 1.8 V to 3.6 V

Function

- 2.4 GHz RF transceiver
  - IEEE802.15.4-2006 specification compatible
    (Modulation: O-QPSK, Spectrum: DSSS
    Transmission speed:250 kbps)
- Self-programming
- On-Chip debugging
- Power-On-Clear (POC) circuit
- Low-Voltage Detector (LVI) circuit
- Multiplier(16 bits x 16 bits)
- Divider (32 bits ÷ 32 bits)
- BCD correction
- DMA 2 channel
- Timer
  - 16bit Timer: 12 channels
    (Unit 0: 8 channels, Unit1: 4 channels)
  - Watchdog Timer: 1 channel
  - Real Time Counter: 1 channel
- Serial Interface
  - CSI: 1 channel (dedicated to RF transceiver communication at internal connection)
  - CSI / UART: / Simplified I^2C: 1channel
  - UART (Tx Only) : 1 channel
  - UART (LIN supported) : 1 channel
- I/O PORT
  - CMOS I/O : 12[Note]
  - CMOS Input : 4[Note]
  - CMOS Output : 1[Note]
  - N-ch Open Drain I/O : 1[Note]

Operation Voltage

1.8 V to 3.6 V

Operating ambient temperature

TA = −40 to +85°C

Package

56-pin QFN (8 x 8) (0.5 mm pitch)

Note Include External Connection on the PCB by users between MCU and RF transceiver.

This information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production. Not all products and/ or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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2. OUTLINE OF FUNCTIONS

Item		μ PD78F8056[Note 1]	μ PD78F8057[Note 1]	μ PD78F8058[Note 1]
Internal memory	Flash Memory	64 KB	96 KB	128 KB
	RAM	8 KB	8 KB	8 KB
System clock	Ceramic/Crystal/External	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz (V_{DD} = 2.7 to 3.6 V), 2 to 5MHz (V_{DD} = 1.8 to 3.6 V)		
	Internal oscillator	1 MHz (TYP.) or 8 MHz (TYP.) or 20 MHz (TYP.)		
Subsystem clock (Oscillation frequency)		XT1 (crystal) oscillation 32.768 KHz (TYP.): V_{DD} = 1.8 V to 5.5 V		
Low Speed internal oscillator (For WDT)		Clock speed : 30 KHz (TYP.)		
Minimum instruction cycle		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		
		61 μs (Subsystem clock: f_{SUB} = 32.768 KHz operation)		
I/O	Total	18[Note 2]		
	CMOS I/O	12[Note 2]		
	CMOS Input	4[Note 2]		
	CMOS Output	1[Note 2]		
	N-ch Open Drain I/O	1[Note 2]		
Interrupt	External	4 channels (INTP0, INTP4[Note 2], INTP5, INTP10)		
	Internal	27 channels		
Timer		- 16 Bit Timer : 12 channels (Unit0: 8 channels, Unit1: 4 channels) - Watch Dog Timer : 1 channel - Real Time Counter: 1 channel		
	Timer outputs	2 (PWM outputs: timer array unit 0: 2[Note 3], timer array unit 1: 0)		
	RTC Output	1 (512 Hz, 16.384 KHz, or 32.768 KHz (subsystem clock: f_{SUB} = 32.768 KHz))		
Serial Interface		- CSI: 1 channel (dedicated to RF transceiver communication at internal connection) - CSI/UART/Simplified I^2C: 1channel - UART (Tx Only) : 1 channel - UART (LIN supported) : 1 channel		
2.4 GHz RF transceiver Function		IEEE802.15.4-2006 specification compatible (Modulation: O-QPSK Spectrum: DSSS Transmission speed:250 kbps)		
Multiplier / Divider		- 16 bits x 16 bits = 32 bits (multiplication) - 32 bits÷32 bits = 32 bits (division)		
DMA controller		2 channels		
Power-on-clear circuit		- Power-on-reset: 1.61±0.09 V - Power-down-reset: 1.59±0.09 V		
Low-voltage detector		1.91 V to 3.45 V (11 steps)		
On-chip debug Function		provided		
Power supply voltage		V_{DD} = 1.8 to 3.6 V		
Operation temperature		Ta = −40 to +85°C		
Package		56-pin QFN (8 x 8) (0.5 mm pitch)		

Notes 1. Under development

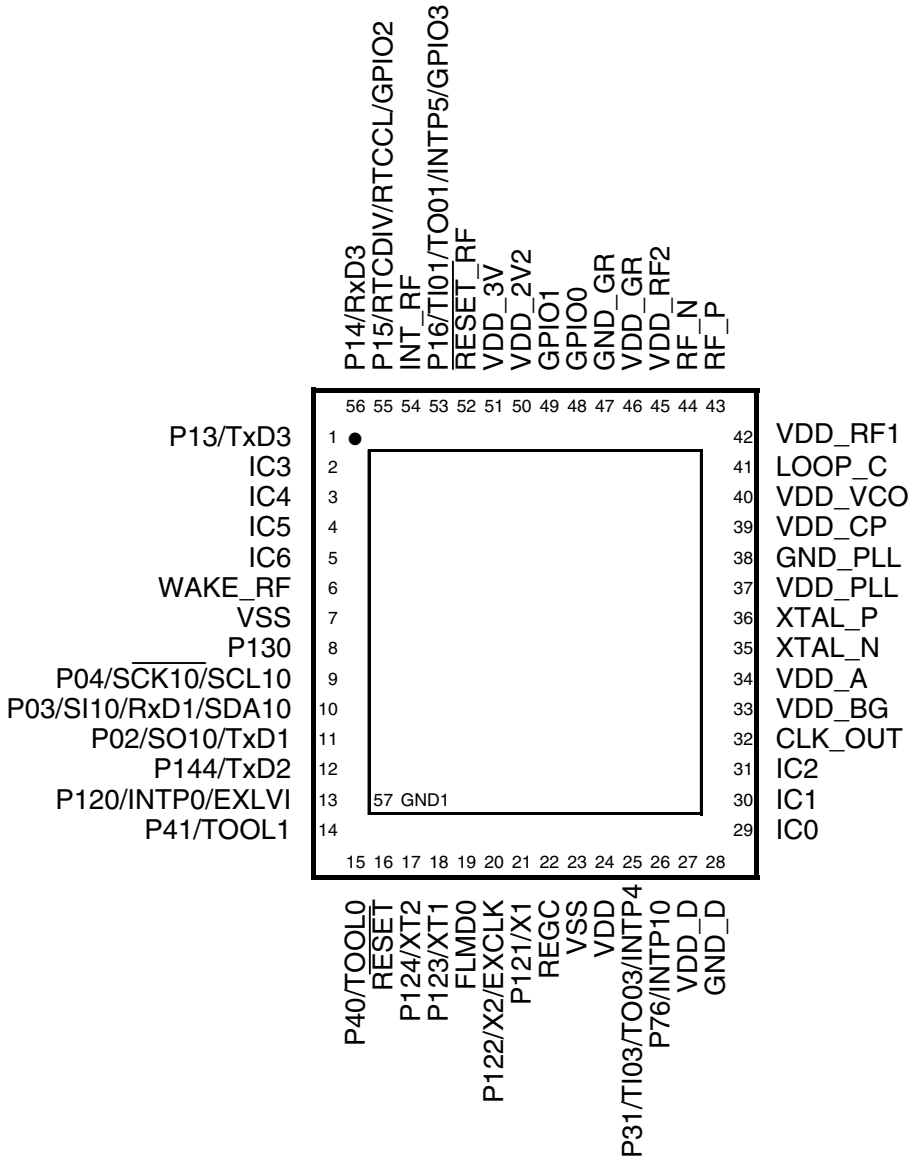
2. Include External Connection externally on the PCB by users between MCU and RF transceiver.

Refer to **6. CONNECTION BETWEEN MCU AND RF TRANSCEIVER**.

3. The number of PWM outputs varies, depending on the setting.

3. PIN CONFIGURATION (TOP VIEW)

- 56-pin plastic QFN (8 x 8) [Note]



Note Under development

Cautions 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: target).

2. Connect the LOOP_C pin to GND_GR via a capacitor (39 pF: target).

3. Connect IC0-IC2 pins to Vss via a resistor.

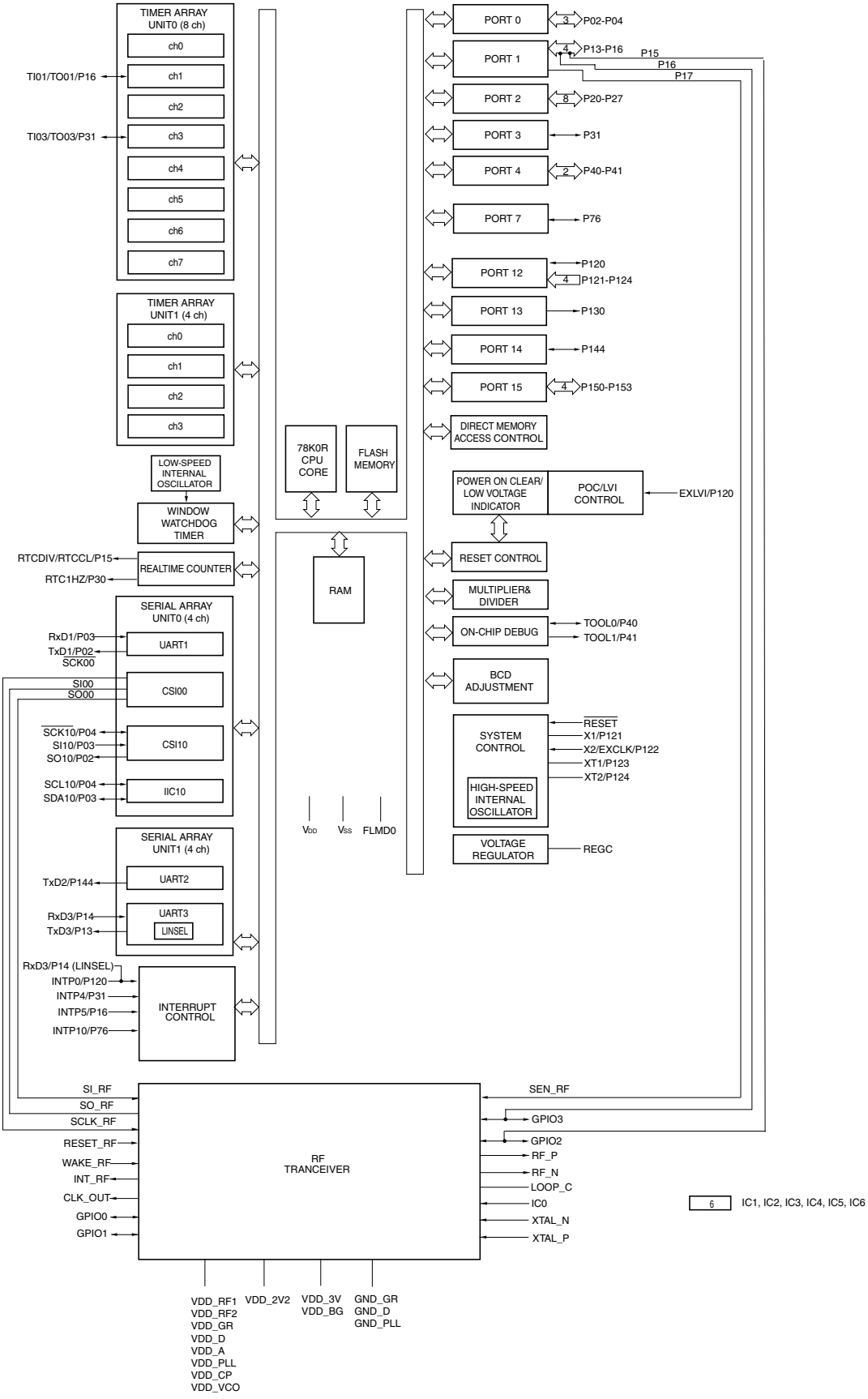
4. Leave open IC3-IC6 pins.

4. PIN IDENTIFICATION

EXCLK : External Clock Input (Main System Clock)
EXLVI : External Potential Input for Low-voltage Detector
FLMD0 : Flash Programming Mode
INTP0,INT4,INTP5 : External Interrupt Input
INT10
P02-P04 : Port 0
P13-P16 : Port 1
P31 : Port 3
P40,P41 : Port 4
P76 : Port 7
P120-P124 : Port 12
P130 : Port 13
P144 : Port 14
CLK_OUT : Clock Output
INT_RF : Interrupt from RF
WAKE_RF : Wakeup for RF
GPIO0,GPIO1 : Port for RF
GPIO2,GPIO3
RESET_RF : Reset for RF
LOOP_C : Loop Capacitor for RF
RF_P : RF Output(+)
RF_N : RF Output(-)
XTAL_N,XTAL_P : Crystal Oscillator(RF Clock)
IC0-IC6 : Internal Circuit
GND1 : Package exposed die pad
REGC : Regulator Capacitance
$\overline{\text{RESET}}$: Reset

RTCCL : Real-time Counter Clock (32 KHz Original Oscillation) Output
RTCDIV : Real-time Counter Clock (32 KHz Divided Frequency) Output
RXD1,RxD3 : Receive Data
$\overline{\text{SCK10}}$: Serial Clock Input/Output
SCL10 : Serial Clock Input/Output
SDA10 : Serial Data Input/Output
SI10, : Serial Data Input
SO10, : Serial Data Output
TI01, TI03 : Timer Input
TO01, TO03 : Timer Output
TOOL0 : Data Input/Output for Tool
TOOL1 : Clock Output for Tool
TxD1-TxD3 : Transmit Data
VDD : Power Supply
VSS : Ground
X1, X2 : Crystal Oscillator (Main System Clock)
XT1, XT2 : Crystal Oscillator (Subsystem Clock)
VDD_RF1 : Power Supply for RF
VDD_RF2
VDD_GR : Power Supply for RF Guard Ring
VDD_3V : Power Supply for RF Regulator
VDD_D : Power Supply for RF Digital
VDD_BG : Power Supply for RF Band Gap
VDD_A : Power Supply for RF Analog
VDD_PLL : Power Supply for RF PLL
VDD_CP : Power Supply for RF Charge pomp
VDD_VCO : Power Supply for RF VCO
GND_GR : Ground for RF Guard Ring
GND_D : Ground for RF digital
GND_PLL : Ground for RF PLL
VDD_2V2 : DC/DC Output

5. BLOCK DIAGRAM



6. CONNECTION BETWEEN MCU AND RF TRANSCEIVER

(1) Internal Connection

Name		Function(RF transceiver)	Direction
RF transceiver	MCU		
SCLK_RF	P10/SCK00	Clock signal of SPI interface	MCU→ RF transceiver
SO_RF	P11/SI00	Output signal of SPI interface	RF transceiver→ MCU
SI_RF	P12/SO00	Input signal of SPI Interface	MCU→ RF transceiver
SEN_RF	P17	Enable signal of SPI interface High level: disable Low level: enable	MCU→ RF transceiver
GPIO2	P15/RTCDIV/ RTCCL	Case of using P15/RTCDIV/ RTCCL, set input mode to GPIO2. Case of using GPIO2, set input mode to P15/RTCDIV/RTCCL.	_
GPIO3	P16/TI01/ TO01/INTP5	Case of using P16/TI01/TO01/INTP5, set input mode to GPIO3. Case of using GPIO3, set input mode to P16/TI01/TO01/INTP5.	_

(2) Connection externally on the PCB by users

Name		Function(RF transceiver)	Direction
RF transceiver	MCU		
RESET_RF	P130	RESET input signal for transceiver High level: disable Low level: enable	MCU→ RF transceiver
WAKE_RF	P144	Wakeup request signal for transceiver The active level can be specified by software setting at RF transceiver.	MCU→ RF transceiver
INT_RF	P31/TI03/ TO03/INTP4	Interrupt output signal The active level can be specified by software setting at RF transceiver.	RF transceiver→ MCU
CLK_OUT	P122/X2/ EXCLK	Clock out at 32/16/8/4/2/1 MHz. Use system clock MCU. XTAL_P and XTAL_N of RF transceiver is main clock at 32 MHz.	RF transceiver→ MCU

Note These are mandatory connection for recommendation library of our company.
The RESET_RF connect to V_{DD} via a resistor of about 10 K ohm.

7. PORT

(1) Port functions

Function Name	I/O	Function	After Reset	Alternate Function
P02	I/O	Port 0. 3-bit I/O port Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P03				SI10/RxD1/SDA10
P04				$\overline{SCK10}$/SCL10
P13	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TxD3
P14				RxD3
P15				RTCDIV/RTCCL/ GPIO2
P16				TI01/TO01/INTP5/ GPIO3
P31	I/O	Port 3. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI03/TO03/INTP4
P40[Note]	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P76	I/O	Port 7. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP10
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P130	Output	Port 13. 1-bit output port.	Output port	–
P144	I/O	Port 14. 1-bit I/O port. Output of P144 can be set to the N-ch open-drain output (VDD tolerance). Input/output can be specified in 1-bit units.Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TxD2
GPIO0	I/O	1-bit I/O port of RF transceiver control.	Input port	–
GPIO1	I/O	1-bit I/O port of RF transceiver control.	Input port	–
GPIO2	I/O	1-bit I/O port of RF transceiver control.	Input port	P15/RTCDIV/ RTCCL
GPIO3	I/O	1-bit I/O port of RF transceiver control.	Input port	P16/TI01/TO01/ INTP5

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally

(2) Non-port functions (1/2)

Function Name	I/O	Function	After Reset	Alternate Function
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01/ GPIO3
INTP10				
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to VSS via a capacitor (0.47 to 1 μF: target).	–	–
RTCDIV	Output	Real-time counter clock (32 KHz divided frequency) output	Input port	P15/RTCCL/ GPIO2
RTCCL	Output	Real-time counter clock (32 KHz original oscillation) output	Input port	P15/RTCDIV/ GPIO2
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD3	Input	Serial data input to UART3	Input port	P14
$\overline{\text{SCK10}}$	I/O	Clock input/output for CSI10.	Input port	P04/SCL10
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{\text{SCK10}}$
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P03/SI10/RxD1
SI10	Input	Serial data input to CSI10.	Input port	P03/RxD1/SDA10
SO10	Output	Serial data output from CSI10.	Input port	P02/TxD1
TI01	Input	External count clock input to 16-bit timer 01	Input port	P16/TO01/INTP5/ GPIO3
TI03		External count clock input to 16-bit timer 03		P31/TO03/INTP4
TO01	Output	16-bit timer 01 output	Input port	P16/TI01/INTP5/ GPIO3
TO03		16-bit timer 03 output		P31/TI03/INTP4
TxD1	Output	Serial data output from UART1	Input port	P02/SO10
TxD2		Serial data output from UART2		P144
TxD3		Serial data output from UART3		P13
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
V_{DD}	–	Positive power supply for MCU	–	–
V_{DD}_3V	–	Positive power supply for regulator and ports of RF transceiver.	–	–
V_{SS}	–	Ground potential	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

(2) Non-port functions (2/2)

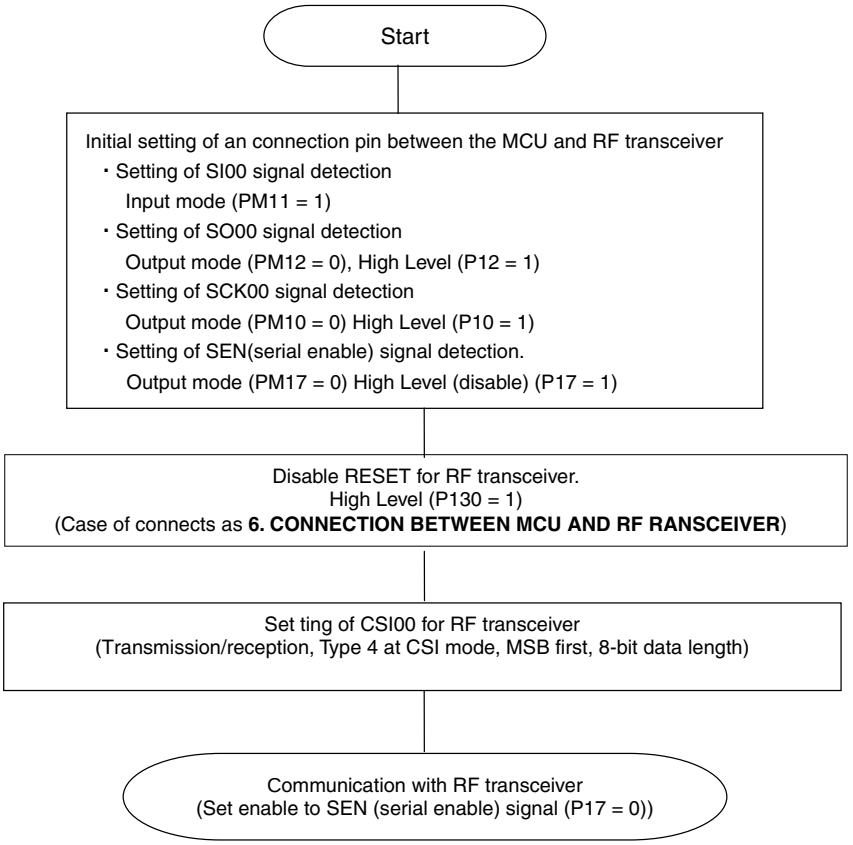
Function Name	I/O	Function	After Reset	Alternate Function
V_{DD}_RF1	–	RF power supply. Bypass with a capacitor as close to the pin as possible.	–	–
V_{DD}_RF2	–	RF power supply. Bypass with a capacitor as close to the pin as possible.	–	–
V_{DD}_GR	–	Guard ring power supply. Bypass with a capacitor as close to the pin as possible.	–	–
V_{DD}_D	–	Digital circuit power supply.	–	–
V_{DD}_BG	–	Power supply for band gap reference circuit. Bypass with capacitor as close to the pin as possible.	–	–
V_{DD}_A	–	Power supply for an analog circuit. Bypass with a capacitor as close to the pin as possible.	–	–
V_{DD}_PLL	–	PLL power supply. Bypass with a capacitor as close to the pin as possible.	–	–
V_{DD}_CP	–	Charge pump power supply. Bypass with a capacitor as close to the pin as possible.	–	–
V_{DD}_VCO	–	VCO supply. Bypass with a capacitor as close to the pin as possible.	–	–
GND_GR	–	Guard ring ground	–	–
GND_D	–	Ground for digital circuit	–	–
GND_PLL	–	Ground for a PLL	–	–
V_{DD}_2V2	–	DC-DC output voltage	–	–
XTAL_N	–	32 MHz Crystal input (-)	–	–
XTAL_P	–	32 MHz Crystal input (+)	–	–
RF_P	Output	Differential RF input/output (+)	Output	–
RF_N	Output	Differential RF input/output (-)	Output	–
CLK_OUT	Output	32/16/8/4/2/1 MHz Clock output	Input	–
INT_RF	Output	Interrupt pin of RF transceiver to the MCU.	Output	–
WAKE_RF	Input	External wake up trigger to RF transceiver.	Input	–
$\overline{\text{RESET\_RF}}$	Input	Global hardware reset pin, active low.	Input	–
LOOP_C	–	PLL loop filter external capacitor. Connected to the external (39 pF: target) capacitor.	–	–
IC0-2	Input	Internal connection.	Input	–
IC3-6	–	Internal connection.	–	–
GND1	–	exposed die pad Make these pins the same potential as V_{SS}.	–	–

(3) Connection of Unused Pins

Pin Name	I/O Circuit Type	Recommended Connection of Unused Pins
P02/SO10/TxD1	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P03/SI10/RxD1/SDA10		
P04/$\overline{SCK10}$/SCL10		
P13/TxD3		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P14/RxD3		
P15/RTCDIV/RTCCL/ GPIO2		
P16/TI01/TO01/INTP5/ GPIO3		
P31/TI03/TO03/INTP4		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. Refer to **6. CONNECTION BETWEEN MCU AND RF RANSCEIVER.**
P40/TOOL0		<When on-chip debugging is enabled> Pull this pin up (pulling it down is prohibited). <When on-chip debugging is disabled> Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P41/TOOL1		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P76/KR6/INTP10	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P120/INTP0/EXLVI		
P121/X1	Input	Independently connect to V_{DD} or V_{SS} via a resistor. Refer to **6. CONNECTION BETWEEN MCU AND RF RANSCEIVER** at P122.
P122/X2/EXCLK		
P123/XT1		
P124/XT2		
P130	Output	Leave Open Refer to **6. CONNECTION BETWEEN MCU AND RF RANSCEIVER**.
P144/TxD2	I/O	Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. Refer to **6. CONNECTION BETWEEN MCU AND RF RANSCEIVER**.
FLMD0	–	Leave open or connect to V_{SS} via a resistor of 100 kΩ or more.
$\overline{RESET}$	Input	Connect directly or via a resistor to V_{DD}.
REGC	–	Connect to V_{SS} via capacitor (0.47 to 1 μF: target).
LOOP_C	–	Connect to GND_GR via capacitor (39 pF: target).
IC0	Input	Connect to V_{SS} via a resistor.
IC1	Input	Connect to V_{SS} via a resistor.
IC2	Input	Connect to V_{SS} via a resistor.
IC3	–	Leave Open
IC4	–	Leave Open
IC5	–	Leave Open
IC6	–	Leave Open
GND1	–	Make this pin the same potential as V_{SS}.

8. CAUTIONS WHILE DEVELOPING PROGRAM

A reference flow chart of the program with RF transceiver



While developing user program, please be sure to set the following setting as initial setting after reset.

Internal Port Name of MCU	Recommended setting
P05, P06, P30, P42 to P44, P46, P47, P50, P51, P53 to P55, P60, P61, P64 to P67, P70 to P75, P77, P110, P140	set this port to output mode after reset

9. CLOCK GENERATOR

The clock generator generates the clock to be supplied to the CPU and peripheral hardware. The following three kinds of system clocks are selectable.

<1> X1 oscillator
This circuit oscillates a clock of fx = 2 to 20 MHz by connecting a resonator to X1 and X2.

<2> Internal high-speed oscillator
This circuit oscillates clocks of f_{IH} = 1, 8 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock.

<3> 20 MHz internal high-speed oscillator
This circuit oscillates clocks of f_{IH20} = 20 MHz (TYP.).

<4> Supply from the EXCLK pin
An external main system clock (f_{EX} = 2 to 20 MHz) can also be supplied from the EXCLK pin.

Select <4> Supply from the EXCLK pin case of connects as **6. CONNECTION BETWEEN MCU AND RF RANSCEIVER**.

The clock generator is basically the same as the one in 78K0R/KF3-L.
Please refer to user manual of 78K0R/KF3-L (U19459E) for the details.

10. PERIPHERALS

The following peripherals are the same as the ones in 78K0R/KF3-L.
Please refer to user manual of 78K0R/KF3-L (U19459E) for the details.

- **WATCHDOG TIMER**
- **MULTIPLIER/DIVIDER**
- **RESET FUNCTION**
- **STANDBY FUNCTION**
- **POWER-ON-CLEAR CIRCUIT**
- **REGULATOR**
- **OPTION BTYE**
- **FLASH MEMORY**
- **ON-CHIP DEBUG FUNCTION**
- **BCD CORRECTION CIRCUIT**

The following peripherals don't exist from the ones in 78K0R/KF3-L.

- **CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER**
- **A/D CONVERTER**
- **SERIAL INTERFACE IICA**
- **KEY INTERRUPT FUNCTION**

The following peripherals are little different from the ones in 78K0R/KF3-L.

- **TIMER ARRAY UNIT**
- **SERIAL ARRAY UNIT**
- **DMA CONTROLLER**
- **INTERRUPT FUNCTIONS**
- **LOW-VOLTAGE DETECTOR**

The difference of each peripheral will be described from next page.

(1) TIMER ARRAY UNIT

The timer array unit has two units. The timer array unit 0 has eight 16-bit timers and the timer array unit 1 has four 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.

Single-operation Function	Combination-operation Function
・Interval timer ・Square wave output ・External event counter ・Input pulse interval measurement ・Measurement of high-/low-level width of input signal	・PWM output ・One-shot pulse output ・Multiple PWM output

The timer array unit is basically the same as the one in 78K0R/KF3-L. But the pin of timer input and output is only the channel 1 and 3 of unit 0.

Please refer to user manual of 78K0R/KF3-L (U19459E) for the details.

(2) SERIAL ARRAY UNIT

The serial array unit has four serial channels per unit and can use two or more of various serial interfaces (3-wire serial (CSI), UART, and simplified I^2C) in combination.

The serial channel is basically the same as the one in 78K0R/KF3-L. Please refer to user manual of 78K0R/KF3-L (U19459E) for the detail explanation of 3-wire serial (CSI) and UART interface.

The following interfaces are supported.

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00 (dedicated to RF transceiver communication)	–	–
	1	–		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	–	UART2(Tx Only)	–
	1	–	–	–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–

Channels 2 and 3 of unit 1 are dedicated to UART3 (supporting LIN-bus).

(3) DMA CONTROLLER

Data can be automatically transferred between SFRs of the peripheral hardware supporting DMA and internal RAM without via CPU by DMA triggers.

DMA triggers are selected by setting IFCn3 to IFCn0, bit 3 to 0 of DMA mode control register (DMCn). The following DMA triggers are selectable.

IFCn3	IFCn2	IFCn1	IFCn0	Selection of DMA start source	
				Trigger signal	Trigger contents
0	0	0	0	–	Disable DMA transfer by interrupt. (Only software trigger is enabled.)
0	0	1	0	INTTM00	End of timer array unit 0 channel 0 count or capture
0	0	1	1	INTTM01	End of timer array unit 0 channel 1 count or capture
0	1	0	0	INTTM04	End of timer array unit 0 channel 4 count or capture
0	1	0	1	INTTM05	End of timer array unit 0 channel 5 count or capture
0	1	1	0	INTCSI00	CSI00 transmission transfer end
1	0	0	0	INTST1/INTCSI10/INTIIC10	UART1 transmission transfer end or CSI10 transmission transfer end or IIC10 transmission transfer end
1	0	0	1	INTSR1	UART1 reception end interrupt
1	0	1	0	INTST3	UART3 transmission transfer end interrupt
1	0	1	1	INTSR3	UART3 reception end interrupt
Other than above				Setting prohibited	

Remark n: DMA channel number (n=0, 1)

Please refer to user manual of 78K0R/KF3-L (U19459E) for the details.

(4) INTERRUPT FUNCTIONS

The following two types of interrupt functions are used.

<1> Maskable interrupts
These interrupts undergo mask control.

<2> Software interrupt
This is a vectored interrupt generated by executing the BRK instruction.

The following maskable interrupts are available.

Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address
	Name	Trigger		
0	INTWDTI	Watchdog timer interval Note 2 (75% of overflow time)	Internal	0004H
1	INTLVI	Low-voltage detection Note 3		0006H
2	INTP0	Pin input edge detection	External	0008H
3	INTP4			0010H
4	INTP5			0012H
5	INTST3	UART3 transmission transfer end or buffer empty interrupt	Internal	0014H
6	INTSR3	UART3 reception transfer end		0016H
7	INTSRE3	UART3 reception communication error occurrence		0018H
8	INTDMA0	End of DMA0 transfer		001AH
9	INTDMA1	End of DMA1 transfer		001CH
10	INTCSI00	CSI00 transfer end or buffer empty interrupt		001EH
11	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/ CSI10 transfer end or buffer empty interrupt/ IIC10 transfer end		0024H
12	INTSR1	UART1 reception transfer end		0026H
13	INTSRE1	UART1 reception communication error occurrence		0028H
14	INTTM00	End of timer array unit 0 channel 0 count		002CH
15	INTTM01	End of timer array unit 0 channel 1 count or capture		002EH

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority.
2. When bit 7 (WDTINT) of the option byte (00C0H) is set to 1.
3. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
	Name	Trigger		
16	INTTM02	End of timer array unit 0 channel 2 count	Internal	0030H
17	INTTM03	End of timer array unit 0 channel 3 count or capture		0032H
18	INTRTC	Fixed-cycle signal of real-time counter/alarm match detection		0036H
19	INTRTCI	Interval signal detection of real-time counter		0038H
20	INTST2	UART2 transmission transfer end or buffer empty interrupt		003CH
21	INTTM13	End of timer array unit 1 channel 3 count		0040H
22	INTTM04	End of timer array unit 0 channel 4 count		0042H
23	INTTM05	End of timer array unit 0 channel 5 count		0044H
24	INTTM06	End of timer array unit 0 channel 6 count		0046H
25	INTTM07	End of timer array unit 0 channel 7 count or capture		0048H
26	INTP10	Pin input edge detection	External	0052H
27	INTTM10	End of timer array unit 1 channel 0 count	Internal	0056H
38	INTTM11	End of timer array unit 1 channel 1 count		0058H
29	INTTM12	End of timer array unit 1 channel 2 count		005AH
30	INTMD	End of division operation		005EH

Note. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority.

Please refer to user manual of 78K0R/KF3-L (U19459E) for the details.

(5) LOW-VOLTAGE DECTECTOR

The low-voltage detector (LVI) is basically the same as the one in 78K0R/KF3-L. But the low-voltage detection levels are different.

The low-voltage detection levels are set by LVIS3 to LVIS0, bit 3 to 0 of low-voltage detection level select register (LVIS). The low-voltage detection levels are as below.

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	1	0	1	V_{LVI5} (3.45 ± 0.1V)Note
0	1	1	0	V_{LVI6} (3.30 ± 0.1V)Note
0	1	1	1	V_{LVI7} (3.15 ± 0.1V)Note
1	0	0	0	V_{LVI8} (2.99 ± 0.1V)Note
1	0	0	1	V_{LVI9} (2.84 ± 0.1V)Note
1	0	1	0	V_{LVI10} (2.68 ± 0.1V)Note
1	0	1	1	V_{LVI11} (2.53 ± 0.1V)Note
1	1	0	0	V_{LVI12} (2.38 ± 0.1V)Note
1	1	0	1	V_{LVI13} (2.22 ± 0.1V)Note
1	1	1	0	V_{LVI14} (2.07 ± 0.1V)Note
1	1	1	1	V_{LVI15} (1.91 ± 0.1V)Note
Other than above				Setting prohibited

Note These are preliminary values and subject to change.

Please refer to user manual of 78K0R/KF3-L (U19459E) for the details.

11. RF transceiver FUNCTION

The RF transceiver function is implemented by 2.4GHz RF transceiver inside.

It integrates a wireless RF transceiver operating at 2.4 GHz with an IEEE802.15.4-2006 compliant baseband and MAC layer function blocks.

The RF block of the RF transceiver integrates a receiver, a transmitter, a voltage-controlled oscillator (VCO), and a phase-locked loop (PLL). It uses advanced radio architecture to minimize the external component count and the power consumption.

The MAC/Baseband provides the hardware architecture for both an 802.15.4 MAC and PHY layers. It mainly consists of TX/RX FIFOs, a CSMA-CA controller, a 'Superframe' constructor, a receiving frame filter, a security engine, and a digital signal processing module.

NOTE FOR USING RF TRANSCEIVER

International regulations and national laws regulate the use of radio receivers and transmitters.
Please note the compliance with regulation for using country.

The following most important regulations for the 2.4 GHz
Japan : ARIB STD-T66
USA : FCC CFR47 part15.247 and part15.249
Europe : EN300 440 and EN 300 328

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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