LSM320HAY30

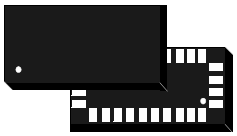
MEMS motion sensor module:
3D digital accelerometer and 2D pitch and yaw analog gyroscope

Features

- 2.7 V to 3.6 V power supply operation
- Low voltage compatible digital IOs, 1.8 V
- ±2 *g*/±4 *g*/±8 *g* dynamically selectable full-scale
- ±300 dps absolute analog angular rate output
- I^2C/SPI digital linear acceleration interface (16 bit data output)
- Two separated outputs for pitch and yaw axis (1x and 4x amplified)
- Integrated low-pass filters for angular rate
- 2 independent programmable interrupt generators for free-fall and motion detection
- Sleep-to-wakeup function
- 6D orientation detection
- Extended operating temperature range (40 °C to +85 °C)
- High stability over temperature
- High shock survivability
- Embedded self-test
- Embedded power-down
- Embedded low-power mode
- ECOPACK® RoHS and “Green” compliant (see *Section 9*)

Applications

- Motion control for smart user interface
- Display orientation
- Gaming and virtual reality input devices
- Industrial and robotics
- Vibration monitoring and compensation
- Impact recognition and logging
- Motion-activated functions
- Intelligent power-saving for handheld devices
- Free-fall detection



LGA-28L (4.4x7.5x1.1mm)

Description

The LSM320HAY30 is a low-power system-in-package featuring a 3D digital linear acceleration sensor and a 2D analog angular rate pitch and yaw sensor. It provides excellent temperature stability and high resolution over an extended operating temperature range (-40°C to +85°C). ST’s family of sensor modules leverages the robust and mature manufacturing process already used for the production of micromachined accelerometers. The LSM320HAY30 has a dynamically user-selectable full-scale acceleration range of ±2 *g*/±4 *g*/±8 *g*, and an angular rate of ±300 dps capable of detecting rates with a -3 dB bandwidth up to 140 Hz along pitch and yaw axes. The LSM320HAY30 is capable of measuring linear accelerations with output data rates from 0.5 Hz up to 1 kHz. The embedded self-test capability allows the user to check the functioning of each sensor in the final application. The device can be configured to generate an interrupt signal by inertial wakeup/free-fall events as well as by the position of the device itself. Several years ago ST successfully pioneered the use of this package for accelerometers. Today, ST has the widest manufacturing capability and strongest expertise in the world for production of sensors in plastic LGA packages.

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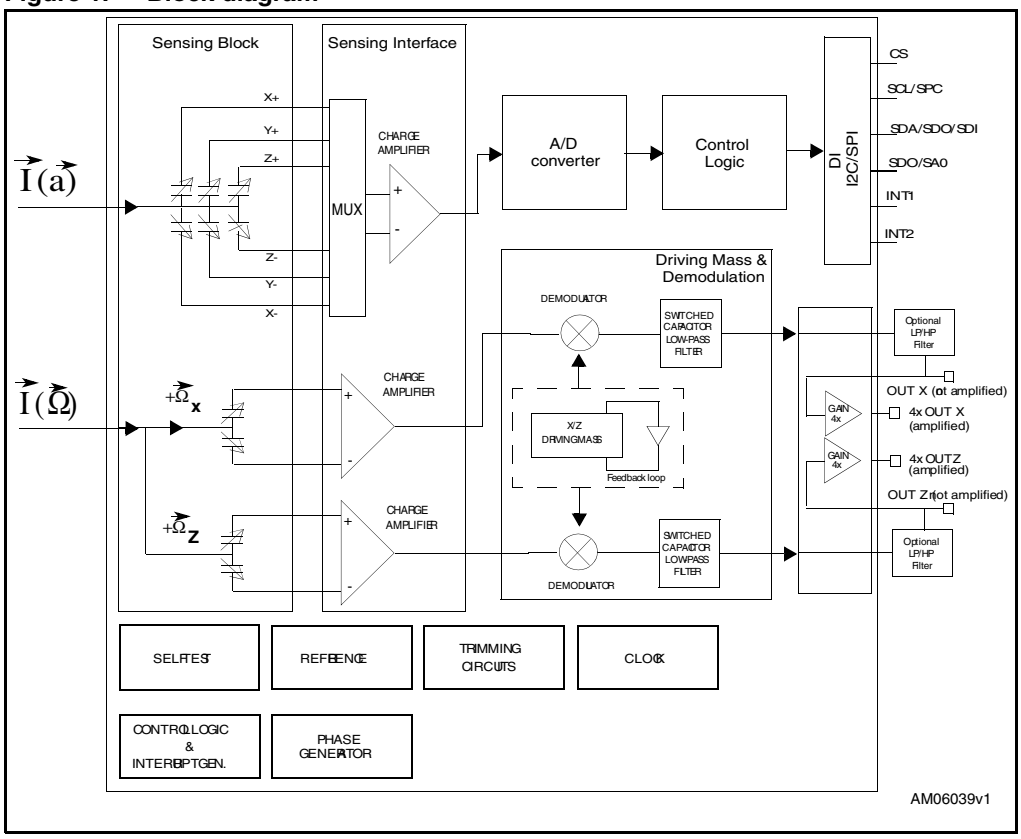
1 Block diagram and pin description

Figure 1. Block diagram



1.1 Pin connection and description

Figure 2. Pin connection

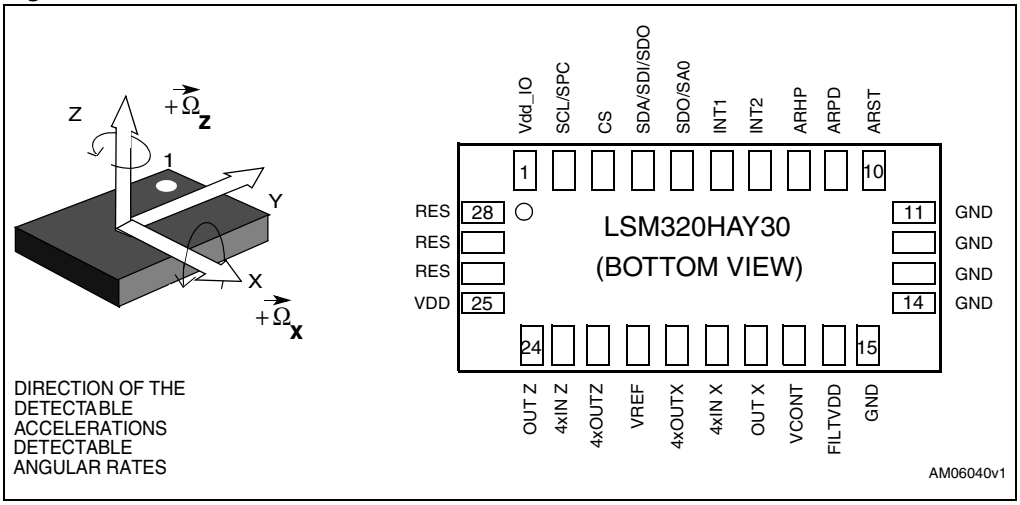


Table 1. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL/SPC	I^2C serial clock (SCL)/SPI serial port clock (SPC)
3	CS	SPI enable/I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
4	SDA/SDI/SDO	I^2C serial data (SDA)/SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	SDO/SA0	SPI serial data output (SDO)/ I^2C less significant bit of the device address (SA0)
6	INT1	Inertial interrupt 1
7	INT2	Inertial interrupt 2
8	ARHP	Angular rate high-pass filter reset (logic 0: normal operation mode; logic1: external high-pass filter is reset)
9	ARPD	Angular rate power-down (see *Table 5*)
10	ARST	Angular rate self-test (see *Table 5*)
11	GND	0 V supply
12	GND	0 V supply
13	RES	0 V supply
14	GND	0 V supply
15	GND	0 V supply
16	FILTVDD	PLL filter connection pin 16
17	VCONT	PLL filter connection pin 15
18	OUT X	Not amplified Out X

Table 1. Pin description (continued)

Pin#	Name	Function
19	4xIN X	Input of 4x amplifier
20	4xOUT X	X rate signal output voltage (amplified)
21	Vref	Reference voltage
22	4x OUTZ	Z rate signal output voltage (amplified)
23	4xIN Z	Input of 4x amplifier
24	OUT Z	Not amplified Out Z
25	VDD	Power supply
26	RES	Connected to Vdd
27	RES	Connected to Vdd
28	RES	Connected to Vdd

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd=3,0 V, T=25 °C unless otherwise noted.[a]

Table 2. Mechanical characteristics

Symbol[1]	Parameter	Test conditions	Min.	Typ.[2]	Max.	Unit
LA_FS	Linear acceleration measurement range[3]	FS bit set to 00		±2.0		g
		FS bit set to 01		±4.0		
		FS bit set to 11		±8.0		
AR_FS	Angular rate measurement range	4x OUT (amplified)		±300		dps
		OUT (not amplified)		±1200		
LA_So	Linear acceleration sensitivity	FS bit set to 00 (12 bit)	0.9	1	1.1	mg/digit
		FS bit set to 01 (12 bit)	1.8	2	2.2	
		FS bit set to 11 (12 bit)	3.5	3.9	4.3	
AR_So	Angular rate sensitivity[4]	4x OUT (amplified)		3.33		mV/dps
		OUT (not amplified)		0.83		mV/dps
LA_TCSo	Linear acceleration sensitivity change vs. temperature	FS bit set to 00		±0.01		%/°C
AR_TCSo	Angular rate sensitivity change vs temperature	Delta from 25°C		0.07		%/°C
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy[5],[6]	FS bit set to 00		±20		mg
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature	Max delta from 25°C		±0.1		mg/°C
AR_ZrI	Zero-rate level[6]			1.5		V
AR_Vref	Reference voltage			1.5		V
AR_TCZrl	Angular rate zero-rate level change vs. temperature	Max delta from 25°C		±0.05		dps/°C
LA_An	Linear acceleration noise density	FS bit set to 00		218		µg/√Hz
AR_Rn	Angular rate noise density			0.02		dps/√Hz
AR_NL	Angular rate non linearity	Best fit straight line		±1		% FS
LA_BW	Linear acceleration bandwidth[7]			ODR/2		Hz
AR_BW	Angular rate bandwidth[8]			140		Hz
LA_ST	Linear acceleration self-test output change[9],[10],[11]	FS bit set to 00 X axis		+500		LSb
		FS bit set to 00 Y axis		-500		LSb
		FS bit set to 00 Z axis		+600		LSb

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.7 V to 3.6 V.

Table 2. Mechanical characteristics (continued)

Symbol[1]	Parameter	Test conditions	Min.	Typ.[2]	Max.	Unit
AR_ST	Angular rate self-test output change			250		mV
Top	Operating temperature range		-40		+85	°C

1. Linear acceleration (LA), Angular Rate (AR) parameter labeling
2. Typical specifications are not guaranteed
3. Verified by wafer level test and measurement of initial offset and sensitivity
4. Sensitivity and zero-rate offset are not ratiometric to supply voltage
5. Typical zero-*g* level offset value after MSL3 preconditioning
6. Offset can be eliminated by enabling the built-in high-pass filter
7. Refer to *Table 23* for filter cut-off frequency.
8. The product is capable of measuring angular rates extending from DC to the selected BW.
9. The sign of “Self-test output change” is defined by LA_CTRL_REG4 STsign bit (*Table 27*), for all axes.
10. Linear acceleration sensing Self-Test output changes with the power supply. “Self-test output change” is defined as $OUTPUT[LSb]_{(LA\_CTRL\_REG4\ ST\ bit=1)}$ - $OUTPUT[LSb]_{(LA\_CTRL\_REG4\ ST\ bit=0)}$. 1LSb=4g/4096 at 12bit representation, ±2 g Full-scale
11. Output data reach 99% of final value after 1/ODR+1ms when enabling linear acceleration sensing self-test mode, due to device filtering.

2.2 Electrical characteristics

@ Vdd=3,0 V, T=25 °C unless otherwise noted.[b]

Table 3. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		2.7	3.0	3.6	V
Vdd_IO	I/O pins supply voltage[2]		1.71		Vdd+0.1	V
LA_Idd	Linear acceleration current consumption in normal mode	ODR = 50 Hz		0.25		mA
AR_Idd	Angular rate current consumption in normal mode	ARPD pin connected to GND		6.8		mA
LA_IddLP	Linear acceleration current consumption in low-power mode	ODR_{LP} = 0.5 Hz		10		µA
AR_IddSl	Angular rate current consumption in sleep mode	ARPD, ARST pin connected to Vdd		2.1	5	mA
LA_IddPdn	Linear acceleration current consumption in power-down mode			1		µA
AR_IddPdn	Angular rate current consumption in power-down mode	ARPD pin connected to Vdd		1	5	µA

b. The product is factory calibrated at 3 V.

Table 3. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
AR_VST	Angular rate self-test input	Logic 0 level	0		0.2*Vdd	V
		Logic 1 level	0.8*Vdd		Vdd	
AR_VPD	Angular rate power-down input	Logic 0 level	0		0.2*Vdd	V
		Logic 1 level	0.8*Vdd		Vdd	
LA_VIH	Linear acceleration digital high level input voltage		0.8*Vdd_IO			V
LA_VIL	Linear acceleration digital low level input voltage				0.2*Vdd_IO	V
LA_VOH	Linear acceleration high level output voltage		0.9*Vdd_IO			V
LA_VOL	Linear acceleration low level output voltage				0.1*Vdd_IO	V
LA_ODR	Linear acceleration output data rate in normal mode	DR bit set to 00		50		Hz
		DR bit set to 01		100		
		DR bit set to 10		400		
		DR bit set to 11		1000		
LA_ODR_{LP}	Linear acceleration output data rate in low-power mode	PM bit set to 010		0.5		Hz
		PM bit set to 011		1		
		PM bit set to 100		2		
		PM bit set to 101		5		
		PM bit set to 110		10		
LA_Ton	Linear acceleration turn-on time(3)	ODR = 100 Hz		1/ODR+1 ms		s
AR_Ton	Angular rate turn-on time(4)			200		ms
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed
2. It is possible to remove Vdd, maintaining Vdd_IO without blocking the communication buses. In this condition the measurement chain is powered off.
3. Time to obtain valid data after exiting power-down mode
4. Time to obtain valid data after exiting power-down mode

3 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (PD, ST)	-0.3 to Vdd +0.3	V
A	Acceleration	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
Vdd_IO	I/O pin supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3 V)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

4 Functionality and terminology

The LSM320HAY30 is an inertial module capable of detecting 3-axis linear acceleration and 2-axis angular rate. The system is housed in an LGA package.

The device includes an ASIC with a digital IC interface capable of providing linear acceleration information through an I^2C/SPI serial interface and analog output related to angular rate.

The LSM320HAY30 may also be configured to generate an inertial *wakeup* and *free-fall* interrupt signal according to a programmed acceleration event along the enabled axes. Both free-fall and wakeup can be used simultaneously on two different pins (INT1/INT2).

4.1 Factory calibration

The system is factory calibrated for sensitivity and zero level. The trimming values are stored inside the device in non-volatile memory. When the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows the use of the device without further calibration.

4.2 Sensitivity

Linear acceleration sensing

Liner Acceleration Sensitivity (LA_So) describes the gain of the sensor and can be determined e.g. by applying 1 *g* acceleration to it. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, a ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

Angular rate sensing

Angular rate detection produces a positive-going output voltage for counter-clockwise rotation around the sensitive axis considered. Angular Rate Sensitivity (AR_So) describes the gain of the sensor and can be determined by applying a defined angular rate to it. This value changes very little over temperature and over time.

4.3 Zero level

Zero-*g* level

Zero-*g* level Offset (LA_TyOff) describes the deviation of an actual output signal from the ideal output signal if no linear acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X and Y axes, whereas the Z axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content

of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

Zero-*g* level offset changes little over temperature, see "Zero-*g* level change vs. temperature" (LA_TCOff) in *Table 2*. The Zero-*g* level tolerance (LA_TyOff) describes the standard deviation of the range of Zero-*g* levels of a group of sensors.

Zero-rate level

Angular rate zero-rate level (AR_Zrl) describes the actual angular rate output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

4.4 Self-test

Linear acceleration self-test

Self-test allows the checking of sensor functionality without moving it. The self-test function is off when the self-test bit (ST) of LA_CTRL_REG4 (control register 4) is programmed to '0'. When the self-test bit of LA_CTRL_REG4 is programmed to '1' an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs will exhibit a change in their DC levels which are related to the selected full-scale through the device sensitivity. When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 2*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

Angular rate self-test

Self-test allows testing of the mechanical and electric parts of the sensor, permitting the seismic mass to be moved by means of an electrostatic test-force. The self-test function is off when the ARST pin is connected to GND. When the ARST pin is tied to Vdd and ARPD is tied to GND (see *Table 5*), an actuation force is applied to the sensor, emulating a definite Coriolis force. In this case the sensor output exhibits a voltage change in its DC level which is also dependent on the supply voltage. When ST is active, the device output level is given by the algebraic sum of the signals produced by the velocity acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 2*, then the mechanical element is working properly and the parameters of the interface chip are within the defined specifications.

4.5 Advanced features

4.5.1 Linear acceleration sensing

The LSM320HAY30 linear acceleration sensor includes a low-power mode characterized by lower data rate refreshing. In this way the device, even when sleeping, continues sensing acceleration and generating interrupt requests.

The “sleep-to-wakeup” function, in conjunction with low-power mode, allows further reduction of system power consumption and the development of new smart applications.

When the sleep-to-wakeup function is activated,the LSM320HAY30 is able to automatically wake up the linear acceleration sensor as soon as an interrupt event has been detected.

With this feature the system is efficiently switched from low-power mode to normal mode based on user-selectable positioning and acceleration events, thus ensuring power-saving and flexibility.

4.5.2 Angular rate sensing

Sleep mode, self-test and power-down

The LSM320HAY30 has advanced power-saving features for angular rate sensing thanks to the availability of three different operating modes. When the device is set to sleep mode configuration, the reading chain is completely turned off, resuting in low power consumption. In this condition, the device turn-on time is significantly reduced, allowing simple external power cycling.

Based on the table below, the user can select the desired operating mode using two dedicated pins (ARST and ARPD).

Table 5. Angular rate sleep mode and power-down mode configuration

Operating mode	ARST pin	ARPD pin
Normal mode	0	0
Power-down	0	1
Self-test	1	0
Sleep mode	1	1

High-pass filter reset (ARHP)

The LSM320HAY30 provides the possibility to reset the optional external high-pass filter by applying a high logic value to the ARHP pad. This procedure ensures faster response, especially during overload conditions. Moreover, this operation is recommended each time the device is powered.

5 Application hints

Figure 3. LSM320HAY30 electrical connections

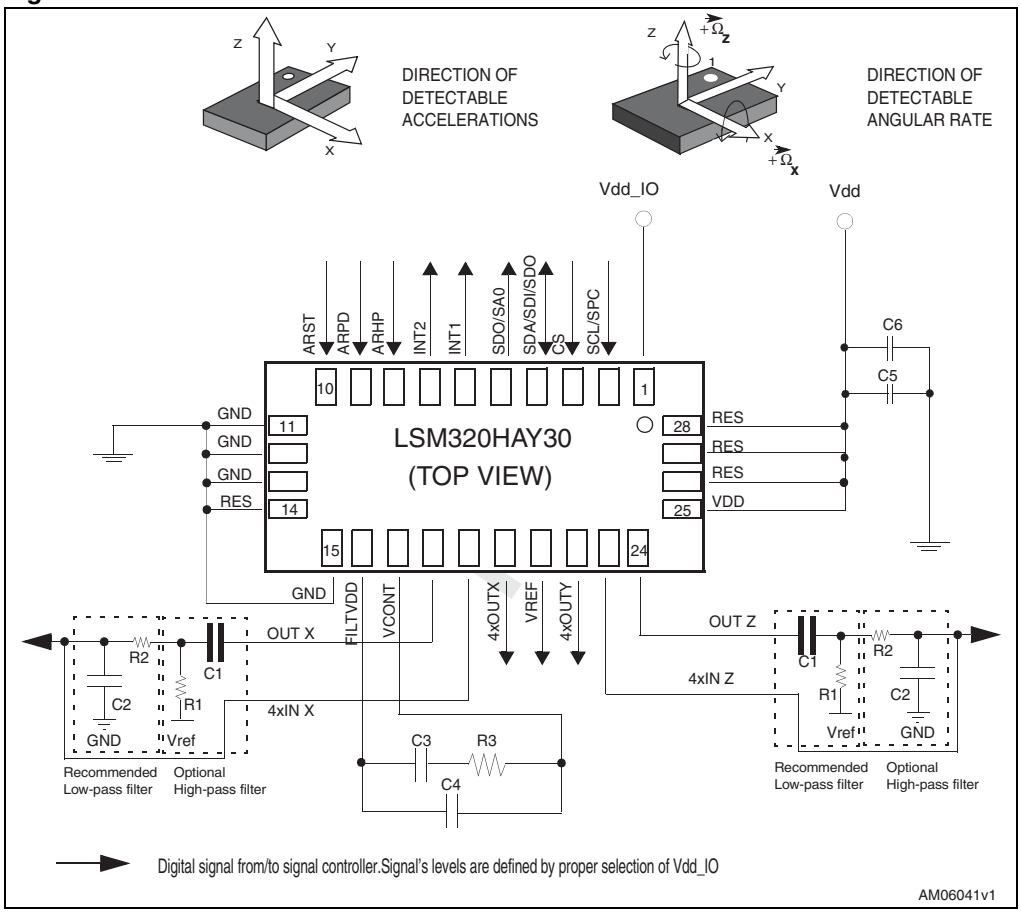


Table 6. External component values

Component type	Component	Value
Capacitor	C1	4.7 µF
	C2	2.2 nF to 2.2 µF
	C3	470 nF
	C4	10 nF
	C5	100 nF
	C6	10 µF
Resistor	R1	1 MΩ
	R2	33 kΩ
	R3	10 kΩ

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1=100 nF ceramic, C2=10 µF aluminum) should be placed as near as possible to the supply pin of the device (common design practice).

All voltage and ground supplies must be present at the same time to obtain proper behavior of the IC (refer to *Figure 3*).

5.1 Linear acceleration sensing

The functionality of the device and the measured acceleration data is selectable and accessible through the SPI/I^2C interface.

The functions, the threshold and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user though the SPI/I^2C interface.

5.2 Angular rate sensing

The LSM320HAY30 allows band limitation of the output rate response through the use of an external low-pass filter (recommended) and/or high-pass filter (optional) in addition to the embedded low-pass filter (f_t = 140 Hz).

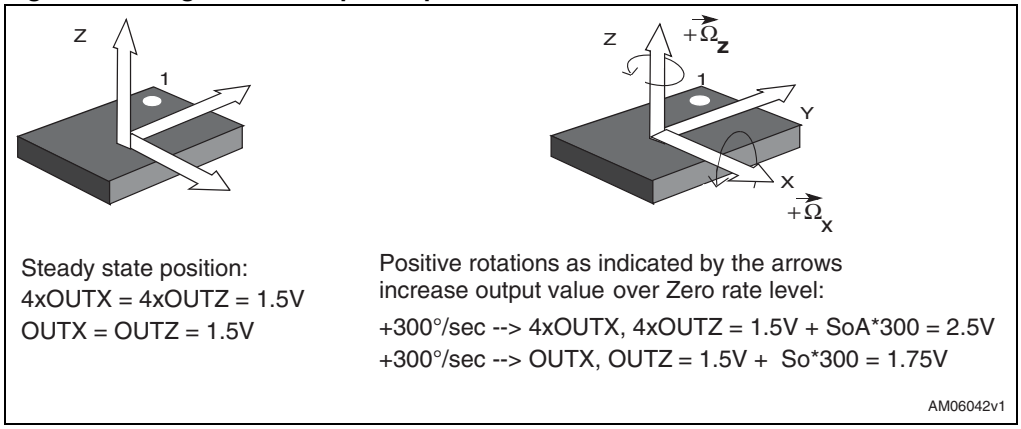
4xOUTX and 4xOUTZ are, respectively, OUTX and OUTZ amplified outputs lines, internally buffered to ensure low output impedance.

If external filtering is not applied, it is mandatory to short-circuit pad 18 to pad 19 and pad 23 to pad 24, respectively, when amplified outputs are used.

When only a non-amplified output is used (OUTX/OUTZ), it is recommended to set pin 19 and 23 to a fixed reference voltage (Vref).

The LSM320HAY30 IC includes a PLL (phase locked loop) circuit to synchronize driving and sensing interfaces. Capacitors and resistors must be added at the **FILTVDD** and **VCONT** pins (as shown in *Figure 3*) to implement a second-order low-pass filter.

Figure 4. Angular rate output response vs. rotation



5.3 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

6 Digital interfaces

The registers embedded in the LSM320HAY30 may be accessed through both the I^2C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 7. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I^2C less significant bit of the device address (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LSM320HAY30 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 8. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd_IO through a pull-up resistor embedded inside the LSM320HAY30. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the 8th bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave ADdress (SAD) associated with the LSM320HAY30 is 001100xb. The **SDO**/**SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b), otherwise if the SA0 pad is connected to ground, the LSb value is '0' (address 0011000b). This solution permits connecting and addressing two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LSM320HAY30 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto-increment. If the MSb of the SUB field is '1', the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit was '1' (read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with direction unchanged. *Table 9* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 9. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Table 10. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 11. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 12. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 13. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing a real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

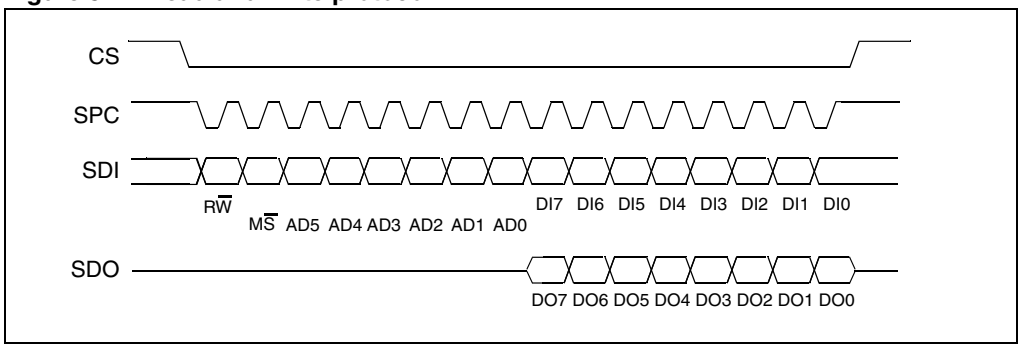
In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

6.2 SPI bus interface

The LSM320HAY30 SPI is a bus slave. The SPI allows writing and reading of the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 5. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

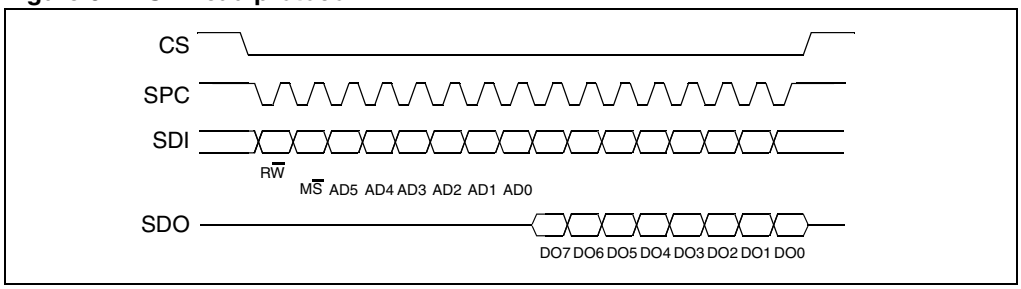
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is '0' the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is '1' the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 6. SPI read protocol



The SPI Read command is performed with 16 clock pulses. A multiple byte read command is performed adding blocks of 8 clock pulses after the previous one.

bit 0: READ bit. The value is 1.

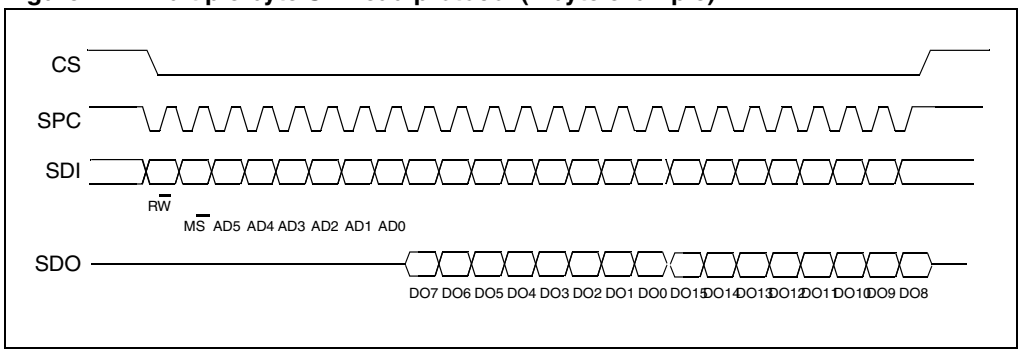
bit 1: MS bit. When 0, do not increment the address. When 1, increment the address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

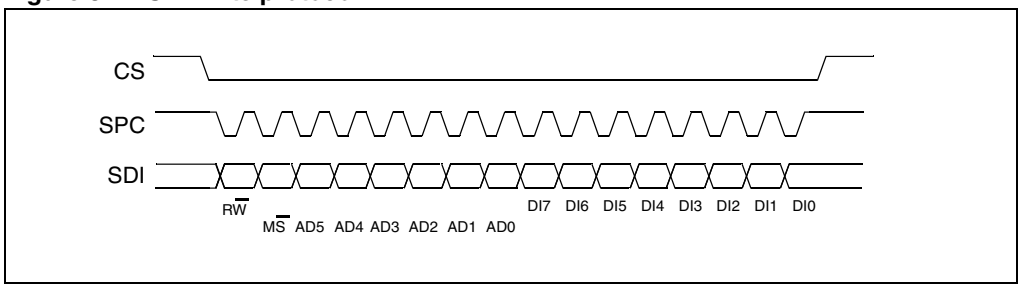
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 7. Multiple byte SPI read protocol (2 byte example)



6.2.2 SPI write

Figure 8. SPI write protocol



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed adding blocks of 8 clock pulses after the previous one.

bit 0: WRITE bit. The value is 0.

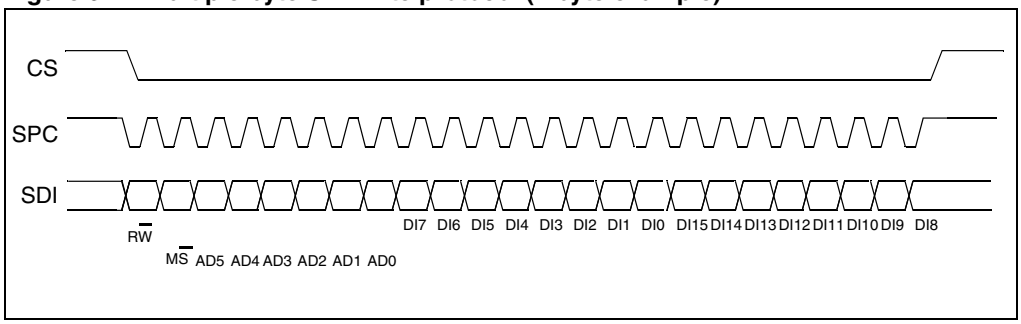
bit 1: MS bit. When 0, do not increment the address. When 1, increment the address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

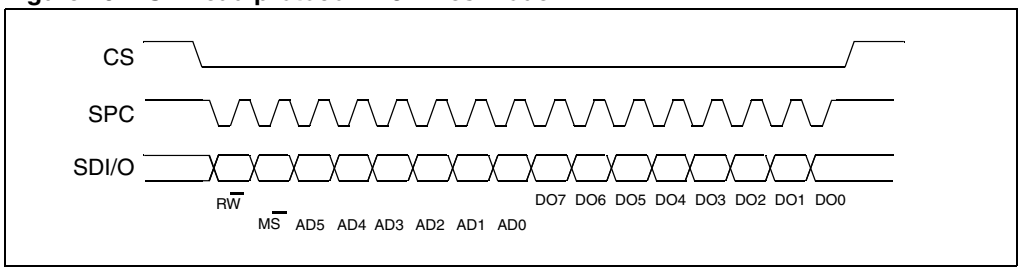
Figure 9. Multiple byte SPI write protocol (2 byte example)



6.2.3 SPI read in 3-wires mode

3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in LA_CTRL_REG4.

Figure 10. SPI read protocol in 3-wires mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, do not increment the address. When 1, increment the address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

7 Register mapping

The table given below provides a listing of the 8-bit registers embedded in the device and the related addresses:

Table 14. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00 - 0E			Reserved
WHO_AM_I	r	0F	000 1111	00110010	Dummy register
Reserved (do not modify)		10 - 1F			Reserved
LA_CTRL_REG1	rw	20	010 0000	00000111	
LA_CTRL_REG2	rw	21	010 0001	00000000	
LA_CTRL_REG3	rw	22	010 0010	00000000	
LA_CTRL_REG4	rw	23	010 0011	00000000	
LA_CTRL_REG5	rw	24	010 0100	00000000	
LA_HP_FILTER_RESET	r	25	010 0101		Dummy register
LA_REFERENCE	rw	26	010 0110	00000000	
LA_STATUS_REG	r	27	010 0111	00000000	
LA_OUT_X_L	r	28	010 1000	output	
LA_OUT_X_H	r	29	010 1001	output	
LA_OUT_Y_L	r	2A	010 1010	output	
LA_OUT_Y_H	r	2B	010 1011	output	
LA_OUT_Z_L	r	2C	010 1100	output	
LA_OUT_Z_H	r	2D	010 1101	output	
Reserved (do not modify)		2E - 2F			Reserved
LA_INT1_CFG	rw	30	011 0000	00000000	
LA_INT1_SOURCE	r	31	011 0001	00000000	
LA_INT1_THS	rw	32	011 0010	00000000	
LA_INT1_DURATION	rw	33	011 0011	00000000	
LA_INT2_CFG	rw	34	011 0100	00000000	
LA_INT2_SOURCE	r	35	011 0101	00000000	
LA_INT2_THS	rw	36	011 0110	00000000	
LA_INT2_DURATION	rw	37	011 0111	00000000	
Reserved (do not modify)		38 - 3F			Reserved

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibrated values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control acceleration portion behavior and to retrieve acceleration data. The register address, composed of 7 bits, is used to identify them and to write the data through the serial interface.

8.1 WHO_AM_I (0Fh)

Table 15. WHO_AM_I register

0	0	1	1	0	0	1	0

This register is the device identification register, and contains the device identifier which, for the LSM320HAY30, is set to 32h.

8.2 LA_CTRL_REG1 (20h)

Table 16. LA_CTRL_REG1 register

PM2	PM1	PM0	DR1	DR0	Zen	Yen	Xen

Table 17. LA_CTRL_REG1 description

PM2 - PM0	Power mode selection. Default value: 000 (000: Power-down; Others: refer to *Table 18*)
DR1, DR0	Data rate selection. Default value: 00 (00:50 Hz; others: refer to *Table 19*)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

PM bits allow selection between power-down and two operating active modes. The device is in power-down mode when the PD bits are set to “000” (default value after boot). *Table 18* shows all the possible power mode configurations and respective output data rates. Output data in the low-power modes are computed with a low-pass filter cut-off frequency defined by DR1, DR0 bits.

DR bits, in normal mode operation, select the data rate at which acceleration samples are produced. In low-power mode they define the output data resolution. *Table 19* shows all the possible configurations for the DR1 and DR0 bits.

Table 18. Power mode and low-power output data rate configurations

PM2	PM1	PM0	Power mode selection	Output data rate [Hz] ODR_{LP}
0	0	0	Power-down	--
0	0	1	Normal mode	ODR
0	1	0	Low power	0.5
0	1	1	Low power	1
1	0	0	Low power	2
1	0	1	Low power	5
1	1	0	Low power	10

Table 19. Normal mode output data rate configurations and low-pass cut-off frequencies

DR1	DR0	Output data rate [Hz] ODR	Low-pass filter cut-off frequency [Hz]
0	0	50	37
0	1	100	74
1	0	400	292
1	1	1000	780

8.3 LA_CTRL_REG2 (21h)

Table 20. LA_CTRL_REG2 register

BOOT	HPM1	HPM0	FDS	HPen2	HPen1	HPCF1	HPCF0

Table 21. LA_CTRL_REG2 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
HPM1, HPM0	High-pass filter mode selection. Default value: 00 (00: normal mode. Others: refer to *Table 22*)
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register)
HPen2	High-pass filter enabled for Interrupt 2 source. Default value: 0 (0: filter bypassed; 1: filter enabled)

Table 21. LA_CTRL_REG2 description (continued)

HPen1	High-pass filter enabled for Interrupt 1 source. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPCF1, HPCF0	High-pass filter cut-off frequency configuration. Default value: 00 (00: HPc=8; 01: HPc=16; 10: HPc=32; 11: HPc=64)

The **BOOT** bit is used to refresh the content of the internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the internal registers related to trimming functions to permit good device behavior. If, for any reason, the content of the trimming registers was changed, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to '1', the content of internal Flash is copied to the corresponding internal registers and is used to calibrate the device. These values are factory-trimmed and are different for every accelerometer. They permit good device behavior and normally do not have to be modified. At the end of the boot process, the BOOT bit is again set to '0'.

Table 22. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode (reset reading HP_RESET_FILTER)

HPCF[1:0]. These bits are used to configure the high-pass filter cut-off frequency f_t which is given by:

$$f_t = \ln\left(1 - \frac{1}{HPc}\right) \cdot \frac{f_s}{2\pi}$$

The equation can be simplified to the following approximated equation:

$$f_t = \frac{f_s}{6 \cdot HPc}$$

Table 23. High-pass filter cut-off frequency configuration

HPcoeff2,1	f_t [Hz] Data rate = 50 Hz	f_t [Hz] Data rate = 100 Hz	f_t [Hz] Data rate = 400 Hz	f_t [Hz] Data rate = 1000 Hz
00	1	2	8	20
01	0.5	1	4	10
10	0.25	0.5	2	5
11	0.125	0.25	1	2.5

8.4 LA_CTRL_REG3 (22h)

Table 24. LA_CTRL_REG3 register

IHL	PP_OD	LIR2	I2_CFG1	I2_CFG0	LIR1	I1_CFG1	I1_CFG0

Table 25. LA_CTRL_REG3 description

IHL	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/open drain selection on interrupt pad. Default value 0. (0: push-pull; 1: open drain)
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
I2_CFG1, I2_CFG0	Data signal on INT 2 pad control bits. Default value: 00. (see table below)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
I1_CFG1, I1_CFG0	Data signal on INT 1 pad control bits. Default value: 00. (see table below)

Table 26. Data signal on INT 1 and INT 2 pad

I1(2)_CFG1	I1(2)_CFG0	INT 1(2) Pad
0	0	Interrupt 1 (2) source
0	1	Interrupt 1 source OR Interrupt 2 source
1	0	Data ready
1	1	Boot running

8.5 LA_CTRL_REG4 (23h)

Table 27. LA_CTRL_REG4 register

BDU	BLE	FS1	FS0	STsign	0	ST	SIM

Table 28. LA_CTRL_REG4 description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated between MSB and LSB reading)
BLE	Big/little endian data selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
FS1, FS0	Full-scale selection. Default value: 00. (00: ±2 *g*; 01: ±4 *g*; 11: ±8 *g*)
STsign	Self-test sign. Default value: 00. (0: self-test plus; 1 self-test minus)
ST	Self-test enable. Default value: 0. (0: self-test disabled; 1: self-test enabled)
SIM	SPI serial interface mode selection. Default value: 0. (0: 4-wire interface; 1: 3-wire interface)

The BDU bit is used to inhibit output register updates between the reading of the upper and lower register parts. In default mode (BDU = '0'), the lower and upper register parts are updated continuously. If it is not certain to read faster than the output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output register is not updated until the upper (lower) part is read also. This feature avoids reading LSB and MSB related to different samples.

8.6 LA_CTRL_REG5 (24h)

Table 29. LA_CTRL_REG5 register

0	0	0	0	0	0	TurnOn1	TurnOn0

Table 30. LA_CTRL_REG5 description

TurnOn1, TurnOn0	Turn-on mode selection for sleep-to-wake function. Default value: 00.

TurnOn bits are used for turning on the **sleep-to-wake** function.

Table 31. Sleep-to-wake configuration

TurnOn1	TurnOn0	Sleep-to-wake status
0	0	Sleep-to-wake function is disabled
1	1	Turned on: The device is in low-power mode (ODR is defined in LA_CTRL_REG1)

By setting the TurnOn[1:0] bits to 11, the “sleep-to-wake” function is enabled. When an interrupt event occurs, the device is goes into normal mode, increasing the ODR to the value defined in LA_CTRL_REG1. Although the device is in normal mode, LA_CTRL_REG1 content is not automatically changed to “normal mode” configuration.

8.7 LA_HP_FILTER_RESET (25h)

Dummy register. Reading at this address instantaneously zeroes the content of the internal high-pass filter. If the high-pass filter is enabled, all three axes are instantaneously set to 0 *g*. This makes it possible to surmount the settling time of the high-pass filter.

8.8 REFERENCE (26h)

Table 32. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 33. REFERENCE description

Ref7 - Ref0	Reference value for high-pass filter. Default value: 00h.

This register sets the acceleration value taken as a reference for the high-pass filter output.

When the filter is turned on (at least one FDS, HPen2, or HPen1 bit is equal to ‘1’) and HPM bits are set to “01”, filter out is generated taking this value as a reference.

8.9 LA_STATUS_REG (27h)

Table 34. LA_STATUS_REG register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 35. LA_STATUS_REG description

ZYXOR	X, Y and Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous one before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous one)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous one)

Table 35. LA_STATUS_REG description (continued)

XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous one)
ZYXDA	X, Y and Z axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.10 LA_OUT_X_L (28h), LA_OUT_X_H (29h)

X-axis acceleration data. The value is expressed as two's complement.

8.11 LA_OUT_Y_L (2Ah), LA_OUT_Y_H (2Bh)

Y-axis acceleration data. The value is expressed as two's complement.

8.12 LA_OUT_Z_L (2Ch), LA_OUT_Z_H (2Dh)

Z-axis acceleration data. The value is expressed as two's complement.

8.13 LA_INT1_CFG (30h)

Table 36. LA_INT1_CFG register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 37. LA_INT1_CFG description

AOI	AND/OR combination of interrupt events. Default value: 0. (See *Table 38*)
6D	6 direction detection function enable. Default value: 0. (See *Table 38*)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

Table 37. LA_INT1_CFG description (continued)

ZLIE	Enable interrupt generation on Z Low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X Low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for Interrupt 1 source.

Table 38. Interrupt 1 source configurations

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

8.14 LA_INT1_SRC (31h)

Table 39. LA_INT1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 40. LA_INT1_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z High. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z Low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y High. Default value: 0 (0: no interrupt, 1: Y high event has occurred)

Table 40. LA_INT1_SRC description (continued)

YL	Y Low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X High. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X Low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Interrupt 1 source register. Read-only register.

Reading at this address clears LA_INT1_SRC IA bit (and the interrupt signal on INT 1 pin) and allows the refreshing of data in the LA_INT1_SRC register if the latched option was chosen.

8.15 LA_INT1_THS (32h)

Table 41. LA_INT1_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 42. LA_INT1_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.16 LA_INT1_DURATION (33h)

Table 43. LA_INT1_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 44. LA_INT2_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.17 LA_INT2_CFG (34h)

Table 45. LA_INT2_CFG register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 46. LA_INT2_CFG description

AOI	AND/OR combination of Interrupt events. Default value: 0. (See table below)
6D	6 direction detection function enable. Default value: 0. (See table below)
ZHIE	Enable interrupt generation on Z High event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z Low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y High event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y Low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X High event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X Low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for Interrupt 2 source.

Table 47. Interrupt mode configuration

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

8.18 LA_INT2_SRC (35h)

Table 48. LA_INT2_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 49. LA_INT2_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z High. Default value: 0 (0: no interrupt, 1: Z High event has occurred)
ZL	Z Low. Default value: 0 (0: no interrupt; 1: Z Low event has occurred)
YH	Y High. Default value: 0 (0: no interrupt, 1: Y High event has occurred)
YL	Y Low. Default value: 0 (0: no interrupt, 1: Y Low event has occurred)
XH	X High. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X Low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Interrupt 2 source register. Read-only register.

Reading at this address clears the LA_INT2_SRC IA bit (and the interrupt signal on INT 2 pin) and allows the refreshing of data in the LA_INT2_SRC register if the latched option was chosen.

8.19 LA_INT2_THS (36h)

Table 50. LA_INT2_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 51. LA_INT2_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.20 LA_INT2_DURATION (37h)

Table 52. LA_INT2_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 53. LA_INT2_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

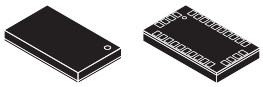
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

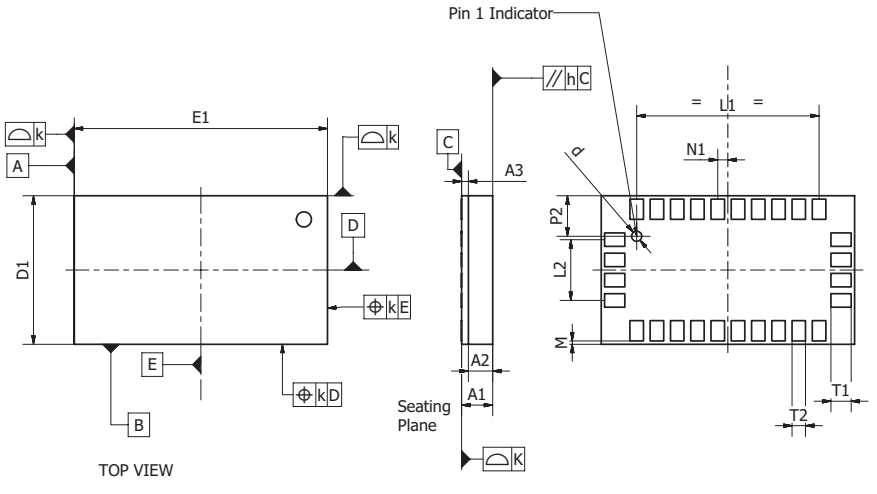
Figure 11. LGA-28: mechanical data and package dimensions

Dim.	mm		
	Min.	Typ.	Max.
A1			1.1
A2		0.855	
A3		0.2	
D1	4.25	4.4	4.55
E1	7.25	7.5	7.55
N1		0.3	
L1		5.4	
L2		1.8	
P2		1.2	
T1		0.6	
T2		0.4	
M		0.1	
d		0.3	
k		0.05	
h		0.1	

Outline and mechanical data



LGA-28L (4.4x7.5x1.1mm)
Land Grid Array Package



10 Ordering information

Table 54. Device summary

Order code	Temperature. range [°C]	Package [mm]	Packing
LSM320HAY30	-40 to +85	LGA-28 (4.4x7.5x1.1)	Tray
LSM320HAY30TR			Tape and reel

11 Revision history

Table 55. Document revision history

Date	Revision	Changes
16-Dec-09	1	First issue.

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