

SMD Efficient Fast Recovery Rectifier

CEFL101-G Thru CEFL105-G (RoHS Device)

Reverse Voltage: 50 ~ 600 Volts

Forward Current: 1.0 Amp

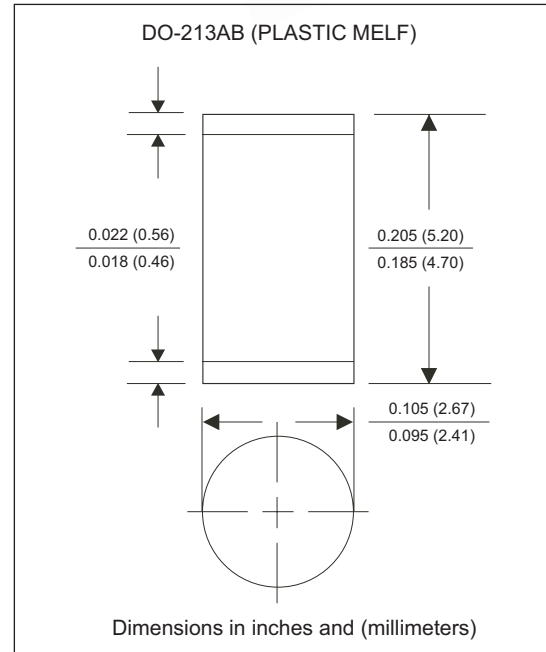


Features:

- Ideal for surface mount applications
- Easy pick and place
- Plastic package has Underwriters Lab. flammability classification 94V-0.
- Built-in strain relief
- High surge current capability

Mechanical Data:

- Case: JEDEC DO-213AB molded plastic
- Terminals: solderable per MIL-STD-750, method 2026
- Polarity: Color band denotes cathode end
- Mounting position: Any
- Approx. Weight: 0.116 gram



Maximum Ratings and Electrical Characteristics:

| Parameter | Symbol | CEFL101-G | CEFL102-G | CEFL103-G | CEFL104-G | CEFL105-G | Unit |
|--|-----------------|-------------|-----------|-----------|-----------|-----------|---------------|
| Max. Repetitive Peak Reverse Voltage | V_{RRM} | 50 | 100 | 200 | 400 | 600 | V |
| Max. DC Blocking Voltage | V_{DC} | 50 | 100 | 200 | 400 | 600 | V |
| Max. RMS Voltage | V_{RMS} | 35 | 70 | 140 | 280 | 420 | V |
| Peak Surge Forward Current 8.3ms single half sine-wave superimposed on rate load (JEDEC method) | I_{FSM} | 30 | | | | | A |
| Max. Average Forward Current | I_o | 1.0 | | | | | A |
| Max. Instantaneous Forward Voltage at 1.0A | V_F | 0.875 | | | 1.1 | 1.25 | V |
| Reverse recovery time | T_{rr} | 25 | | | 35 | 50 | nS |
| Max. DC Reverse Current at Rated DC Blocking Voltage $T_a=25^{\circ}C$ $T_a=100^{\circ}C$ | I_R | 5.0 250 | | | | | μA |
| Max. Thermal Resistance (Note1) | $R_{\theta JL}$ | 50 | | | | | $^{\circ}C/W$ |
| Max. Operating Junction Temperature | T_j | -55 to +155 | | | | | $^{\circ}C$ |
| Storage Temperature | T_{STG} | -55 to +125 | | | | | $^{\circ}C$ |

Note1: Thermal resistance from junction to lead 8.0mm square (0.13mm thick) land areas.



Rating and Characteristic Curves (CEFL101-G thru CEFL105-G)

Fig. 1 - Reverse characteristics

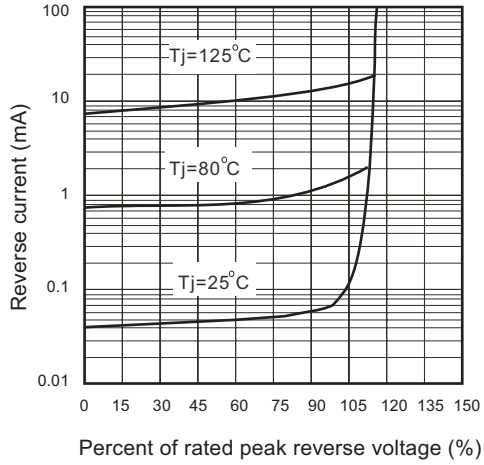


Fig.2 - Forward characteristics

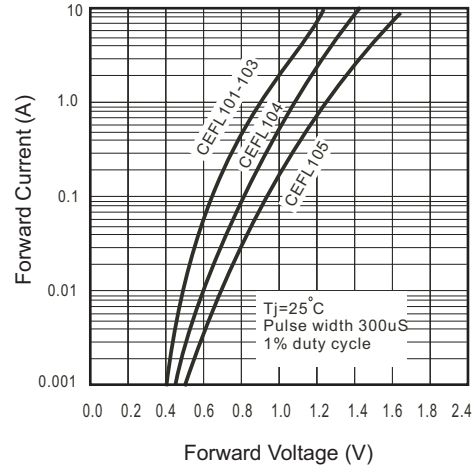


Fig. 3 - Junction Capacitance

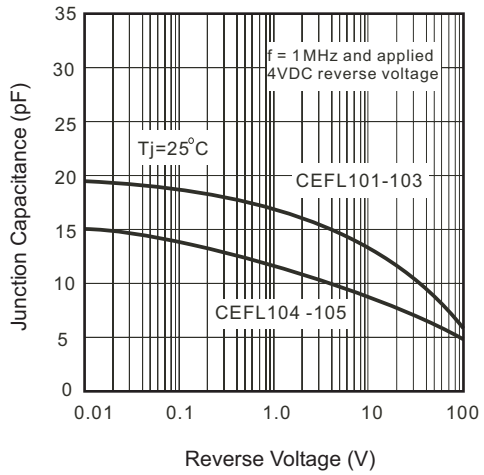


Fig.4 - Non Repetitive Forward Surge Current

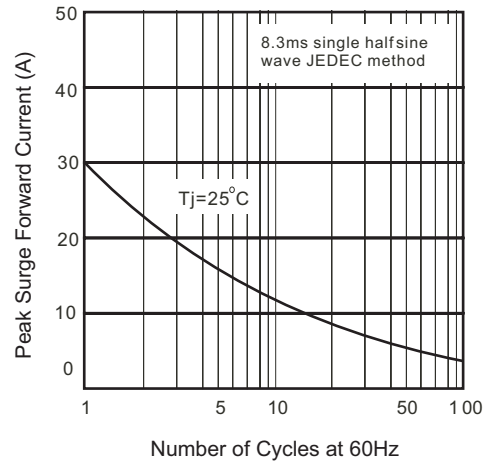


Fig. 5 - Test circuit diagram and Reverse recovery time characteristics

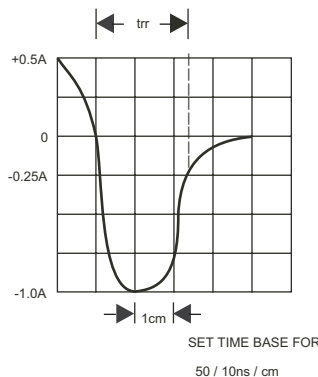
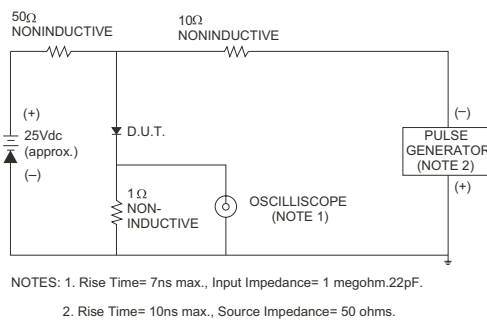


Fig. 6 - Current derating curve

