DATA SHEET

MIPS
PR31500
Poseidon embedded processor

Preliminary specification

1996 Sep 24

Version 0.1

Philips
Semiconductors

PHILIPS

Poseidon embedded processor

MIPS PR31500

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GENERAL DESCRIPTION

PR31500 Processor is a single-chip, low-cost, integrated embedded processor consisting of MIPS R3000 core and system support logic to interface with various types of devices.

PR31500 consists of a MIPS R3000 RISC CPU with 4 KBytes of instruction cache memory and 1 KByte of data cache memory, plus integrated functions for interfacing to numerous system components and external I/O modules. The R3000 RISC CPU is also augmented with a multiply/accumulate module to allow integrated DSP functions, such as a software modem for high-performance standard data and fax protocols.

The PR31500 processor can support both Little and Big Endian operating systems. In addition the PR31500 provides a memory management unit with an on-chip Translation Look aside Buffer (TLB) for very fast virtual to physical address translation.

PR31500 also contains multiple DMA channels and a high-performance and flexible Bus Interface Unit (BIU) for providing an efficient means for transferring data between external system memory, cache memory, the CPU core, and external I/O modules. The types of external memory devices supported include dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), static random access memory (SRAM), Flash memory, read-only memory (ROM), and expansion cards (e.g., PCMCIA). PR31500 also contains a System Interface Module (SIM) containing integrated functions for interfacing to numerous external I/O modules such as liquid crystal displays (LCDs), the UCB1100 (which handles most of the analog functions of the system, including sound and telecom codecs and touchscreen ADC), ISDN/high-speed serial, infrared, wireless peripherals, etc. Lastly, PR31500 contains support for implementation of power management, whereby various PR31500 internal modules and external subsystems can be individually (under software control) powered up and down.

Figure 1 shows an External Block Diagram of PR31500.

FEATURES

- 32-bit R3000 RISC static CMOS CPU
- 4 KByte instruction cache
- 1 KByte data cache
- Multiply/accumulator Instruction
- R3000A memory management unit with on-chip TLB
- Supports Big/Little Endian operating systems
- On-chip peripherals with individual power-down
  - Multi-channel DMA controller
  - Bus interface unit
  - Memory controller for ROM, Flash, RAM, DRAM, SDRAM, SRAM, and PCMCIA
  - Power management module
  - Video module
  - Real-time clock 32.760KHz reference
  - High-speed serial interface
  - Infrared module
  - Dual-UART
  - SPI bus
- 3.3V supply voltage
- 208-pin LQFP (Low profile quad flat pack)
- 40MHz operation frequency

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE (°C) AND PACKAGE	FREQUENCY (MHz)	DRAWING NUMBER
PR31500ABC	0 to +70, 208-pin Low Profile Quad Flat Pack	40	LQFP208

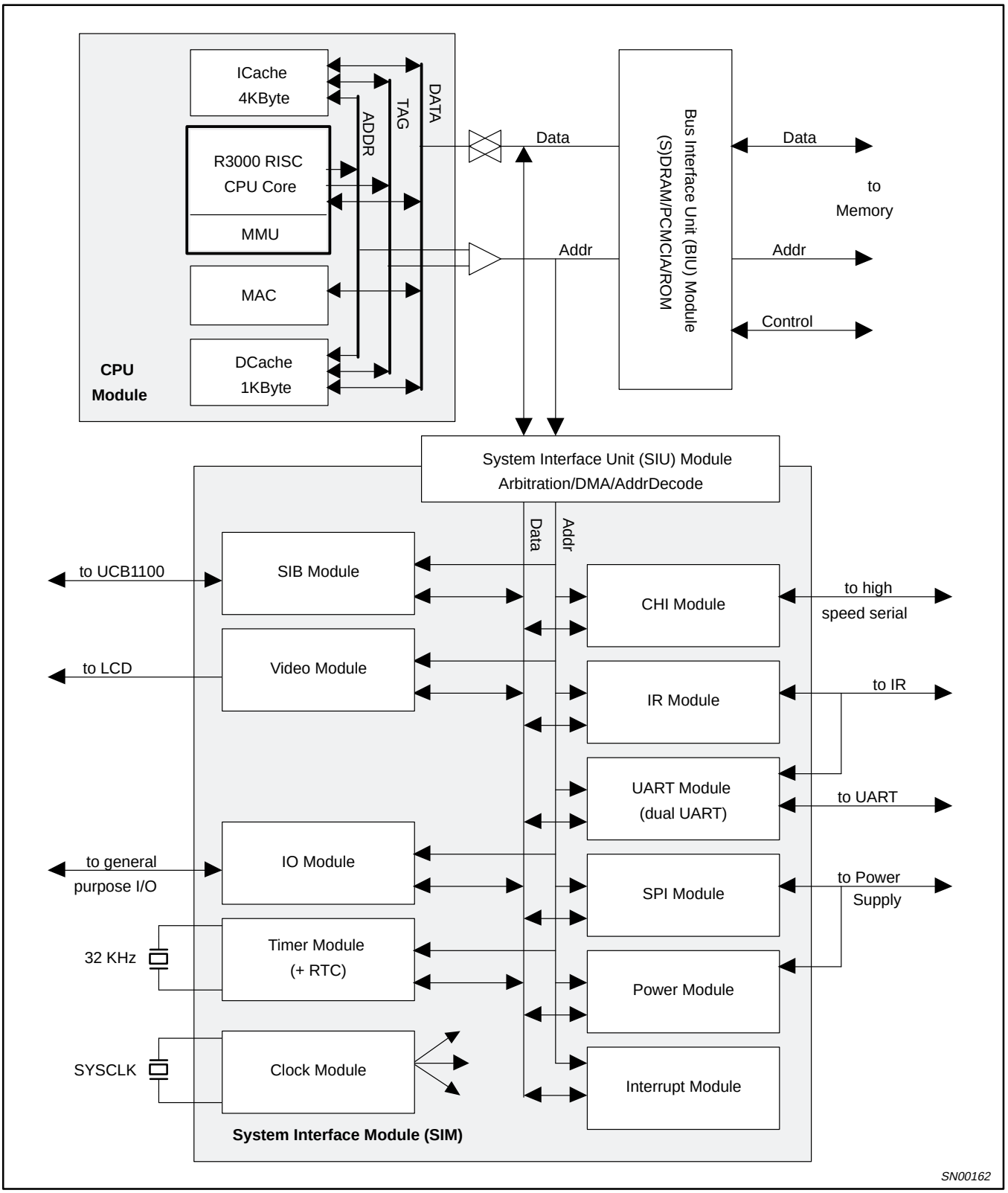


Figure 1. PR31500 Block Diagram

OVERVIEW

Each of the on-chip peripherals consist of:

BIU Module

- System memory and PR31500 Bus Interface Unit (BIU)
  - supports up to 2 banks of physical memory
  - supports self-refreshing DRAM and SDRAM
  - programmable parameters for each bank of DRAM or SDRAM (row/column address configuration, refresh, burst modes, etc.)
- programmable chip select memory access
  - 4 programmable (size, wait states, burst mode control) memory device and general purpose chip selects
    available for system ROM, SRAM, Flash
    available for external port expansion registers
- supports up to 2 identical full PCMCIA ports
  - PR31500 and UCB1100 provide the control signals and accepts the status signals which conform to the PCMCIA version 2.01 standard
  - appropriate connector keying and level-shifting buffers required for 3.3V versus 5V PCMCIA interface implementations

SIU Module

- multi-channel 32-bit DMA controller and System Interface Unit (SIU)
- independent DMA channels for video, SIB to/from UCB1100 audio/telecom codecs, high-speed serial port, IR UART, and general purpose UART
- address decoding for submodules within System Interface Module (SIM)

CPU Module

- R3000 RISC central processing unit core
  - full 32-bit operation (registers, instructions, addresses)
  - 32 general purpose 32-bit registers; 32-bit program counter
  - MIPS RISC Instruction Set Architecture (ISA) supported
- on-chip cache
  - 4 KByte direct-mapped instruction cache (I-cache)
    physical address tag and valid bit per cache line
    programmable burst size
    instruction streaming mode supported
  - 1 KByte data cache (D-cache)
    physical address tag and valid bit per cache line
    programmable burst size
    write-through
  - cache address snoop mode supported for DMA
  - 4-level deep write buffer
- Memory Management Unit
  - MIPS R3000A MMU contains on-chip TLB with:
    32×64 bit wide entries
    fully associative
    2 entry micro TLB for very fast instruction address translation
    Instruction address translation accesses full TLB after micro TLB miss
    Data address translation accesses full TLB
- high-speed multiplier/accumulator
  - on-chip hardware multiplier
  - supports 16x16 or 32x32 multiplier operations, with 64-bit accumulator
  - existing multiply instructions are enhanced and new multiply and add instructions are added to R3000 instruction set to improve the performance of DSP applications
- CPU interface
  - handles data bus, address bus, and control interface between CPU core and rest of PR31500 logic

Clock Module

- PR31500 supports system-wide single crystal configuration, besides the 32 KHz RTC XTAL (reduces cost, power, and board space)
- common crystal rate divided to generate clock for CPU, video, sound, telecom, UARTs, etc.
- external system crystal rate is vendor-dependent
- independent enabling or disabling of individual clocks under software control, for power management

CHI Module

- high-speed serial Concentration Highway Interface (CHI) contains logic for interfacing to external full-duplex serial time-division-multiplexed (TDM) communication peripherals
- supports ISDN line interface chips and other PCM/TDM serial devices
- CHI interface is programmable (number of channels, frame rate, bit rate, etc.) to provide support for a variety of formats
- supports data rates up to 4.096 Mbps
- independent DMA support for CHI receive and transmit

Interrupt Module

- contains logic for individually enabling, reading, and clearing all PR31500 interrupt sources
- interrupts generated from internal PR31500 modules or from edge transitions on external signal pins

IO Module

- contains support for reading and writing the 7 bi-directional general purpose IO pins and the 32 bi-directional multi-function IO pins
- each IO port can generate a separate positive and negative edge interrupt
- independently configurable IO ports allow PR31500 to support a flexible and wide range of system applications and configurations

IR Module

- IR consumer mode
  - allows control of consumer electronic devices such as stereos, TVs, VCRs, etc.
  - programmable pulse parameters
  - external analog LED circuitry
- IRDA communication mode
  - allows communication with other IRDA devices such as FAX machines, copiers, printers, etc.
  - supported by UART module within PR31500
  - external analog receiver preamp and LED circuitry
  - data rate = up to 115 Kbps at 1 meter
- IR FSK communication mode
  - supported by UART module within PR31500
  - external analog IR chip(s) perform frequency modulation to generate the desired IR communication mode protocol
  - data rate = up to 36000 bps at 3 meters
- carrier detect state machine
  - periodically enables IR receiver to check if a valid carrier is present

Power Module

- power-down modes for individual internal peripheral modules
- serial (SPI port) power supply control interface supported
- power management state machine has 4 states: RUNNING, DOZING, SLEEP, and COMA

Serial Interconnect Bus (SIB) Module

- PR31500 contains holding and shift registers to support the serial interface to the UCB1100 and/or other optional codec devices
- interface compatible with slave mode 3 of Crystal CS4216 codec
- synchronous, frame-based protocol
- PR31500 always master source of clock and frame frequency and phase; programmable clock frequency
- each SIB frame consists of 128 clock cycles, further divided into 2 subframes or words of 64 bits each (supports up to 2 devices simultaneously)
- independent DMA support for audio receive and transmit, telecom receive and transmit
- supports 8-bit or 16-bit mono telecom formats
- supports 8-bit or 16-bit mono or stereo audio formats
- independently programmable audio and telecom sample rates
- CPU read/write registers for subframe control and status

System Peripheral Interface (SPI) Module

- provides interface to SPI peripherals and devices
- full-duplex, synchronous serial data transfers (data in, data out, and clock signals)
- PR31500 supplies dedicated chip select and interrupt for an SPI interface serial power supply
- 8-bit or 16-bit data word lengths for the SPI interface
- programmable SPI baud rate

Timer Module

- Real Time Clock (RTC) and Timer
- 40-bit counter (30.517 µsec granularity); maximum uninterrupted time = 388.36 days
- 40-bit alarm register (30.517 µsec granularity)
- 16-bit periodic timer (0.868 µsec granularity); maximum timeout = 56.8 msec
- interrupts on alarm, timer, and prior to RTC roll-over

UART Module

- 2 independent full-duplex UARTs
- programmable baud rate generator
- UART-A port used for serial control interface to external IR module
- UART-B port used for general purpose serial control interface
- UART-A and UART-B DMA support for receive and transmit

Video Module

- bit-mapped graphics
- supports monochrome, grey scale, or color modes
- time-based dithering algorithm for grey scale and color modes
- supports multiple screen sizes
- supports split and non-split displays
- variable size and relocatable video buffer
- DMA support for fetching image data from video buffer

Little/Big Endian Configuration

The PR31500 can be configures as a Big Endian or as a Little Endian processor based on the /LB endian pin at power-up.

The byte ordering is as follows:

LITTLE ENDIAN	BIG ENDIAN
D[31:24]	D[7:0]
D[23:16]	D[15:8]
D[15:8]	D[23:16]
D[7:0]	D[31:24]
/CAS3	/CAS0
/CAS2	/CAS1
/CAS1	/CAS2
/CAS0	/CAS3

Figure 2 shows a typical system block diagram cosisting of PR31500 and UCB1100 for a total system solution.

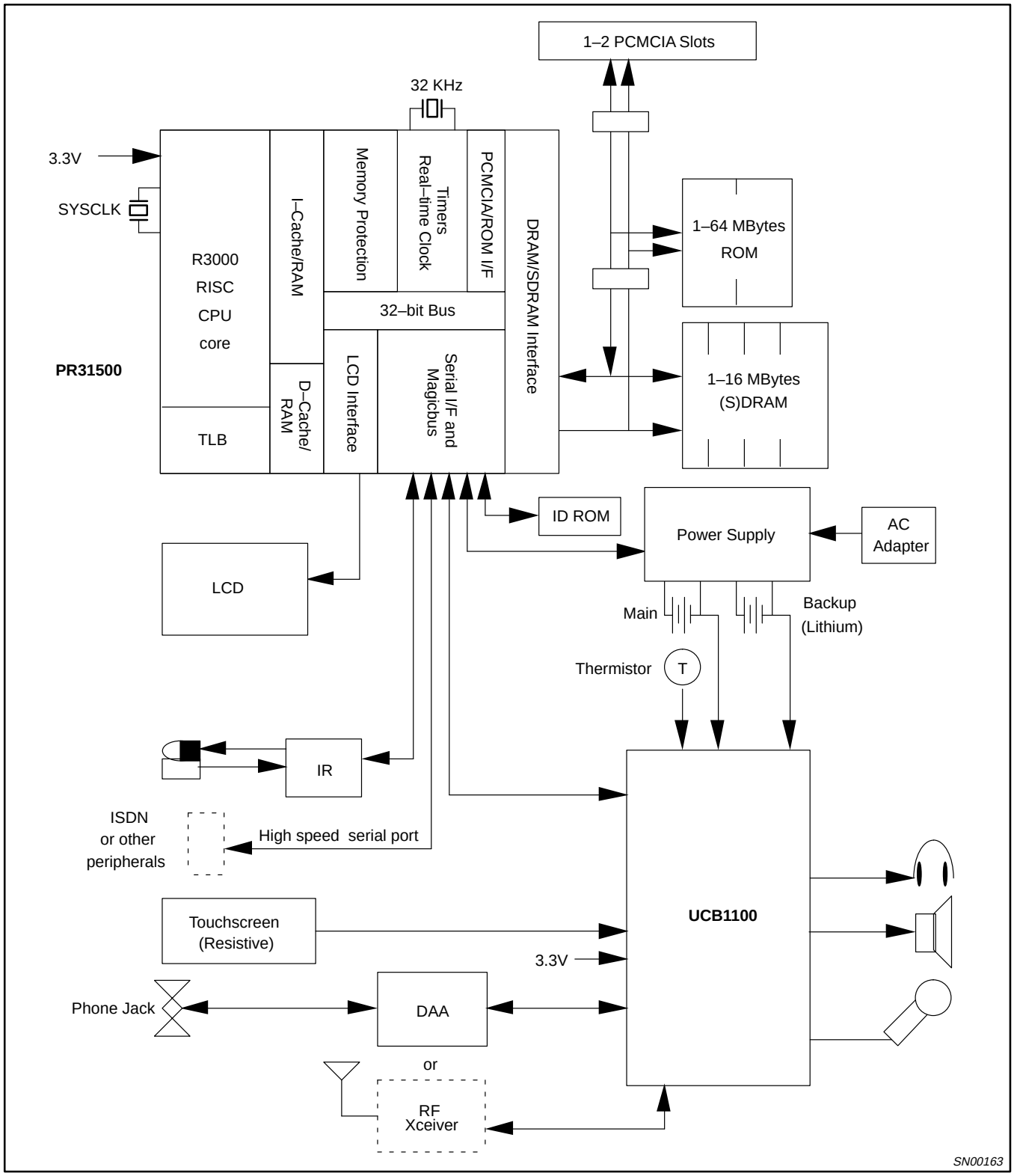
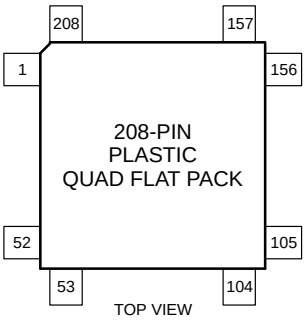


Figure 2. System Block Diagram

PIN CONFIGURATION



Pin	Function		Pin	Function	Pin	Function		Pin	Function	
1	V_{DD}		53	V_{DD}	105	/CARD2WAIT		157	D(17)	[D(9)]
2	D(0)	[D(24)]	54	RXD	106	/CARD2CSH		158	V_{SS}	
3	V_{SS}		55	TXD	107	/CARD2CSL		159	D(16)	[D(8)]
4	D(1)	[D(25)]	56	IO(4)	108	IO(0)		160	V_{DD}	
5	D(2)	[D(26)]	57		109	V_{SS}		161		
6	V_{DD}		58	IRIN	110	/IORD		162	/CS0	
7	D(3)	[D(27)]	59	IROUT	111	/IOWR		163	/RD	
8	V_{SS}		60	V_{SS}	112	/CARDREG		164	V_{SS}	
9	D(4)	[D(28)]	61	V_{DD}	113	/CARD1WAIT		165	V_{DD}	
10	V_{DD}		62	CARDET	114	V_{DD}		166	/DGRNT	
11	D(5)	[D(29)]	63	TXPWR	115	MFIO(2)		167	/DREQ	
12	D(6)	[D(30)]	64	IO(3)	116	V_{DD}		168	ALE	
13	V_{SS}		65	IO(2)	117	/CARD1CSL		169	/WE	
14	D(7)	[D(31)]	66	V_{SS}	118	/CARD1CSH		170	V_{DD}	
15	V_{SS}		67	SPICLK	119	V_{SS}		171	A(12)	
16	D(8)	[D(16)]	68	SPIIN	120	/MCS3		172	A(11)	
17	V_{DD}		69	SPIOUT	121	/MCS2		173	V_{SS}	
18	D(9)	[D(17)]	70	V_{DD}	122	/MCS1		174	A(10)	
19	D(10)	[D(18)]	71	TESTCPU	123	/MCS0		175	A(9)	
20	V_{SS}		72	TESTIN	124	/CS3		176	V_{DD}	
21	D(11)	[D(19)]	73	VIDDONE	125	/CS2		177	A(8)	
22	V_{DD}		74	TESTSIU	126	/CS1		178	A(7)	
23	D(12)	[D(20)]	75	V_{SS}	127	V_{DD}		179	V_{SS}	
24	D(13)	[D(21)]	76	$V_{CC}3$	128	SYSCLKIN		180	A(6)	
25	V_{SS}		77	BC32K	129	SYSCLKOUT		181	A(5)	
26	D(14)	[D(22)]	78	V_{DD}	130	V_{SS}		182	V_{DD}	
27	D(15)	[D(23)]	79	C32KIN	131	V_{SS}		183	A(4)	
28	V_{DD}		80	C32KOUT	132	V_{DD}		184	V_{SS}	
29	/LB endian		81	V_{SS}	133	D(31)	[D(7)]	185	A(3)	
30	MFIO(1)		82	PWRCS	134	D(30)	[D(6)]	186	A(2)	
31	–		83	PWRINT	135	V_{SS}		187	V_{DD}	
32	–		84	PWROK	136	D(29)	[D(5)]	188	A(1)	
33	V_{SS}		85		137	V_{DD}		189	A(0)	
34	–		86	ONBUTN	138	D(28)	[D(4)]	190	V_{SS}	
35	V_{DD}		87	/PON	139	D(27)	[D(3)]	191	V_{SS}	
36	V_{DD}		88	/CPURES	140	V_{SS}		192	/DCS0	
37	SIBMCLK		89	V_{DD}	141	D(26)	[D(2)]	193	/RAS1	
38	V_{SS}		90	DISPON	142	V_{SS}		194	/RAS0	
39	SIBSCLK		91	FRAME	143	D(25)	[D(1)]	195	/CAS3	[/CAS0]
40	SIBSYNC		92	V_{SS}	144	V_{DD}		196	V_{DD}	
41	SIBDIN		93	DF	145	D(24)	[D(0)]	197	/CAS2	[/CAS1]
42	SIBDOUT		94	LOAD	146	D(23)	[D(15)]	198	/CAS1	[/CAS2]
43	V_{DD}		95	CP	147	V_{DD}		199	/CAS0	[/CAS3]
44	SIBIRQ		96	V_{SS}	148	D(22)	[D(14)]	200	V_{SS}	
45	MFIO(0)		97	V_{DD}	149	V_{SS}		201	V_{DD}	
46	IO(6)		98	VDAT(0)	150	D(21)	[D(13)]	202	DCKE	
47	IO(50		99	VDAT(1)	151	V_{DD}		203	V_{SS}	
48	V_{SS}		100	VDAT(2)	152	D(20)	[D(12)]	204	DCLKIN	
49	chiclk		101	VDAT(3)	153	D(19)	[D(11)]	205	DCLKOUT	
50	chifs		102	V_{SS}	154	V_{SS}		206	V_{DD}	
51	chidin		103	IO(1)	155	D(18)	[D(10)]	207	DQMH	
52	chidout		104	V_{DD}	156	V_{DD}		208	DQML	

NOTE: [ ] indicates the signal name in the Little Endian mode.

SN00164

PIN DESCRIPTIONS

Overview

The PR31500 processor contains 208 pins consisting of input, output, bi-directional, and power and ground pins. These pins are used to support various functions. The following sections will describe the function of each pin including any special power-down considerations for each pin.

Pins

The PR31500 PROCESSOR contains 208 total pins, consisting of 136 signal pins, 4 spare pins, 34 power pins, and 34 ground pins. Of the 136 signal pins, 32 of them are multi-function and can be independently programmed either as IO ports or for an alternate standard/normal function. As an IO port, any of these pins can be programmed as an input or output port, with the capability of generating a separate positive and negative edge interrupt. See Section 2.3 for a summary of the multi-function IO ports versus their standard functions.

PIN #	NAME	TYPE	NAME AND FUNCTION
Memory Pins			
	D(31:0)	I/O	These pins are the data bus for the system. 8-bit SDRAMs should be connected to bits 7:0 and 16-bit SDRAMs and DRAMs should be connected to bits 15:0. All other 16-bit ports should be connected to bits 31:16. Of course, 32-bit ports should be connected to bits 31:0. These pins are normally outputs and only become inputs during reads, thus no resistors are required since the bus will only float for a short period of time during bus turn-around.
	A(12:0)	O	These pins are the address bus for the system. The address lines are multiplexed and can be connected directly to SDRAM and DRAM devices. To generate the full 26-bit address for static devices, an external latch must be used to latch the signals using the ALE signal. For static devices, address bits 25:13 are provided by the external latch and address bits 12:0 (directly connected from PR31500's address bus) are held afterward by PR31500 processor for the remainder of the address bus cycle.
168	ALE	O	This pin is used as the address latch enable to latch A(12:0) using an external latch, for generating the upper address bits 25:13.
163	/RD	O	This pin is used as the read signal for static devices. This signal is asserted for reads from /MCS3-0, /CS3-0, /CARD2CS and /CARD1CS for memory and attribute space, and for reads from PR31500 processor accesses if SHOWPR31500 is enabled (for debugging purposes).
169	/WE	O	This pin is used as the write signal for the system. This signal is asserted for writes to /MCS3-0, /CS3-0, /CARD2CS and /CARD1CS for memory and attribute space, and for writes to DRAM and SDRAM.
199	/CAS0 (/WE0)	O	This pin is used as the CAS signal for SDRAMs, the CAS signal for D(7:0) for DRAMs, and the write enable signal for D(7:0) for static devices.
198	/CAS1 (/WE1)	O	This pin is used as the CAS signal for D(15:8) for DRAMs and the write enable signal for D(15:8) for static devices.
197	/CAS2 (/WE2)	O	This pin is used as the CAS signal for D(23:16) for DRAMs and the write enable signal for D(23:16) for static devices.
195	/CAS3 (/WE3)	O	This pin is used as the CAS signal for D(31:24) for DRAMs and the write enable signal for D(31:24) for static devices.
194	/RAS0	O	This pin is used as the RAS signal for SDRAMs and the RAS signal for Bank0 DRAMs.
193	/RAS1 (/DCS1)	O	This pin is used as the chip select signal for Bank1 SDRAMs and the RAS signal for Bank1 DRAMs.
192	/DCS0	O	This pin is used as the chip select signal for Bank0 SDRAMs.
202	DCKE	O	This pin is used as the clock enable for SDRAMs.
204	DCLKIN	I	This pin must be tied externally to the DCLKOUT signal and is used to match skew for the data input when reading from SDRAM and DRAM devices.
205	DCLKOUT	O	This pin is the (nominal) 73.728 MHz clock for the SDRAMs.
207	DQMH	O	This pin is the upper data mask for a 16-bit SDRAM configuration.
208	DQML	O	This pin is the lower data mask for a 16-bit SDRAM or 8-bit SDRAM configuration.
124–126, 162	/CS3–0	O	These pins are the Chip Select 3 through 0 signals. They can be configured to support either 32-bit or 16-bit ports.
120–123	/MCS3–0	O	These pins are the MagicCard Chip Select 3 through 0 signals. They only support 16-bit ports.
106, 107	/CARD2CSH,L	O	These pins are the Chip Select signals for PCMCIA card slot 2.

PIN #	NAME	TYPE	NAME AND FUNCTION
Memory Pins (continued)			
117, 118	/CARD1CSH,L	O	These pins are the Chip Select signals for PCMCIA card slot 1.
112	/CARDREG	O	This pin is the /REG signal for the PCMCIA cards.
110	/CARDIORD	O	This pin is the /IORD signal for the PCMCIA IO cards.
111	/CARDIOWR	O	This pin is the /IOWR signal for the PCMCIA IO cards.
115	/CARDDIR	O	This pin is used to provide the direction control for bi-directional data buffers used for the PCMCIA slot(s). This signal will assert whenever /CARD2CSH or /CARD2CSL or /CARD1CSH or /CARD1CSL is asserted and a read transaction is taking place.
105	/CARD2WAIT	I	This pin is the card wait signal from PCMCIA card slot 2.
113	/CARD1WAIT	I	This pin is the card wait signal from PCMCIA card slot 1.
Bus Arbitration Pins			
167	/DREQ	I	This pin is used to request external arbitration. If the TESTSIU signal is high and the TESTSIU function has been enabled, then once /DGRNT is asserted, external logic can initiate reads or writes to PR31500 processor registers by driving the appropriate input signals. If the TESTSIU signal is low or the TESTSIU function has not been enabled, then PR31500 memory transactions are halted and certain memory signals will be tri-stated when /DGRNT is asserted in order to allow an external master to access memory.
166	/DGRNT	O	This pin is asserted in response to /DREQ to inform the external test logic or bus master that it can now begin to drive signals.
Clock Pins			
128	SYSCLKIN	I	This pin should be connected along with SYSCLKOUT to an external crystal which is the main PR31500 clock source.
129	SYSCLKOUT	O	This pin should be connected along with SYSCLKIN to an external crystal which is the main PR31500 clock source.
79	C32KIN	I	This pin along with C32KOUT should be connected to a 32.768 KHz crystal.
80	C32KOUT	O	This pin along with C32KIN should be connected to a 32.768 KHz crystal.
77	BC32K	O	This pin is a buffered output of the 32.768 KHz clock.
CHI Pins			
50	CHIFS	I/O	This pin is the CHI frame synchronization signal. This pin is available for use in one of two modes. As an output, this pin allows PR31500 to be the master CHI sync source. As an input, this pin allows an external peripheral to be the master CHI sync source and the PR31500 CHI module will slave to this external sync.
49	CHICLK	I/O	This pin is the CHI clock signal. This pin is available for use in one of two modes. As an output, this pin allows PR31500 to be the master CHI clock source. As an input, this pin allows an external peripheral to be the master CHI clock source and the PR31500 CHI module will slave to this external clock.
52	CHIDOUT	O	This pin is the CHI serial data output signal.
51	CHIDIN	I	This pin is the CHI serial data input signal.
IO Pins			
46, 107, 47, 108, 56, 64, 64	IO(6:0)	I/O	These pins are general purpose input/output ports. Each port can be independently programmed as an input or output port. Each port can generate a separate positive and negative edge interrupt. Each port can also be independently programmed to use a 16 to 24 msec debouncer.
30, 45	MFIO(1:0)	I/O	These pins are multi-function input/output ports. Each port can be independently programmed as an input or output port, or can be programmed for multi-function use to support vendor-dependent test signals (for debugging purposes only). Each port can generate a separate positive and negative edge interrupt. Note that 30 other multi-function pins are available for usage as multi-function input/output ports. These pins are named after their respective standard/normal function and are not listed here.
Endian Processor Pin			
29	/LB endian	I	Little/Big Endian. This pin, when pulled Low at power-up, configures the PR31500 as a Little Endian. When this pin is pulled High at power-up, it configures the PR31500 as a Big Endian processor.

PIN #	NAME	TYPE	NAME AND FUNCTION
Reset Pins			
88	/CPURES	I	This pin is used to reset the CPU core. This pin should be connected to a switch for initiating a reset in the event that a software problem might hang the CPU core. The pin should also be pulled up to VSTANDBY through an external pull-up resistor.
87	/PON	I	This pin serves as the Power On Reset signal for PR31500. This signal must remain low when VSTANDBY is asserted until VSTANDBY is stable. Once VSTANDBY is asserted, this signal should never go low unless all power is lost in the system.
Power Supply Pins			
86	ONBUTN	I	This pin is used as the On Button for the system. Asserting this signal will cause PWRCS to set to indicate to the System Power Supply to turn power on to the system. PWRCS will not assert if the PWROK signal is low.
82	PWRCS	O	This pin is used as the chip select for the System Power Supply. When the system is off, the assertion of this signal will cause the System Power Supply to turn VCCDRAM and VCC3 on to power up the system. The Power Supply will latch SPI commands on the falling edge of PWRCS.
84	PWROK	I	This pin provides a status from the System Power Supply that there is a good source of power in the system. This signal typically will be asserted if there is a Battery Charger supplying current or if the Main Battery is good and the Battery Door is closed. If PWROK is low when the system is powered off, PWRCS will not assert as a result of the user pressing the ONBUTN or an interrupt attempting to wake up the system. If the device is on when the PWROK signal goes low, the software will immediately shut down the system since power is about to be lost. When PWROK goes low, there must be ample warning so that the software can shut down the system before power is actually lost.
83	PWRINT	I	This pin is used by the System Power Supply to alert the software that some status has changed in the System Power Supply and the software should read the status from the System Power Supply to find out what has changed. These will be low priority events, unlike the PWROK status, which is a high priority emergency case.
76	VCC3	I	This pin provides the status of the power supply for the ROM, UCB1100, system buffers, and other transient components in the system. This signal will be asserted by the System Power Supply when PWRCS is asserted, and will always be turned off when the system is powered down.
SIB Pins			
41	SIBDIN	I	This pin contains the input data shifted from UCB1100 and/or external codec device.
42	SIBDOUT	O	This pin contains the output data shifted to UCB1100 and/or external codec device.
39	SIBSCLK	O	This pin is the serial clock sent to UCB1100 and/or external codec device. The programmable SIBSCLK rate is derived by dividing down from SIBMCLK.
40	SIBSYNC	O	This pin is the frame synchronization signal sent to UCB1100 and/or external codec device. This frame sync is asserted for one clock cycle immediately before each frame starts and all devices connected to the SIB monitor SIBSYNC to determine when they should transmit or receive data.
44	SIBIRQ	I	This pin is a general purpose input port used for the SIB interrupt source from UCB1100. This interrupt source can be configured to generate an interrupt on either a positive and/or negative edge.
37	SIBMCLK	I/O	This pin is the master clock source for the SIB logic. This pin is available for use in one of two modes. First, SIBMCLK can be configured as a high-rate output master clock source required by certain external codec devices. In this mode all SIB clocks are synchronously slaved to the main PR31500 system clock CLK2X. Conversely, SIBMCLK can be configured as an input slave clock source. In this mode, all SIB clocks are derived from an external SIBMCLK oscillator source, which is asynchronous with respect to CLK2X. Also, for this mode, SIBMCLK can still be optionally used as a high-rate master clock source required by certain external codec devices.
SPI Pins			
67	SPICLK	O	This pin is used to clock data in and out of the SPI slave device.
69	SPIOUT	O	This pin contains the data that is shifted into the SPI slave device.
68	SPIIN	I	This pin contains the data that is shifted out of the SPI slave device.

PIN #	NAME	TYPE	NAME AND FUNCTION
UART and IR Pins			
55	TXD	O	This pin is the UART transmit signal from the UARTA module.
54	RXD	I	This pin is the UART receive signal to the UARTA module.
59	IROUT	O	This pin is the UART transmit signal from the UARTB module or the Consumer IR output signal if Consumer IR mode is enabled.
58	IRIN	I	This pin is the UART receive signal to the UARTB module.
	RXPWR	O	This pin is the receiver power output control signal to the external communication IR analog circuitry.
62	CARDET	I	This pin is the carrier detect input signal from the external communication IR analog circuitry.
Video Pins			
91	FRAME	O	This pin is the frame synchronization pulse signal between the Video Module and the LCD, and is used by the LCD to return it's pointers to the top of the display. The Video Module asserts FRAME after all the lines of the LCD have been shifted and transferred, producing a full frame of display.
93	DF	O	This pin is the AC signal for the LCD. Since LCD plasma tends to deteriorate whenever subjected to a DC voltage, the DF signal is used by the LCD to alternate the polarity of the row and column voltages used to turn the pixels on and off. The DF signal can be configured to toggle on every frame or can be configured to toggle every programmable number of LOAD signals.
94	LOAD	O	This pin is the line synchronization pulse signal between the Video Module and the LCD, and is used by the LCD to transfer the contents of it's horizontal line shift register to the LCD panel for display. The Video Module asserts LOAD after an entire horizontal line of data has been shifted into the LCD.
95	CP	O	This pin is the clock signal for the LCD. Data is pushed by the Video Module on the rising edge of CP and sampled by the LCD on the falling edge of CP.
101, 100, 99, 98	VDAT(3:0)	O	These pins are the data for the LCD. These signals are directly connected to the LCD for 4-bit non-split displays. For 4-bit split and 8-bit non-split displays, an external register is required to demultiplex the 4-bit data into the desired 8 parallel data lines needed for the LCD.
90	DISPON	O	This pin is the display-on enable signal for the LCD.
Test Pins			
74	TESTSIU	I	This pin allows external logic to initiate read or write transactions to PR31500 registers. The TESTSIU mode is enabled by toggling this signal after the device has powered up. Once the function is enabled, if the TESTSIU pin is high when the bus is arbitrated (using /DREQ and /DGRNT), then external logic can initiate read and write transactions to PR31500 registers. This pin is used for debugging purposes only.
71	TESTCPU	I	This pin allows numerous internal CPU core signals to be brought to external PR31500 pins, in place of the normal signals assigned to these pins. The CPU core signals assigned to their respective pins during TESTCPU mode are vendor-dependent. The TESTCPU mode is enabled by asserting this TESTCPU signal, and this function is provided for generating test vectors for the CPU core. This pin is used for debugging purposes only.
72	TESTIN	I	This pin is reserved for vendor-dependent use. This pin is used for debugging purposes only.
73	VIDDONE	O	This signal is used to synchronize UCB1100 to read touchscreen input, when there is no video data shifted into LCD panel.
Spare Pins			
	NC4–1	No Connect	These pins are reserved for future use and should be left unconnected.
34		–	Reserved.
32, 31		–	Reserved.
Power Supply Pins			
	V_{DD} (34 each)	+3.3V	These pins are the power pins for PR31500 and should be connected to the digital +3.3V power supply VSTANDBY.
	V_{SS} (34 each)	GND	These pins are the ground pins for PR31500 and should be connected to digital ground. **NOTE:** For some vendor-dependent implementations of PR31500, pin 131 may be used for a filter capacitor for the SYSCLK oscillator (capacitor connected between pin 131 and digital ground).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	Power supply voltage	V_{SS} – 0.5 to 4.5	V
V_{IN}	Input voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
T_{stg}	Storage temperature range	–55 to +125	°C
Pd	Maximum dissipation (T_{amb} = 70°C)	1	W

RECOMMENDED OPERATING CONDITION

V_{SS} = 0V

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Power supply voltage	3.0	3.3	3.6	V
V_{IN}	Input voltage	V_{SS}	–	V_{DD}	V
T_{opr}	Operating temperature range	0	–	70	°C

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 to +70°C, V_{DD} = 3.3 ± 0.3V.

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{DD}	Operating current	V_{IN} = V_{DD} or V_{SS}; V_{DD} = MAX I_{OH} = I_{OL} = 0	–	110	TBD	mA
I_{DDS}	Static current	V_{IN} = V_{DD} or V_{SS}; V_{DD} = MAX I_{OH} = I_{OL} = 0	–	10	100	µA
I_L	Input leakage current	V_{DD} = MAX; V_{IH} = V_{DD} V_{IL} = V_{SS}	–10	–	10	µA
V_{IH1}	High level input voltage[1]	V_{DD} = 3.6V	$V_{DD} \times 0.8$	–	V_{DD} + 0.3	V
V_{IL1}	Low level input voltage[1]	V_{DD} = 3.0V	–0.3	–	$V_{DD} \times 0.2$	V
V_{IH2}	High level input voltage[2]	V_{DD} = 3.6V	2.4	–	V_{DD} + 0.3	V
V_{IL2}	Low level input voltage[2]	V_{DD} = 3.0V	–0.3	–	0.6	V
V_{OH1}	High level output voltage[3]	V_{DD} = 3.0; I_{OH} = –4mA	V_{DD} – 0.6	–	–	V
V_{OL1}	Low level output voltage[3]	V_{DD} = 3.0; I_{OL} = 4mA	–	–	V_{SS} + 0.4	V
V_{OH2}	High level output voltage[4]	V_{DD} = 3.0; I_{OH} = –8mA	V_{DD} – 0.6	–	–	V
V_{OL2}	Low level output voltage[4]	V_{DD} = 3.0; I_{OL} = 8mA	–	–	V_{SS} + 0.4	V
V_{OH3}	High level output voltage[5]	V_{DD} = 3.0; I_{OH} = –16mA	V_{DD} – 0.6	–	–	V
V_{OL3}	Low level output voltage[5]	V_{DD} = 3.0; I_{OL} = 16mA	–	–	V_{SS} + 0.4	V
V_{OH4}	High level output voltage	V_{DD} = 3.0; I_{OH} = –24mA	V_{DD} – 0.6	–	–	V
V_{OL4}	Low level output voltage	V_{DD} = 3.0; I_{OL} = 24mA	–	–	V_{SS} + 0.4	V
I_{IHP}	Input current (pull-down resistor)	V_{DD} = MAX; V_{IN} = V_{DD}	20	–	120	µA

NOTES:
1. SYSVLKIN
2. Other inputs
3. D[31:0], /RAS0, /RAS1, /DCS0, /DCKE, DQMH, DQML, /DREQ, /DGRNT, BC32K, VDAT[3:0], CP, LOAD, DF, FRAME, DISPON, VIDDONE, PWRCS, TXD, RXD, /CS0~3, /MCS0~3, CHIFS, CHICLK, CHIDOUT, CHIDIN, IO[6:0], SPICLK, SPIOUT, SPIIN, SIBSYNC, SIBOUT, SIBMCLK, SIBCLK, RXPWR, IROUT, /CRAD1WAIT, /CARD2WAIT, MIOX[2:0]
4. A[12:0], ALE, /RD, /WE /CAS0~3, /CARDREG, /IOWR, /CARD1CSL, /CARD1CSH, /CARD2CSL, /CARD2CSH
5. DCLKOUT

AC ELECTRICAL CHARACTERISTICS

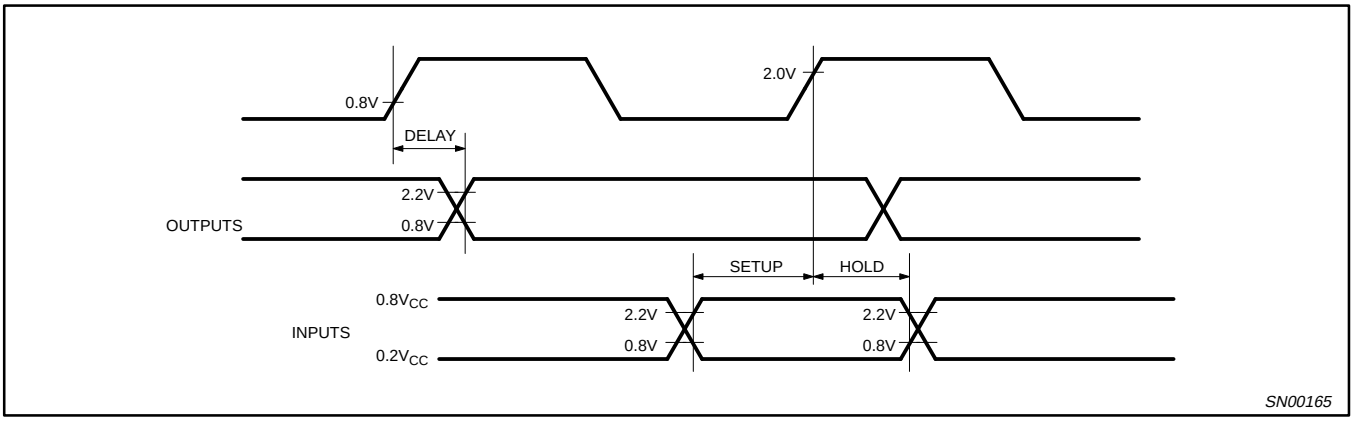
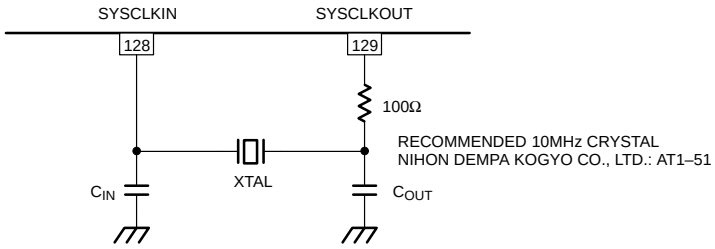


Figure 3. PR31500 Timing – Definition of AC Specification

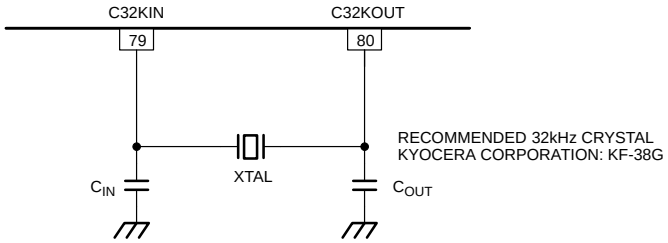
CRYSTAL OSCILLATOR CHARACTERISTICS

10MHz Crystal



SYMBOL	PARAMETER	RECOMMENDED VALUE		UNIT
		MIN.	MAX.	
	Crystal Oscillator			
f_{IN}	frequency	8.25	10	MHz
C_I	crystal impedance	TBD	TBD	kΩ
C_{IN}, C_{OUT}	External capacitors	10	33	pF

32kHz Crystal



SYMBOL	PARAMETER	RECOMMENDED VALUE		UNIT
		MIN.	MAX.	
C_{IN}, C_{OUT}	External capacitors	10	33	pF

MEMORY INTERFACE

T_{amb} = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, External Capacitance = 40pF

ITEM	PARAMETER	RISING/FALLING	LIMITS		UNIT
			MIN	MAX	
1	DCLKOUT high time	–	5.4	–	ns
2	DCLKOUT low time	–	5.4	–	ns
3	DCLKOUT period	–	13.5	–	ns
4	Delay DCLKOUT to ALE	Rising	–	4	ns
		Falling	–	3	ns
4	Delay DCLKOUT to A[12:0]	–	–	8	ns
4	Delay DCLKOUT to D[31:16]	–	–	8	ns
4	Delay DCLKOUT to D[15:0]	–	1.5	8	ns
4	Delay DCLKOUT to /CS3–0	Rising	–	10	ns
		Falling	–	10	ns
4	Delay DCLKOUT to /RD	Risng	–	8	ns
		Falling	–	7	ns
4	Delay DCLKOUT to /WE	Rising	–	5	ns
		Falling	–	4	ns
4	Delay DCLKOUT to /SAS3–0	Rising	–	1.5	ns
		Falling	–	1.5	ns
4	Delay DCLKOUT to /CARDxCSx	Rising	–	9	ns
		Falling	–	8	ns
4	Delay DCLKOUT to /CARDDIR	Rising	–	12	ns
		Falling	–	11	ns
4	Delay DCLKOUT to /CARDREG	Rising	–	9	ns
		Falling	–	10	ns
4	Delay DCLKOUT to /IORD	Rising	–	10	ns
		Falling	–	9	ns
4	Delay DCLKOUT to /IOWR	Rising	–	9	ns
		Falling	–	9	ns
4	Delay DCLKOUT to /RAS0	Rising	–	6	ns
		Falling	–	6	ns
4	Delay DCLKOUT to /RAS1	Rising	1.5	8	ns
		Falling	1.5	9	ns
4	Delay DCLKOUT to DQMH/L	Rising	1.5	8	ns
		Falling	1.5	9	ns
4	Delay DCLKOUT to /DCS0	Rising	1.5	7	ns
		Falling	1.5	6	ns
4	Delay DCLKOUT to DCKE	Rising	1.5	8	ns
		Falling	1.5	8	ns
4	Delay DCLKOUT to /MCS3–0	Rising	–	10	ns
		Falling	–	10	ns
5	D[31:16] to DCLKIN Setup time	–	2	–	ns
6	D[31:16] to DCLKIN Hold time	–	1	–	ns
5	D[15:0] to DCLKIN Setup time	–	1	–	ns
6	D[15:0] to DCLKIN Hold time	–	1.5	–	ns
7	DCLKOUT to DCLKIN Board Delay time	–	0	3	ns

MEMORY INTERFACE TIMING DIAGRAMS

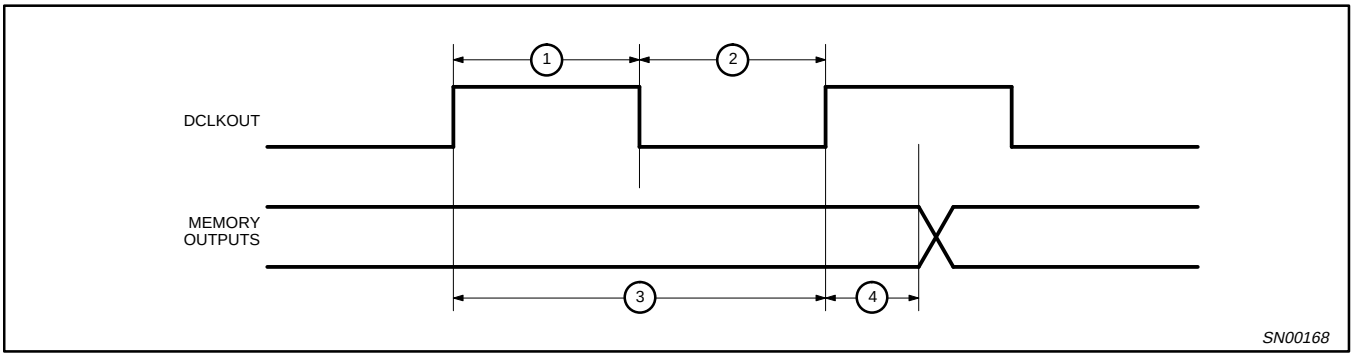


Figure 1. Memory Output and Clock Timing

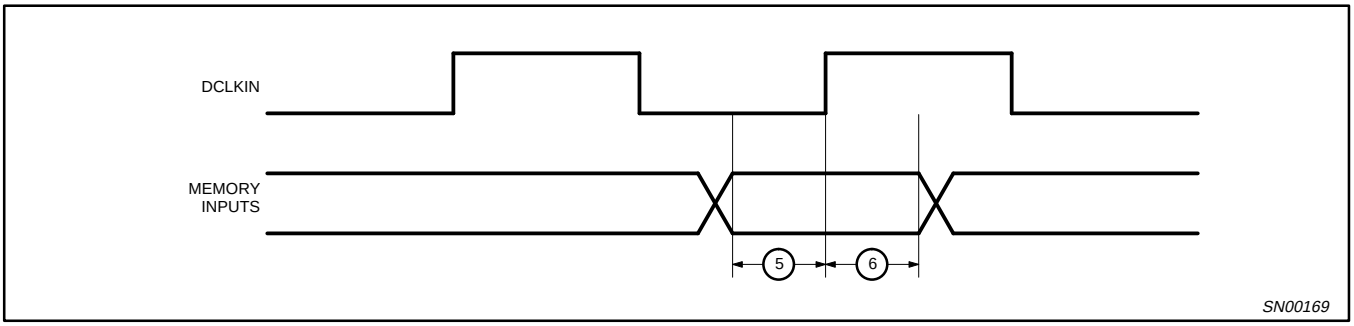


Figure 2. Memory Input Timing

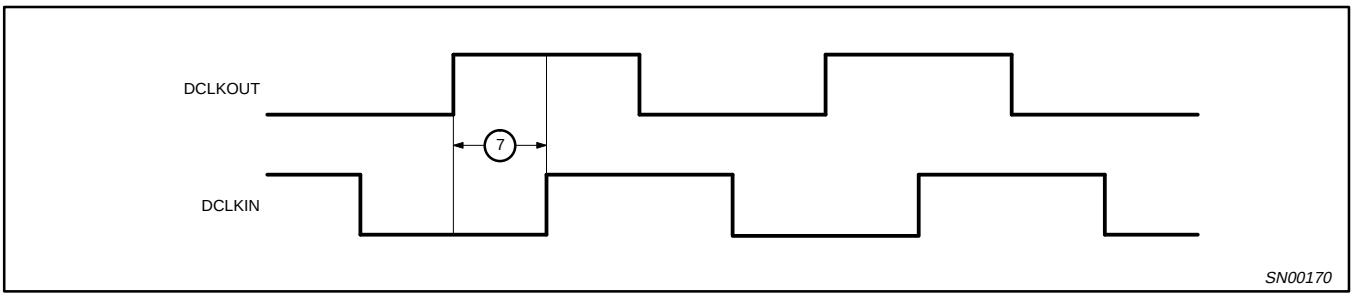


Figure 3. DCLKOUT to DCLKIN

CHI

T_{amb} = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, External Capacitance = 40pF

ITEM	PARAMETER	RISING/FALLING	LIMITS		UNIT
			MIN	MAX	
1	CHICLK high time	–	100	–	ns
2	CHICLK low time	–	100	–	ns
3	CHICLK period	–	225	–	ns
4	Delay CHICLK Rising to CHIDOUT (Master)	Rising	–	5	ns
		Falling	–	5	ns
7	Delay CHICLK Falling to CHIDOUT (Master)	Rising	–	5	ns
		Falling	–	5	ns
4	Delay CHICLK Rising to CHIFS (Master)	Rising	–	5	ns
		Falling	–	5	ns
7	Delay CHICLK Falling to CHIFS (Master)	Rising	–	5	ns
		Falling	–	5	ns
4	Delay CHICLK Rising to CHIDOUT (Slave)	Rising	–	10	ns
		Falling	–	10	ns
7	Delay CHICLK Falling to CHIDOUT (Slave)	Rising	–	10	ns
		Falling	–	10	ns
4	Delay CHICLK Rising to CHIFS (Slave)	Rising	–	10	ns
		Falling	–	10	ns
7	Delay CHICLK Falling to CHIFS (Slave)	Rising	–	10	ns
		Falling	–	10	ns
5	CHIDIN to CHICLK Rising Setup time (Master)	–	20	–	ns
6	CHIDIN to CHICLK Rising Hold time (Master)	–	20	–	ns
8	CHIDIN to CHICLK Falling Setup time (Master)	–	20	–	ns
9	CHIDIN to CHICLK Falling Hold time (Master)	–	20	–	ns
5	CHIFS to CHICLK Rising Setup time (Slave)	–	20	–	ns
6	CHIFS to CHICLK Rising Hold time (Slave)	–	20	–	ns
8	CHIFS to CHICLK Falling Setup time (Slave)	–	20	–	ns
9	CHIFS to CHICLK Falling Hold time (Slave)	–	20	–	ns
5	CHIDIN to CHICLK Rising Setup time (Slave)	–	20	–	ns
6	CHIDIN to CHICLK Rising Hold time (Slave)	–	20	–	ns
8	CHIDIN to CHICLK Falling Setup time (Slave)	–	20	–	ns
9	CHIDIN to CHICLK Falling Hold time (Slave)	–	20	–	ns

CHI TIMING DIAGRAMS

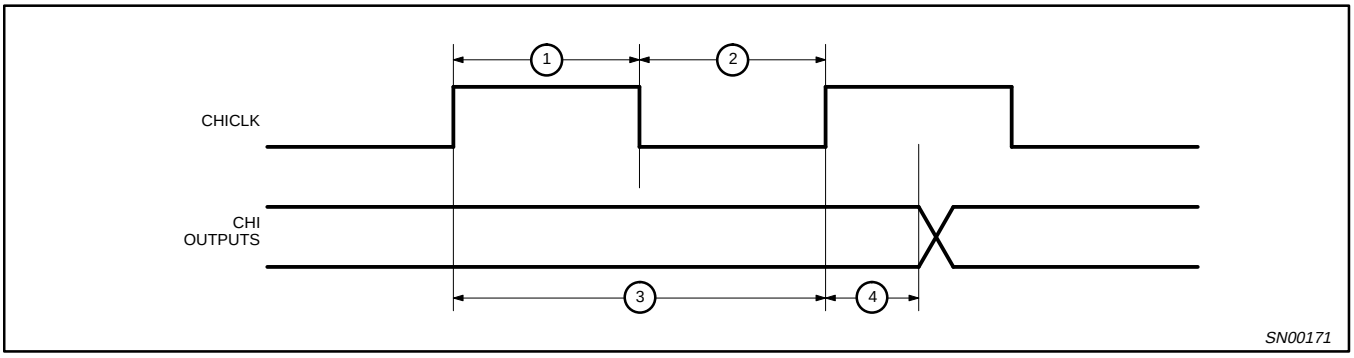


Figure 4. CHI Output and Clock Timing (CHITXEDGE = 1)

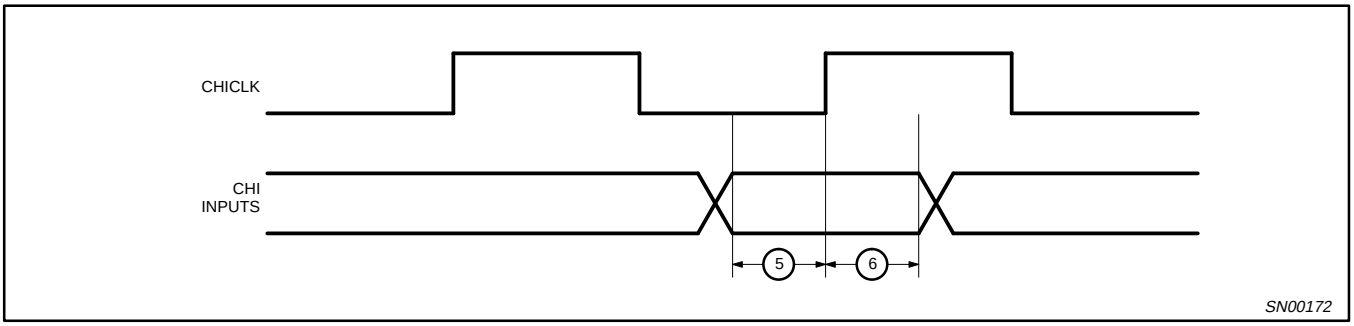


Figure 5. CHI Input Timing (CHIRXEDGE = 1)

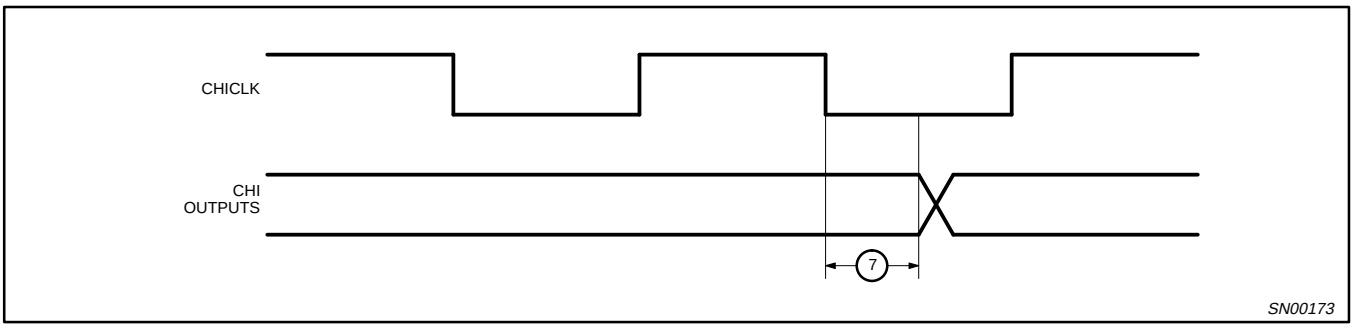


Figure 6. CHI Output and Clock Timing (CHITXEDGE = 0)

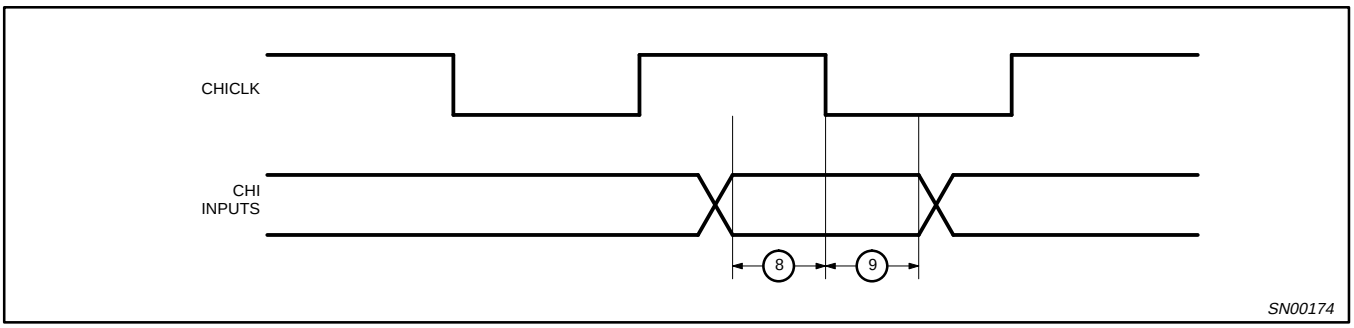


Figure 7. CHI Input Timing (CHIRXEDGE = 0)

SIB

T_{amb} = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, External Capacitance = 40pF

ITEM	PARAMETER	RISING/FALLING	LIMITS		UNIT
			MIN	MAX	
1	SIBMCLK high time	–	20	–	ns
2	SIBMCLK low time	–	20	–	ns
3	SIBMCLK period	–	50	–	ns
4	Delay SIBMCLK to SIBSCLK	Rising	–	5	ns
5	Delay SIBMCLK to SIBSCLK	Falling	–	5	ns
6	Delay SIBSCLK Rising to SIBSYNC	Rising	–	2	ns
		Falling	–	2	ns
6	Delay SIBSCLK Rising to SIBDOUT	Rising	–	2	ns
		Falling	–	2	ns
7	SIBDIN to SIBSCLK Rising Setup time	–	20	–	ns
8	SIBDIN to SIBSCLK Rising Hold time	–	0	–	ns

SIB TIMING DIAGRAMS

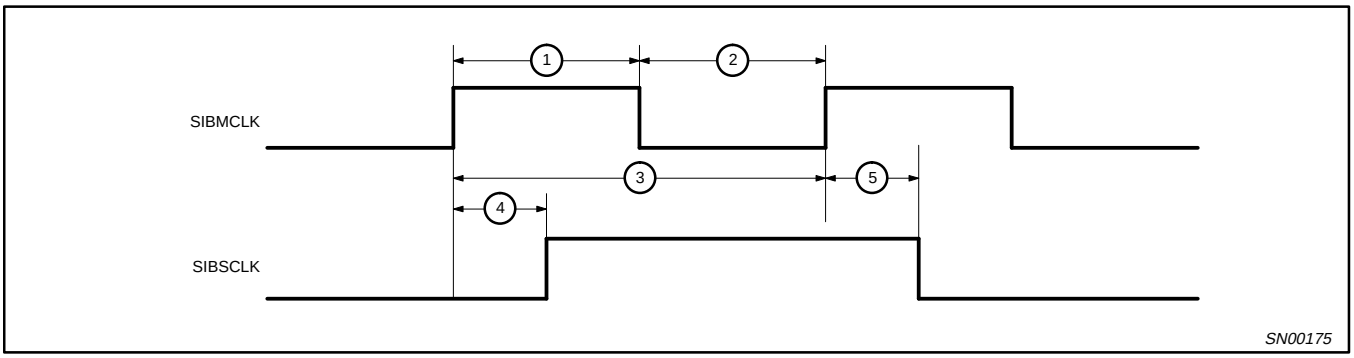


Figure 8. SIB CLK Timing

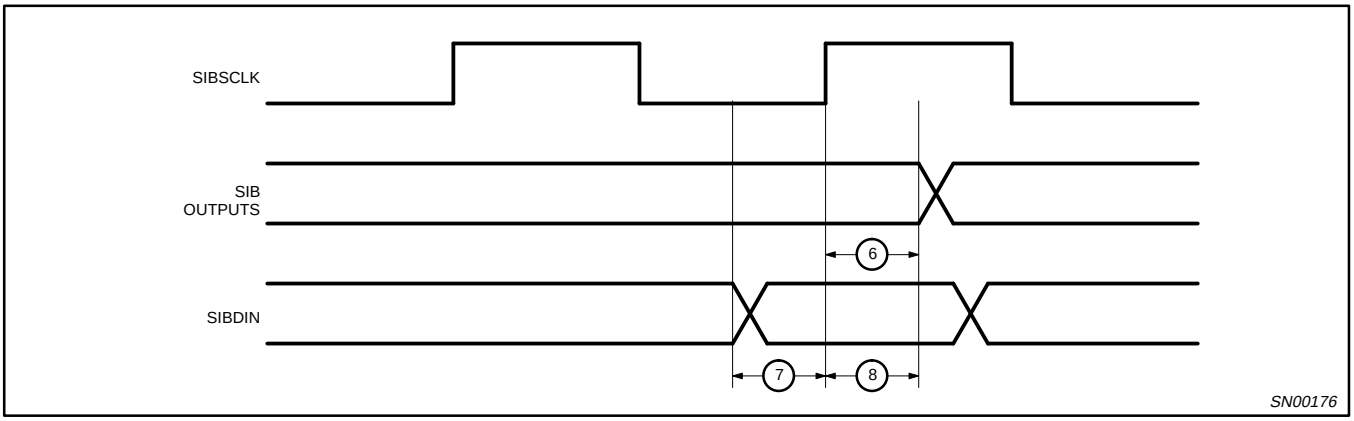


Figure 9. SIB Timing

SPI

ITEM	PARAMETER	RISING/FALLING	LIMITS		UNIT
			MIN	MAX	
1	SPIMCLK high time	–	120	–	ns
2	SPICLK low time	–	120	–	ns
3	SPICLK period	–	250	–	ns
4	Delay SPICLK Rising to SPIOUT	Rising	–		ns
4	Delay SPICLK Rising to SPIOUT	Falling	–		ns
7	Delay SPICLK Falling to SPIOUT	Rising	–		ns
7	Delay SPICLK Falling to SPIOUT	Falling	–		ns
8	SPIIN to SPICLK Rising Setup time	–	15	–	ns
9	SPIIN to SPICLK Rising Hold time	–	15	–	ns
5	SPIIN to SPICLK Falling Setup time	–	15	–	ns
6	SPIIN to SPICLK Falling Hold time	–	15	–	ns

SPI TIMING DIAGRAMS

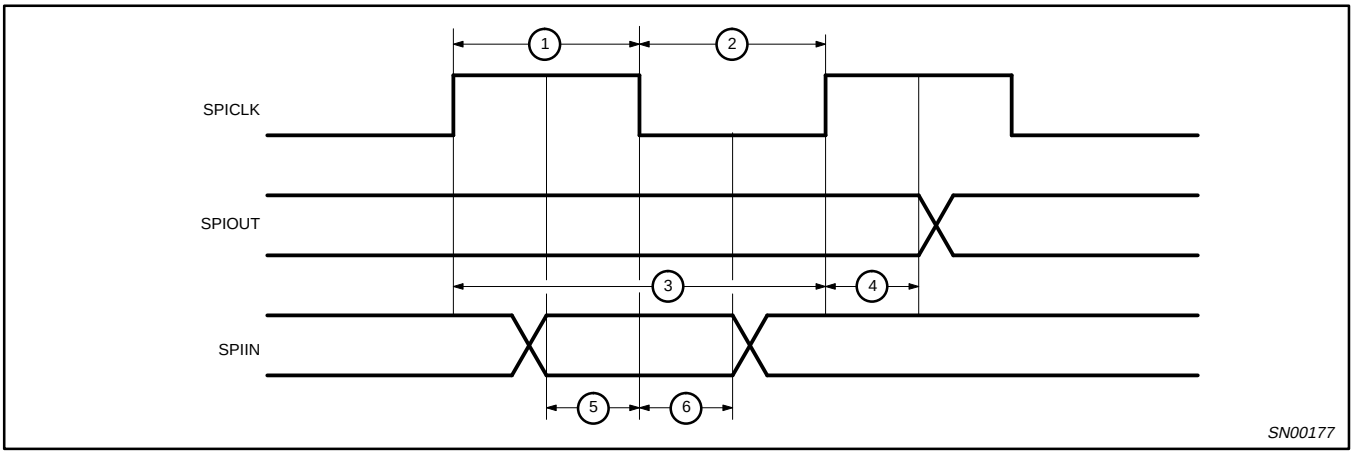


Figure 10. SPI Timing (PHAPOL = 1)

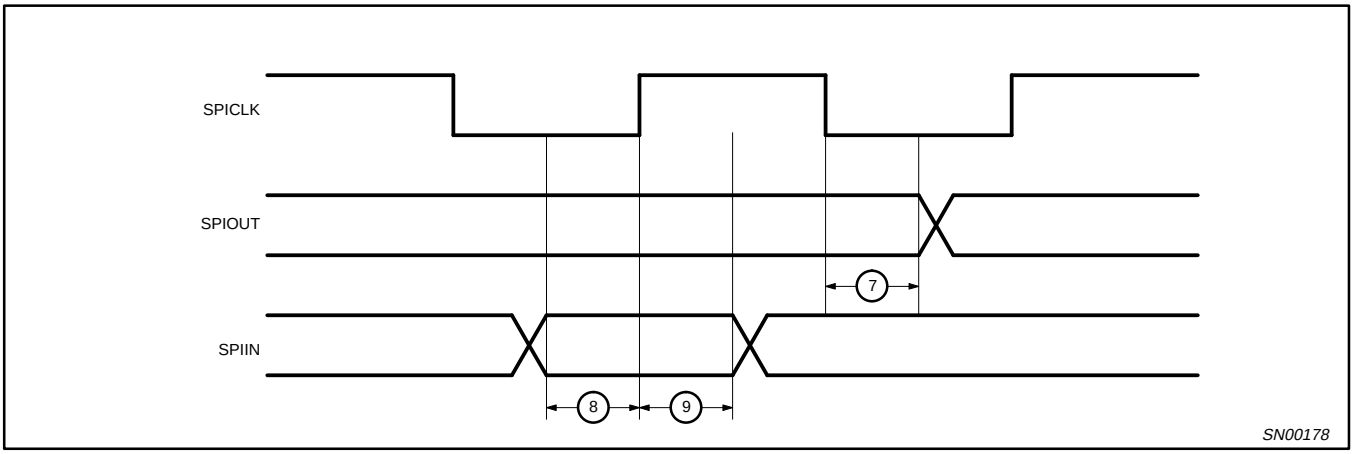


Figure 11. SPI Timing (PHAPOL = 0)

VIDEO

T_{amb} = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, External Capacitance = 40pF

ITEM	PARAMETER	RISING/FALLING	LIMITS		UNIT
			MIN	MAX	
1	LOAD Pulse width	–	100	1600	ns
2	Delay LOAD Falling to FRAME	–	100	3200	ns
3	Delay LOAD Falling to DF	–	100	3200	ns
4	Delay LOAD Falling to CP	–	100	3200	ns
5	Delay CP Rising to VDAT[3:0]	–	–	3	ns
6	VDAT to CP Rising Setup	–	15	25	ns
7	VDAT to CP Rising Hold	–	15	25	ns

NOTE:
Values shown assume a 40MHz clock for the CPU, MIN and MAX values are programmable using Video Control Registers.

VIDEO TIMING DIAGRAMS

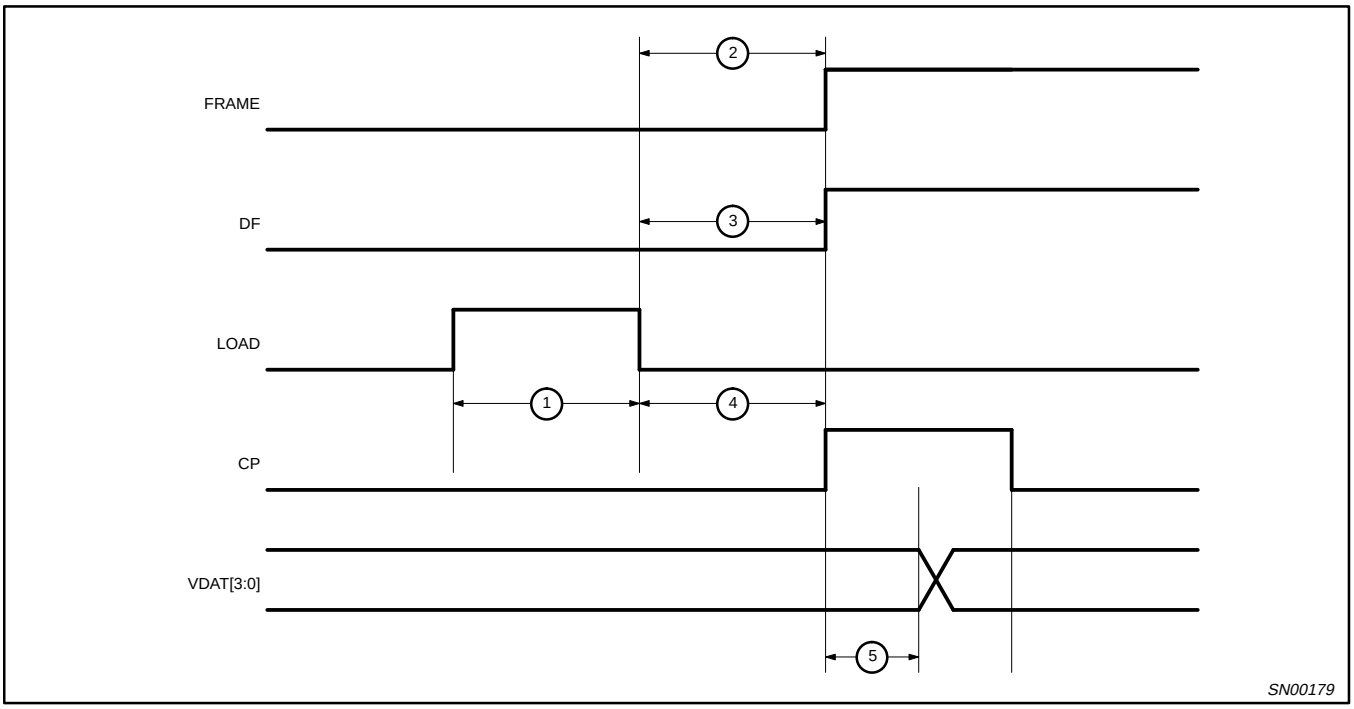


Figure 12. Video Timing, 4 Bit Non-Split LCD

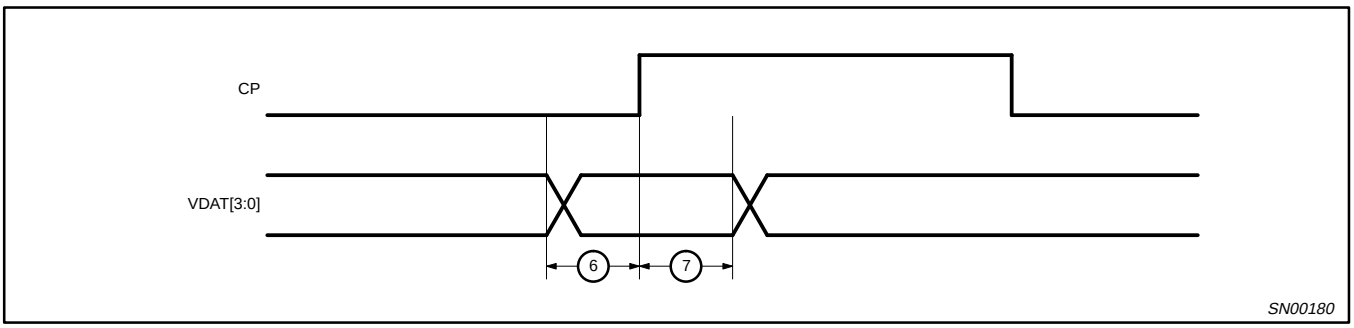


Figure 13. Video Data Timing, 4 Bit Split LCD and 8 Bit Non-Split LCD

POWER

T_{amb} = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, External Capacitance = 40pF

ITEM	PARAMETER	RISING/FALLING	LIMITS		UNIT
			MIN	MAX	
1	VSTANDBY to /PON Rising	–	50	–	ns
2	VSTANDBY to ONBUTN delay time	–	2	–	s

POWER TIMING DIAGRAM

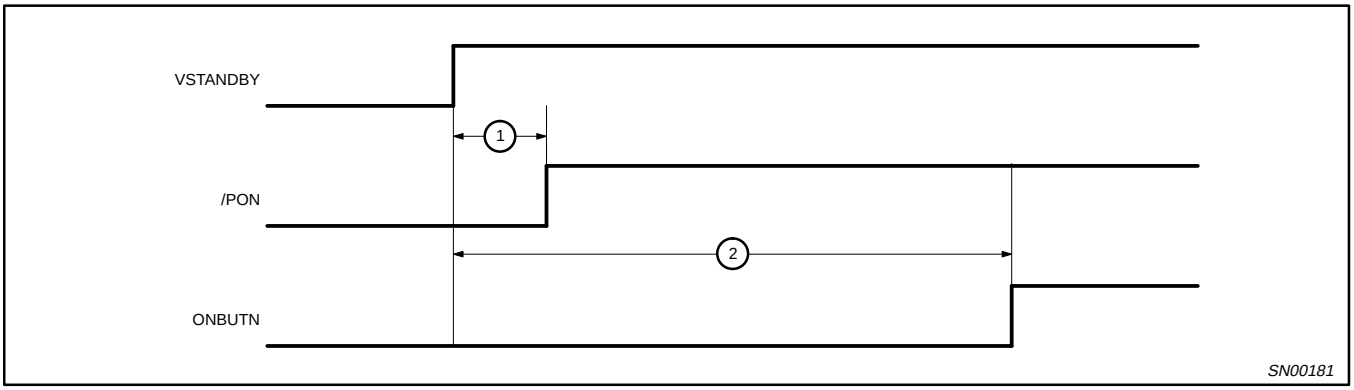


Figure 14.

CPU RESET

T_{amb} = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, External Capacitance = 40pF

ITEM	PARAMETER	RISING/FALLING	LIMITS		UNIT
			MIN	MAX	
1	/CPURES low time	–	10	–	ns

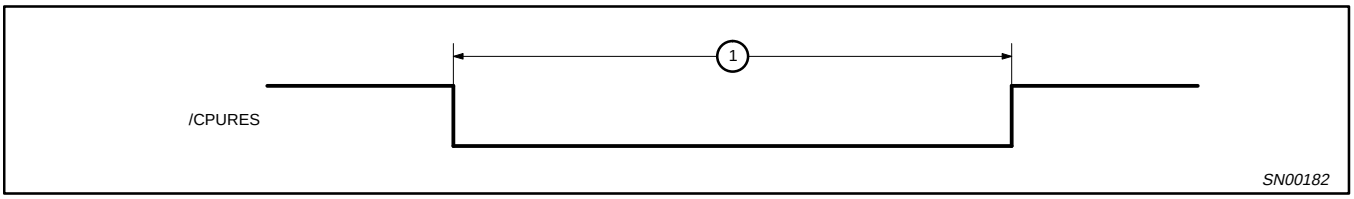
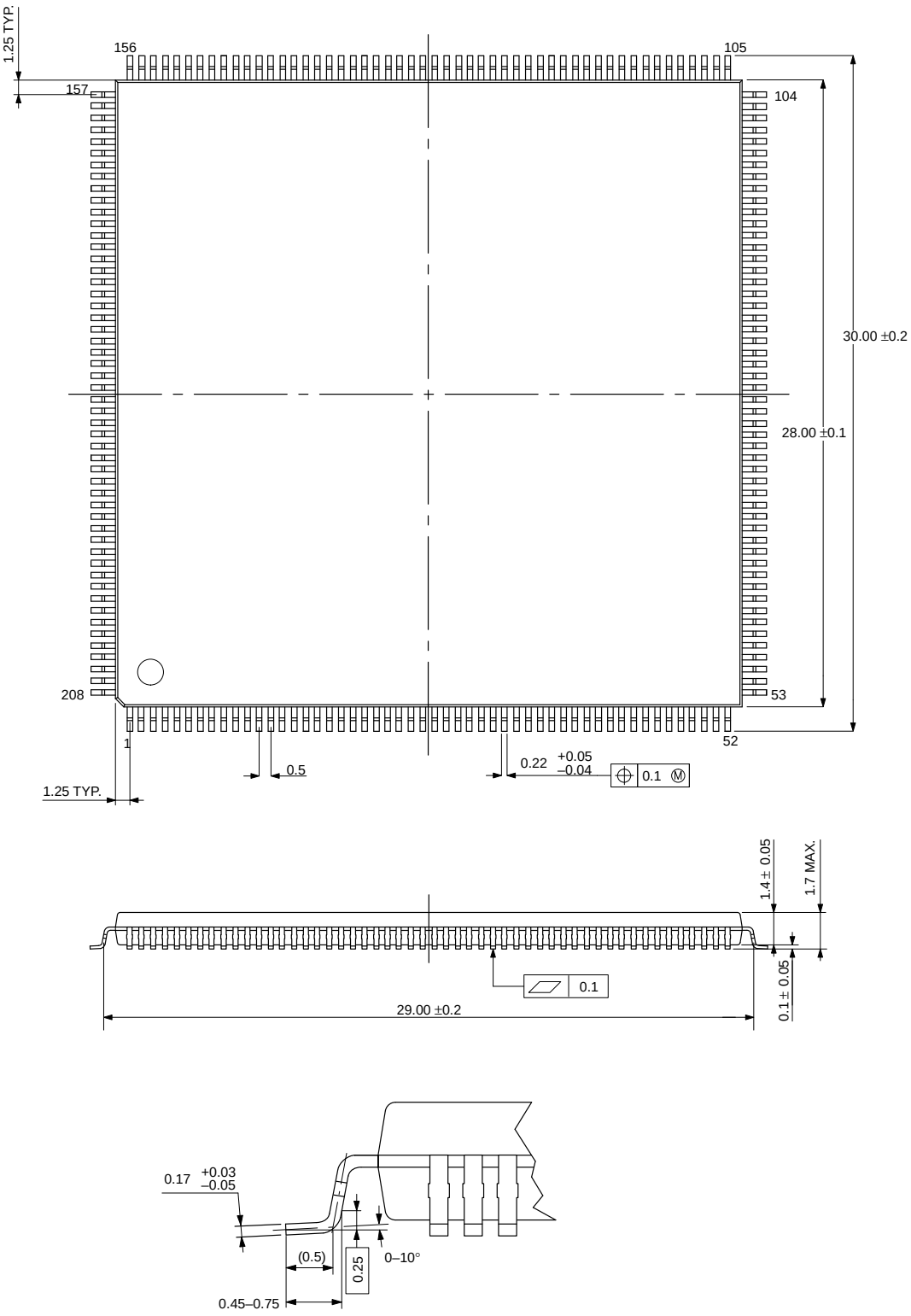


Figure 15.

LQFP208: 208-PIN PLASTIC LOW PROFILE QUAD FLAT PACKAGE



UNIT = mm
(Drawing not to scale)

Poseiden embedded processor

MIPS
PR31500

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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