HN29WT800 Series
HN29WB800 Series

1048576-word × 8-bit / 524288-word × 16-bit CMOS Flash Memory

HITACHI

ADE-203-537A(Z)
Rev. 1.0
May. 9, 1997

Description

The Hitachi HN29WT800 Series, HN29WB800 Series are 1-Mword × 8-bit/512-kword × 16-bit CMOS Flash Memory with DINOR (DIvided bitline NOR) type memory cells, that realize programming and erase capabilities with a single 3.3 V power supply. The built-in Sequence Controller allows Automatic Program/Erase without complex external control. HN29WT800 Series, HN29WB800 Series enable the low power and high performance systems such as mobile, personal computing and communication products.

Features

- On-board single power supply (V_{CC}): V_{CC} = 3.3 V ± 0.3 V
- Access time: 80/100/120 ns (max)
- Low power dissipation:
  - — I_{CC} = 30 mA (max) (Read)
  - — I_{CC} = 200 µA (max) (Standby)
  - — I_{CC} = 40 mA (max) (Program)
  - — I_{CC} = 40 mA (max) (Erase)
  - — I_{CC} = 1 µA (typ) (Deep powerdown)
- Automatic page programming:
  - — Programming time: 25 ms (typ)
  - — Program unit: 128 word
- Automatic erase:
  - — Erase time: 50 ms (typ)
  - — Erase unit: Boot block; 8-kword/16-kbyte × 1
    Parameter block; 4-kword/8-kbyte × 2
    Main block; 16-kword/32-kbyte × 1
    32-kword/64-kbyte × 15

This product is compatible with M5M29FB/T800xx by Ltd. Mitsubishi.

Hitachi semiconductor

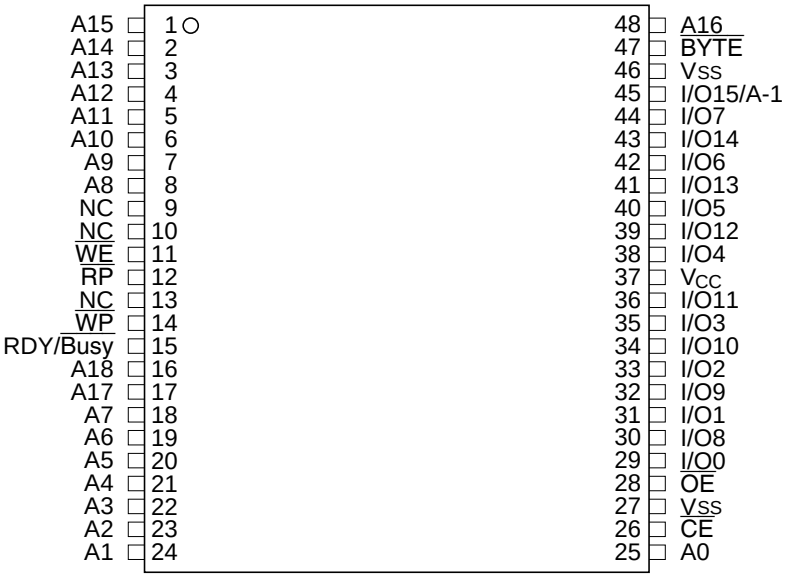
- Block boot:
  - — HN29WT800 Series: Top boot
  - — HN29WB800 Series: Bottom boot
- Program/Erase endurance
  - — 10,000 cycles
- Other functions:
  - — Software command control
  - — Selective block lock
  - — Program suspend/Resume
  - — Erase suspend/Resume
  - — Status register read
- Compatible with M5M29FB/T800xx by Ltd. Mitsubishi

Ordering Information

Type No.	Access time	Package
HN29WT800T-8	80 ns	12 × 20.0 mm² 48-pin plastic TSOP I (TFP-48D)
HN29WT800T-10	100 ns	
HN29WT800T-12	120 ns	
HN29WB800T-8	80 ns	
HN29WB800T-10	100 ns	
HN29WB800T-12	120 ns	
HN29WT800R-8	80 ns	12 × 20.0 mm² 48-pin plastic TSOP I (Reverse) (TFP-48DR)
HN29WT800R-10	100 ns	
HN29WT800R-12	120 ns	
HN29WB800R-8	80 ns	
HN29WB800R-10	100 ns	
HN29WB800R-12	120 ns	

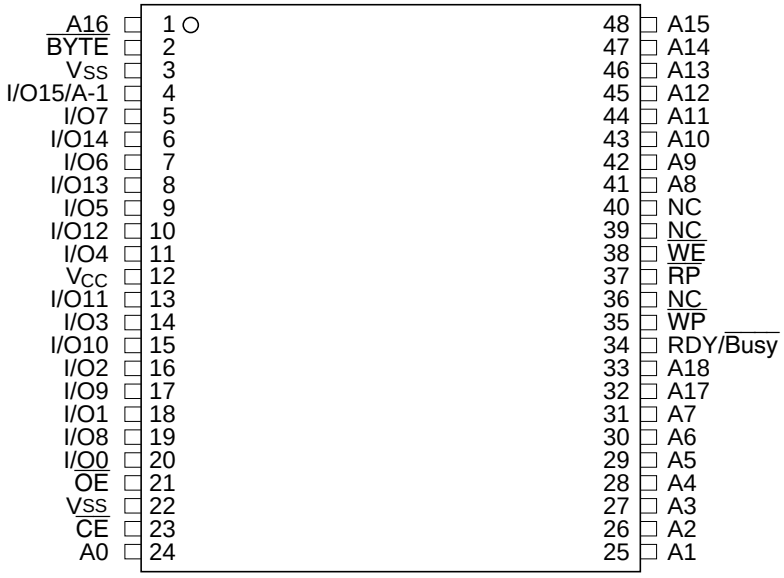
Pin Arrangement

HN29WT800T Series
HN29WB800T Series



(Top view)

HN29WT800R Series
HN29WB800R Series

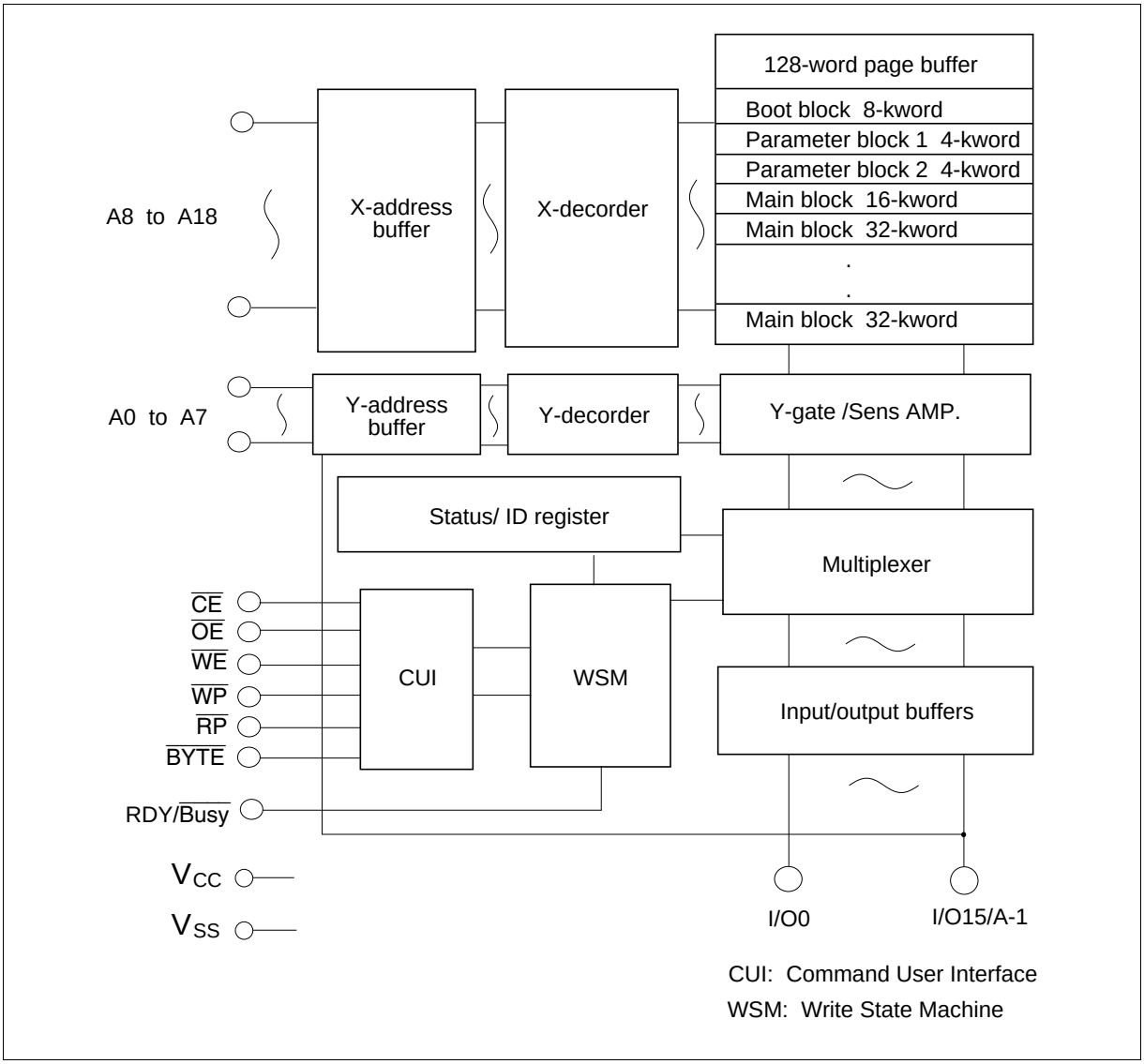


(Top view)

Pin Description

Pin name	Function
A-1 to A18	Address
I/O0 to I/O15	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{RP}$	Reset/Powerdown
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
$\overline{WP}$	Write protect
$\overline{BYTE}$	Byte enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Memory Map

HN29WT800 Series Memory Map

× 8 (Byte mode)	× 16 (Word mode)	
FC000H to FFFFFH	7E000H to 7FFFFH	8-kword boot block
FA000H to FBFFFH	7D000H to 7DFFFH	4-kword parameter block
F8000H to F9FFFH	7C000H to 7CFFFH	4-kword parameter block
F0000H to F7FFFH	78000H to 7BFFFH	16-kword main block
E0000H to EFFFFH	70000H to 77FFFH	32-kword main block
D0000H to DFFFFH	68000H to 6FFFFH	32-kword main block
C0000H to CFFFFH	60000H to 67FFFH	32-kword main block
B0000H to BFFFFH	58000H to 5FFFFH	32-kword main block
A0000H to AFFFFH	50000H to 57FFFH	32-kword main block
90000H to 9FFFFH	48000H to 4FFFFH	32-kword main block
80000H to 8FFFFH	40000H to 47FFFH	32-kword main block
70000H to 7FFFFH	38000H to 3FFFFH	32-kword main block
60000H to 6FFFFH	30000H to 37FFFH	32-kword main block
50000H to 5FFFFH	28000H to 2FFFFH	32-kword main block
40000H to 4FFFFH	20000H to 27FFFH	32-kword main block
30000H to 3FFFFH	18000H to 1FFFFH	32-kword main block
20000H to 2FFFFH	10000H to 17FFFH	32-kword main block
10000H to 1FFFFH	08000H to 0FFFFH	32-kword main block
00000H to 0FFFFH	00000H to 07FFFH	32-kword main block
A-1 to A18 (Byte mode)	A0 to A18 (Word mode)	

HN29WB800 Series Memory Map

× 8 (Byte mode)	× 16 (Word mode)	
F0000H to FFFFFH	78000H to 7FFFFH	32-kword main block
E0000H to EFFFFH	70000H to 77FFFH	32-kword main block
D0000H to DFFFFH	68000H to 6FFFFH	32-kword main block
C0000H to CFFFFH	60000H to 67FFFH	32-kword main block
B0000H to BFFFFH	58000H to 5FFFFH	32-kword main block
A0000H to AFFFFH	50000H to 57FFFH	32-kword main block
90000H to 9FFFFH	48000H to 4FFFFH	32-kword main block
80000H to 8FFFFH	40000H to 47FFFH	32-kword main block
70000H to 7FFFFH	38000H to 3FFFFH	32-kword main block
60000H to 6FFFFH	30000H to 37FFFH	32-kword main block
50000H to 5FFFFH	28000H to 2FFFFH	32-kword main block
40000H to 4FFFFH	20000H to 27FFFH	32-kword main block
30000H to 3FFFFH	18000H to 1FFFFH	32-kword main block
20000H to 2FFFFH	10000H to 17FFFH	32-kword main block
10000H to 1FFFFH	08000H to 0FFFFH	32-kword main block
08000H to 0FFFFH	04000H to 07FFFH	16-kword main block
06000H to 07FFFH	03000H to 03FFFH	4-kword parameter block
04000H to 05FFFH	02000H to 02FFFH	4-kword parameter block
00000H to 03FFFH	00000H to 01FFFH	8-kword boot block
A-1 to A18 (Byte mode)	A0 to A18 (Word mode)	

Top Boot Block Address Map*[1]

	Address							Size	
Block	A18	A17	A16	A15	A14	A13	A12	× 8 (Byte mode)	× 16 (Word mode)
Block18	1	1	1	1	1	1	×	16-kbyte	8-kword
Block17	1	1	1	1	1	0	1	8-kbyte	4-kword
Block16	1	1	1	1	1	0	0	8-kbyte	4-kword
Block15	1	1	1	1	0	×	×	32-kbyte	16-kword
Block14	1	1	1	0	×	×	×	64-kbyte	32-kword
Block13	1	1	0	1	×	×	×	64-kbyte	32-kword
Block12	1	1	0	0	×	×	×	64-kbyte	32-kword
Block11	1	0	1	1	×	×	×	64-kbyte	32-kword
Block10	1	0	1	0	×	×	×	64-kbyte	32-kword
Block9	1	0	0	1	×	×	×	64-kbyte	32-kword
Block8	1	0	0	0	×	×	×	64-kbyte	32-kword
Block7	0	1	1	1	×	×	×	64-kbyte	32-kword
Block6	0	1	1	0	×	×	×	64-kbyte	32-kword
Block5	0	1	0	1	×	×	×	64-kbyte	32-kword
Block4	0	1	0	0	×	×	×	64-kbyte	32-kword
Block3	0	0	1	1	×	×	×	64-kbyte	32-kword
Block2	0	0	1	0	×	×	×	64-kbyte	32-kword
Block1	0	0	0	1	×	×	×	64-kbyte	32-kword
Block0	0	0	0	0	×	×	×	64-kbyte	32-kword

Note: 1. × can be V_{IH}. Address except block address must be V_{IH}.

Bottom Boot Block Address Map*[1]

	Address							Size	
Block	A18	A17	A16	A15	A14	A13	A12	× 8 (Byte mode)	× 16 (Word mode)
Block18	1	1	1	1	×	×	×	64-kbyte	32-kword
Block17	1	1	1	0	×	×	×	64-kbyte	32-kword
Block16	1	1	0	1	×	×	×	64-kbyte	32-kword
Block15	1	1	0	0	×	×	×	64-kbyte	32-kword
Block14	1	0	1	1	×	×	×	64-kbyte	32-kword
Block13	1	0	1	0	×	×	×	64-kbyte	32-kword
Block12	1	0	0	1	×	×	×	64-kbyte	32-kword
Block11	1	0	0	0	×	×	×	64-kbyte	32-kword
Block10	0	1	1	1	×	×	×	64-kbyte	32-kword
Block9	0	1	1	0	×	×	×	64-kbyte	32-kword
Block8	0	1	0	1	×	×	×	64-kbyte	32-kword
Block7	0	1	0	0	×	×	×	64-kbyte	32-kword
Block6	0	0	1	1	×	×	×	64-kbyte	32-kword
Block5	0	0	1	0	×	×	×	64-kbyte	32-kword
Block4	0	0	0	1	×	×	×	64-kbyte	32-kword
Block3	0	0	0	0	1	×	×	32-kbyte	16-kword
Block2	0	0	0	0	0	1	1	8-kbyte	4-kword
Block1	0	0	0	0	0	1	0	8-kbyte	4-kword
Block0	0	0	0	0	0	0	×	16-kbyte	8-kword

Note: 1. × can be V_{IH}. Address except block address must be V_{IH}.

Mode Selection

Word Mode ($\overline{BYTE} = V_{IH}$)

Mode	Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	RDY/$\overline{Busy}$	I/O0 to I/O15
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH} (High-Z)	Dout
	Status register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	×*5	Status Register Data
	Lock bit status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	×	Lock bit data (I/O6)
	Identifier (Maker)*1, *2	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH} (High-Z)	07H
	Identifier (Device)*1, *3	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH} (High-Z)	85H / 86H*6
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	×	High-Z
Standby		V_{IH}	×*5	×*5	V_{IH}	×	High-Z
Command write*4	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	Command/Data in
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	Command
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	Command
Deep powerdown		×	×	×	V_{IL}	V_{OH} (High-Z)	High-Z

Notes: 1. The command programming mode is used to output the identifier code. Refer to the table of Software Command Definition.

2. A0 = V_{IL}
3. A0 = V_{IH}
4. Refer to the table of Software Command Definition. Programming and erase operation begins after mode setting by command input.
5. × can be V_{IL} or V_{IH} for control pins, and V_{OL} or V_{OH} (High-Z) for RDY/$\overline{Busy}$ pin. The RDY/$\overline{Busy}$ is an open drain output pin and indicates status of the internal WSM. When low, it indicates the WSM is Busy performing an operation. A pull-up resistor of 10 k to 100 k Ω is required to allow the RDY/$\overline{Busy}$ signal to transition high indicating a Ready WSM condition.
6. 85H: HN29WT800 Series, 86H: HN29WB800 Series.

$\overline{\text{BYTE}}$ Mode ($\overline{\text{BYTE}} = V_{IL}$)

Mode	Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	RDY/$\overline{Busy}$	I/O0 to I/O7
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH} (High-Z)	Dout
	Status register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	×*5	Status Register Data
	Lock bit status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	×	Lock bit data (I/O6)
	Identifier (Maker)*1, *2	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH} (High-Z)	07H
	Identifier (Device)*1, *3	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH} (High-Z)	85H / 86H*6
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	×	High-Z
Standby		V_{IH}	×*5	×*5	V_{IH}	×	High-Z
Command write*4	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	Command/Data in
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	Command
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	Command
Deep powerdown		×	×	×	V_{IL}	V_{OH} (High-Z)	High-Z

Notes: 1. The command programming mode is used to output the identifier code. Refer to the table of Software Command Definition.

2. A0 = V_{IL}
3. A0 = V_{IH}
4. Refer to the table of Software Command Definition. Programming and erase operation begins after mode setting by command input.
5. × can be V_{IL} or V_{IH} for control pins, and V_{OL} or V_{OH} (High-Z) for RDY/$\overline{Busy}$ pin. The RDY/$\overline{Busy}$ is an open drain output pin and indicates status of the internal WSM. When low, it indicates the WSM is Busy performing an operation. A pull-up resistor of 10 k to 100 k Ω is required to allow the RDY/$\overline{Busy}$ signal to transition high indicating a Ready WSM condition.
6. 85H: HN29WT800 Series, 86H: HN29WB800 Series.

Software Command Definition

	First bus cycle			Second bus cycle			Third bus cycle		
Command	Operation mode	Address	Data (I/O7 to I/O0)*1	Operation mode	Address	Data (I/O7 to I/O0)	Operation mode	Address	Data (I/O7 to I/O0)
Read array (memory)	Write	×	FFH						
Read identifier codes	Write	×	90H	Read	IA*2	ID*2			
Read status register	Write	×	70H	Read	×	SRD*3			
Clear status register	Write	×	50H						
Page program*5	Write	×	41H	Write	WA0*4	WD0*4	Write	WA1	WD1
Block erase	Write	×	20H	Write	BA*6	D0H			
Suspend	Write	×	B0H						
Resume	Write	×	D0H						
Read lock bit status	Write	×	71H	Read	BA	I/O6*7			
Lock bit program/confirm	Write	×	77H	Write	BA	D0H			
Erase all unlocked blocks	Write	×	A7H	Write	×	D0H			

Notes: 1. In the word mode, upper byte data (I/O8 to I/O15) is ignored.

2. IA = Identifier address, A0 = V_{IL} (Manufacture code), A0 = V_{IH} (Device code), ID = ID code, $\overline{BYTE}$ = V_{IL}: A-1, A1 to A18 = V_{IL}, $\overline{BYTE}$ = V_{IH}: A1 to A18 = V_{IL}.
3. SRD = Status register data
4. WA = Write address, WD = Write data
5. $\overline{BYTE}$ = V_{IL}: Write address and write data must be provided sequentially from 00H to FFH for A-1 to A6. Page size is 256 byte (256-byte × 8-bit).
   $\overline{BYTE}$ = V_{IH}: Write address and write data must be provided sequentially from 00H to 7FH for A0 to A6. Page size is 128 word (128-word × 16-bit).
6. BA = Block address (A12 to A18), (Addresses except block address must be V_{IH})
7. I/O6 provides block lock status, I/O6 = 1: Block unlocked, I/O6 = 0: Block locked.

Block Locking

$\overline{RP}$	$\overline{WP}$	Lock bit (internally)	Write protection provided
V_{IL}	×	×	All blocks locked (Deep powerdown mode)
V_{HH}	×	×	All blocks unlocked
V_{IH}	V_{IL}	0	Blocks locked (Depend on lock bit data)
V_{IH}	V_{IL}	1	Blocks unlocked (Depend on lock bit data)
V_{IH}	V_{IH}	×	All blocks unlocked

Note: I/O6 provided lock status of each block after writing the Read lock status command (71H). $\overline{WP}$ pin must not be switched during performing Read/Write operations or WSM busy (WSMS = 0).

Status Register Data (SRD)

Symbol	Function	Definition	
SR. 7 (I/O7)	Write state machine status	1 = Ready	0 = Busy
SR. 6 (I/O6)	Suspend status	1 = Suspend	0 = Operation in progress/completed
SR. 5 (I/O5)	Erase status	1 = Error	0 = Successful
SR. 4 (I/O4)	Program status	1 = Error	0 = Successful
SR. 3 (I/O3)	Block status after program	1 = Error	0 = Successful
SR. 2 (I/O2)	Reserved	The function and the definition for these bits are to be determined. These bits should be masked out when the status register is polled.	
SR. 1 (I/O1)	Reserved		
SR. 0 (I/O0)	Reserved		

Note: The RDY/$\overline{Busy}$ is an open dran output pin and indicates status of the internal WSM. When low, it indicates that the WSM is $\overline{Busy}$ performing an operation. A pull-up resistor of 10k Ω to 100k Ω is required to allow the RDY/$\overline{Busy}$ signal to transition high indicating a Ready WSM condition.

I/O3 indicates the block status after the page programming. When I/O3 is High, the page has the over-programmed cell. If over-program occures, the device is block failed. However, if I/O3 is High, please try the block erase to the block. The block may revive.

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of Flash Memory. By this mode, the device will be automatically matched its own corresponding erase and programming algorithm.

HN29WT800 Series, HN29WB800 Series Identifier Code

Pins	A0	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex. data
Manufacturer code	0	0	0	0	0	0	1	1	1	07H
Device code (T series)	1	1	0	0	0	0	1	0	1	85H
Device code (B series)	1	1	0	0	0	0	1	1	0	86H

Notes: 1. Device identifier code can be read out by using the read identified codes command.
2. In the word mode, the same data as I/O7 to I/O0 is read out from I/O15 to I/O8.
3. A9 = V_{HH} mode. A9 = 11.5 V to 13.0 V. Set A9 to V_{HH} min 200 ns before falling edge of $\overline{CE}$ in ready status. Min 200 ns after return to V_{HH}, device can't be accessed. A1 to A8, A10 to A18, $\overline{CE}$, $\overline{OE}$, = V_{IL}, $\overline{WE}$ = V_{IH}, I/O15/A-1 = V_{IL} ($\overline{BYTE}$ = L).

Operations of the HN29WT800 Series, HN29WB800 Series

The HN29WT800 Series, HN29WB800 Series include on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation. A Deep Powerdown mode is enabled when the $\overline{RP}$ pin is at V_{SS} minimizing power consumption.

Read: The HN29WT800 Series, HN29WB800 Series have three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the HN29WT800 Series, HN29WB800 Series automatically reset to read array mode. In the read array mode, low level input to $\overline{CE}$ and $\overline{OE}$, high level input to $\overline{WE}$ and $\overline{RP}$, and address signals to the address inputs (A0 to A18) output the data of the addressed location to the data input/output (I/O0 to I/O15).

Write: Writes to the CUI enable reading of memory array data, device identifiers and reading and clearing of the Status Register, they also enable block erase and program. The CUI is written by bringing $\overline{WE}$ to low level, while $\overline{CE}$ is at low level and $\overline{OE}$ is at high level. Addresses and data are latched on the earlier rising edge of $\overline{WE}$ and $\overline{CE}$. Standard micro-processor write timings are used.

Output Disable: When $\overline{OE}$ is at V_{IH}, output from the device is disabled. Data input/output are in a high impedance (High-Z) state.

Standby: When $\overline{CE}$ is at V_{IH}, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high impedance (High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Deep Powerdown: When $\overline{RP}$ is at V_{IL}, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high impedance (High-Z) state. After return from powerdown, the CUI is reset to Read Array and the Status Register is cleared to value 80H. During block erase or program modes, $\overline{RP}$ low will abort either operation. Memory array data of the block being altered become invalid.

Functional Description

The device operations are selected by writing specific software command into the CUI.

Read Array Command (FFH): The device is in read array mode on initial device power up and after exit from deep power down, or by writing FFH to the CUI. The device remains in Read Array mode until the other commands are written.

Read Device Identifier Command (90H): Though PROM programmers can normally read device identifier codes by raising A9 to high voltage, multiplexing high voltage onto address lines is not desired for micro-processor system. It is an other means to read device identifier codes that Read Device Identifier Code Command (90H) is written to the command latch. Following the write of the Read Device Identifier command of 90H, the manufacturer code and the device code can be read from addresses 00000H and 00001H, respectively.

Read Status Register Command (70H): The Status Register is read after writing the read status register command of 70H to the CUI. The contents of Status Register are latched on the later falling edge of $\overline{OE}$ or $\overline{CE}$. So $\overline{CE}$ or $\overline{OE}$ must be toggled every status read.

Clear Status Register Command (50H): The Erase Status and Program Status bits are set to High by the Write State Machine and can be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase/Confirm Command (20H/D0H): Automated block erase is initiated by writing the Block Erase of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Suspend/Resume Command (B0H/D0H): Writing the suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The device continues to output status register data when read, after the suspend command is written to it. Polling the WSM status and suspend status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the read array command to the CUI enables reading data from blocks other than that which is suspended. When the resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

Page Program Command (41H): Page program allows fast programming of 128-word of data. Writing of 41H initiates the page program operation. From 2nd cycle to 129th cycle write data must be serially inputted. Address A6 to A0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation. Basically re-program must not be done on a page which has already programmed.

Data Protection: The HN29WT800 Series, HN29WB800 Series provide selective block locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the HN29WT800 Series, HN29WB800 Series have a master write protect pin ($\overline{WP}$) which prevents any modifications to memory blocks whose lock-bits are set to Low, when $\overline{WP}$ is low. When $\overline{WP}$ is high or $\overline{RP}$ is V_{HH}, all blocks can be programmed or erased regardless of the state of lock-bits, and the lock-bits are cleared to High by erase.

Power Supply Voltage: A delay time of 2 µs is required before any device operation is initiated. The delay time is measured from the time V_{CC} reaches V_{CC} min (3.0 V). During powerup, $\overline{RP}$ = V_{SS} is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
V_{CC} voltage	V_{CC}	–0.2 to +4.6	V	1
All input and output voltages except V_{CC}, A9, $\overline{RP}$	Vin, Vout	–0.6 to +4.6	V	1, 2
A9, $\overline{RP}$ supply voltage	V_{HH}, V_{ID}	–0.6 to +14.0	V	1, 2
Operating temperature range	Topr	0 to +70	˚C	
Storage temperature range	Tstg	–65 to +125	˚C	
Storage temperature under bias	Tbias	–10 to +80	˚C	

Notes: 1. Relative to V_{SS}.

2. Minimum DC voltage is –0.5 V on input/output pins. During transition, this level may undershoot to –2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins are V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} +1.5 V for periods < 20 ns.

Capacitance (Ta = 25˚C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

DC Characteristics (V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	–1	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	–10	—	10	µA	Vout = V_{SS} to V_{CC}
Standby V_{CC} current	I_{SB1}	—	50	200	µA	Vin = V_{IH}/V_{IL}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}
	I_{SB2}	—	1	5	µA	Vin = V_{SS} or V_{CC}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{CC} ± 0.3 V
Deep powerdown V_{CC} current	I_{SB3}	—	5	15	µA	Vin = V_{IH}/V_{IL}, $\overline{RP}$ = V_{IL}
	I_{SB4}	—	1	5	µA	Vin = V_{SS} or V_{CC}, $\overline{RP}$ = V_{SS} ± 0.3 V
Read V_{CC} current	I_{CC1}	—	7	30	mA	Vin = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{RP}$ = $\overline{OE}$ = V_{IH}, f = 10 MHz, Iout = 0 mA
Write V_{CC} current	I_{CC2}	—	—	30	mA	Vin = V_{IH}/V_{IL}, $\overline{CE}$ = $\overline{WE}$ = V_{IL}, $\overline{RP}$ = $\overline{OE}$ = V_{IH}
Programming V_{CC} current	I_{CC3}	—	—	40	mA	Vin = V_{IH}/V_{IL}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}
Erasing V_{CC} current	I_{CC4}	—	—	40	mA	Vin = V_{IH}/V_{IL}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}
Suspend V_{CC} current	I_{CC5}	—	—	200	µA	Vin = V_{IH}/V_{IL}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}
$\overline{RP}$ all block unlocked current	$I_{\overline{RP}}$	—	—	100	µA	$\overline{RP}$ = V_{HH} max
A9 intelligent identifier current	I_{ID}	—	—	100	µA	A9 = V_{ID} max
A9 intelligent identifier voltage	V_{ID}	11.4	12.0	12.6	V	
$\overline{RP}$ unlocked voltage	V_{HH}	11.4	12.0	12.6	V	
Input voltage	V_{IL}	–0.5	—	0.8	V	
	V_{IH}	2.0	—	V_{CC} + 0.5	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 5.8 mA
	V_{OH1}	0.85 × V_{CC}	—	—	V	I_{OH} = –2.5 mA
	V_{OH2}	V_{CC} - 0.4	—	—	V	I_{OH} = –100 µA
Low V_{CC} lock-out voltage*[2]	V_{LKO}	1.2	—	—	V	

Notes: 1. All currents are RMS unless otherwise noted. Typical values at V_{CC} = 3.3 V, Ta = 25°C.

2. To protect initiation of write cycle during V_{CC} powerup/powerdown, a write cycle is locked out for V_{CC} less than V_{LKO}. If V_{CC} is less than V_{LKO} Write State Machine is reset to read mode. When the Wirte State Machine is in Busy state, if V_{CC} is less than V_{LKO}, the alternation of memory contents may occur.

AC Characteristics (V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to +70˚C)

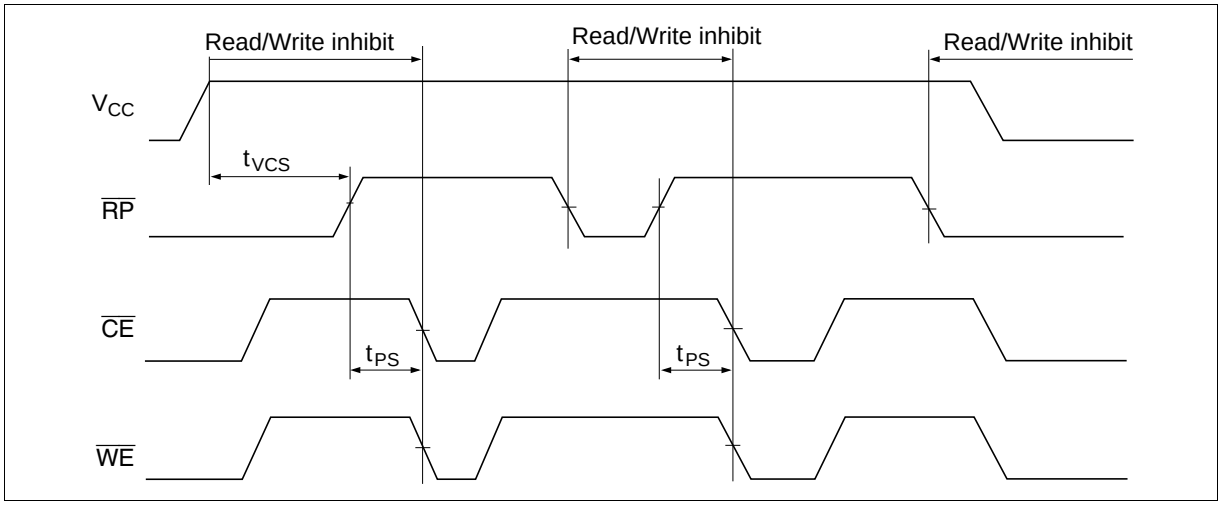
Test Conditions

- Input pulse levels: V_{IL} = 0 V, V_{IH} = 3.0 V
- Input rise and fall time: ≤ 10 ns (HN29WT/WB800-10/12 Series)
- : ≤ 5 ns (HN29WT/WB800-8 Series)
- Output load: 1 TTL gate +100 pF (Including scope and jig.) (HN29WT/WB800-10/12 Series)
- : 1 TTL gate +30 pF (Including scope and jig.) (HN29WT/WB800-8 Series)
- Reference levels for measuring timing: 1.5 V

V_{CC} Powerup/Powerdown Timing

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RP}$ = V_{IH} setup time from V_{CC} min	t_{VCS}	2	—	—	µs

Note: During powerup/powerdown, by the noise pulses on control pins, the device has possibility of accidental erasure or programming. The device must be protected against initiation of write cycle for memory contents during powerup/powerdown. The delay time of min 2 µs is always required before read operation or write operation is initiated from the time V_{CC} reaches V_{CC} min during powerup/powerdown. By holding $\overline{RP}$ V_{IL}, the contents of memory is protected during V_{CC} powerup/powerdown. During powerup, $\overline{RP}$ must be held V_{IL} for min 2 µs from the time V_{CC} reaches V_{CC} min. During powerdown, $\overline{RP}$ must be held V_{IL} until V_{CC} reaches V_{SS}. $\overline{RP}$ doesn't have latch mode, so $\overline{RP}$ must be held V_{IH} during read operation or erase/program operation.



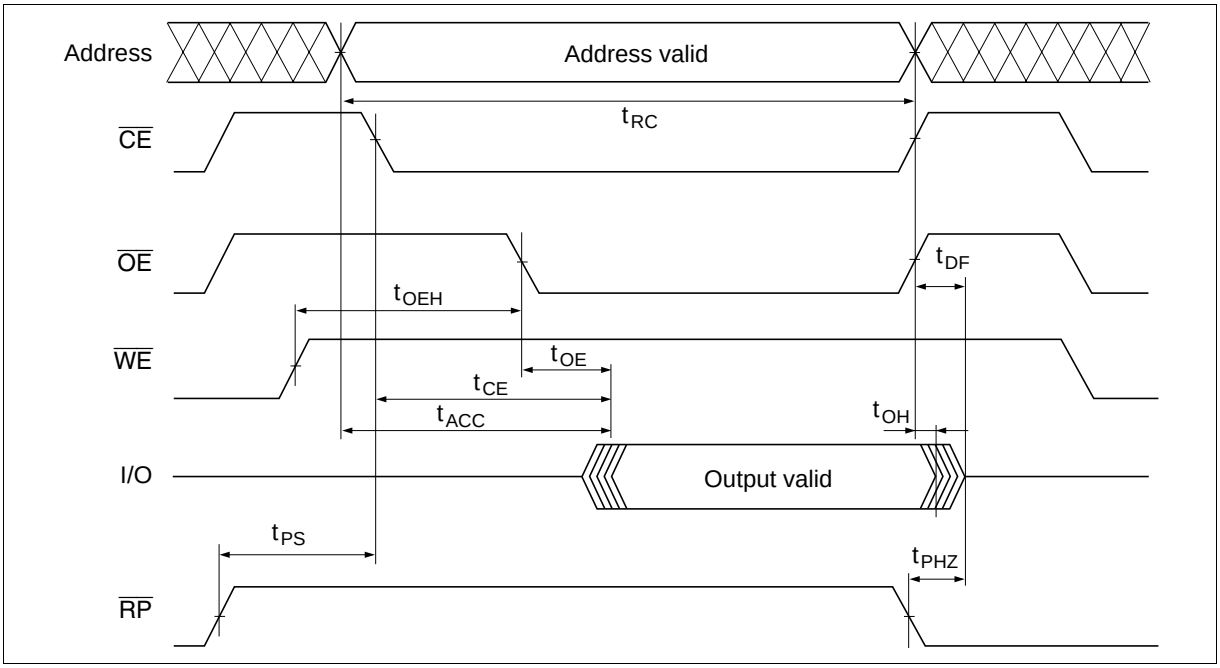
Read Operation

		HN29WT800/HN29WB800						
		-8		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	80	—	100	—	120	—	ns
Address to output delay	t_{ACC}	—	80	—	100	—	120	ns
$\overline{CE}$ to output delay	t_{CE}	—	80	—	100	—	120	ns
$\overline{OE}$ to output delay	t_{OE}	—	40	—	50	—	60	ns
$\overline{CE}$ or $\overline{OE}$ high to output float *[1]	t_{DF}	—	25	—	25	—	30	ns
Address to output hold	t_{OH}	0	—	0	—	0	—	ns
$\overline{OE}$ hold from $\overline{WE}$ high Status register read in busy	t_{OEH}	80	—	100	—	120	—	ns
$\overline{OE}$ hold from $\overline{WE}$ high Other read	t_{OEH}	0	—	0	—	0	—	ns
$\overline{RP}$ recovery time before read	t_{PS}	500	—	500	—	500	—	ns
$\overline{RP}$ low to output High-Z	t_{PHZ}	—	150	—	150	—	300	ns
$\overline{CE}$ low to $\overline{BYTE}$ high or low	t_{BCD}	—	5	—	5	—	5	ns
Address to $\overline{BYTE}$ high or low	t_{BAD}	—	5	—	5	—	5	ns
$\overline{BYTE}$ to output delay	t_{BYTE}	—	80	—	100	—	120	ns
$\overline{BYTE}$ low to output High-Z	t_{BHZ}	—	25	—	25	—	30	ns

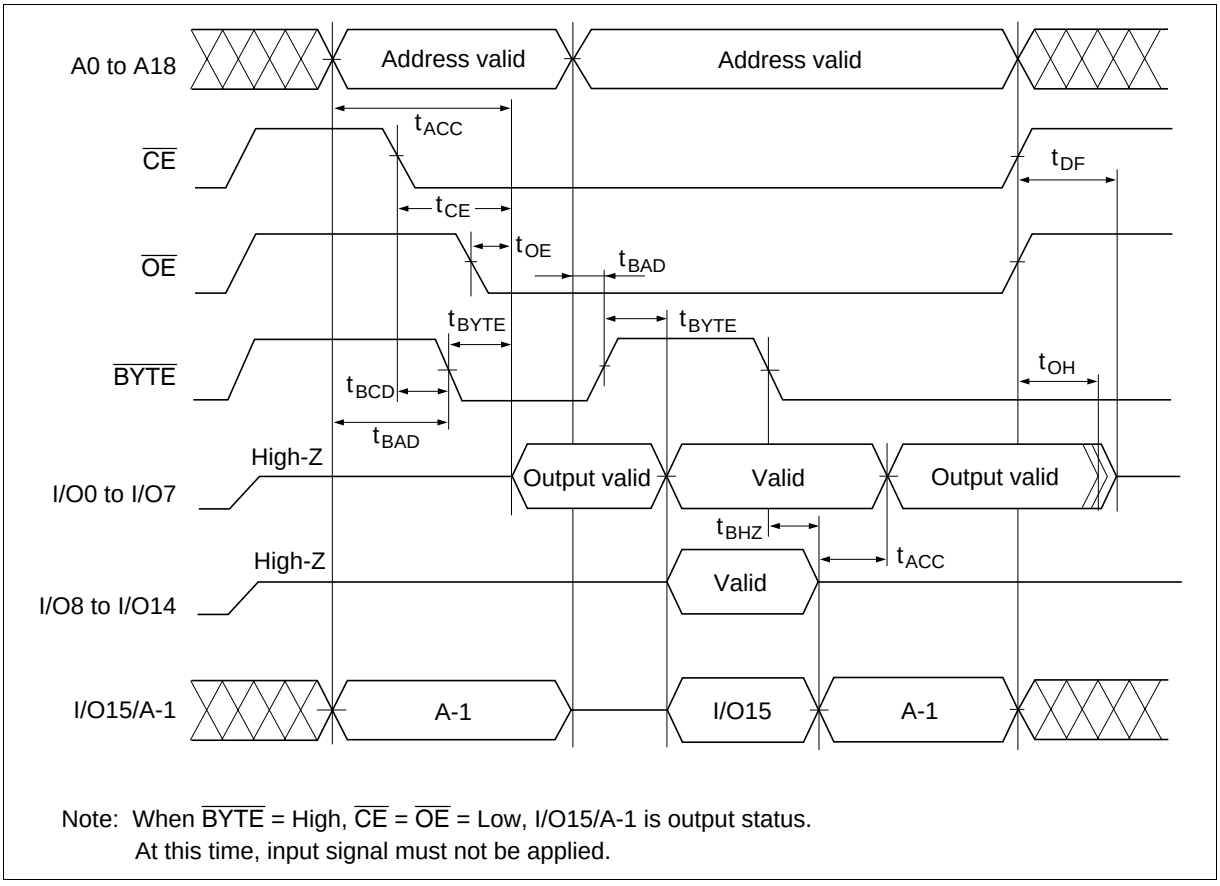
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Timing measurements are made under read timing waveform.

Read Timing Waveform (Byte Mode or Word Mode)



Read Timing Waveform (Byte Mode, Word Mode Switch)



Note: When $\overline{BYTE}$ = High, $\overline{CE}$ = $\overline{OE}$ = Low, I/O15/A-1 is output status.
At this time, input signal must not be applied.

Command Write Operation

		HN29WT800/HN29WB800									
		-8			-10			-12			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Write cycle time	t_{WC}	80	—	—	100	—	—	120	—	—	ns
Address setup time	t_{AS}	50	—	—	50	—	—	50	—	—	ns
Address hold time	t_{AH}	10	—	—	10	—	—	10	—	—	ns
Data setup time	t_{DS}	50	—	—	50	—	—	50	—	—	ns
Data hold time	t_{DH}	10	—	—	10	—	—	10	—	—	ns
$\overline{CE}$ setup time	t_{CS}	0	—	—	0	—	—	0	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	0	—	—	0	—	—	ns
Write pulse width	t_{WP}	60	—	—	60	—	—	60	—	—	ns
Write pulse high time	t_{WPH}	20	—	—	20	—	—	20	—	—	ns
$\overline{WE}$ setup time	t_{WS}	0	—	—	0	—	—	0	—	—	ns
$\overline{WE}$ hold time	t_{WH}	0	—	—	0	—	—	0	—	—	ns
$\overline{CE}$ pulse width	t_{CEP}	60	—	—	60	—	—	60	—	—	ns
$\overline{CE}$ pulse high time	t_{CEPH}	20	—	—	20	—	—	20	—	—	ns
Duration of program operation	t_{DAP}	—	25	80	—	25	80	—	25	80	ms
Duration of block erase operation	t_{DAE}	—	50	600	—	50	600	—	50	600	ms
$\overline{BYTE}$ high or low setup time	t_{BS}	50	—	—	50	—	—	50	—	—	ns
$\overline{BYTE}$ high or low hold time	t_{BH}	80	—	—	100	—	—	120	—	—	ns
$\overline{RP}$ high recovery to $\overline{WE}$ low	t_{PS}	500	—	—	500	—	—	500	—	—	ns
Block lock setup to write enable high	t_{BLS}	80	—	—	100	—	—	120	—	—	ns
	t_{WPS}	80	—	—	100	—	—	120	—	—	ns
Block lock hold from valid SRD	t_{BLH}	0	—	—	0	—	—	0	—	—	ns
	t_{WPH}	0	—	—	0	—	—	0	—	—	ns
$\overline{WE}$ high to RDY/$\overline{Busy}$ low	t_{WHRL}	—	—	80	—	—	100	—	—	120	ns
$\overline{CE}$ high to RDY/$\overline{Busy}$ low	t_{EHRL}	—	—	80	—	—	100	—	—	120	ns

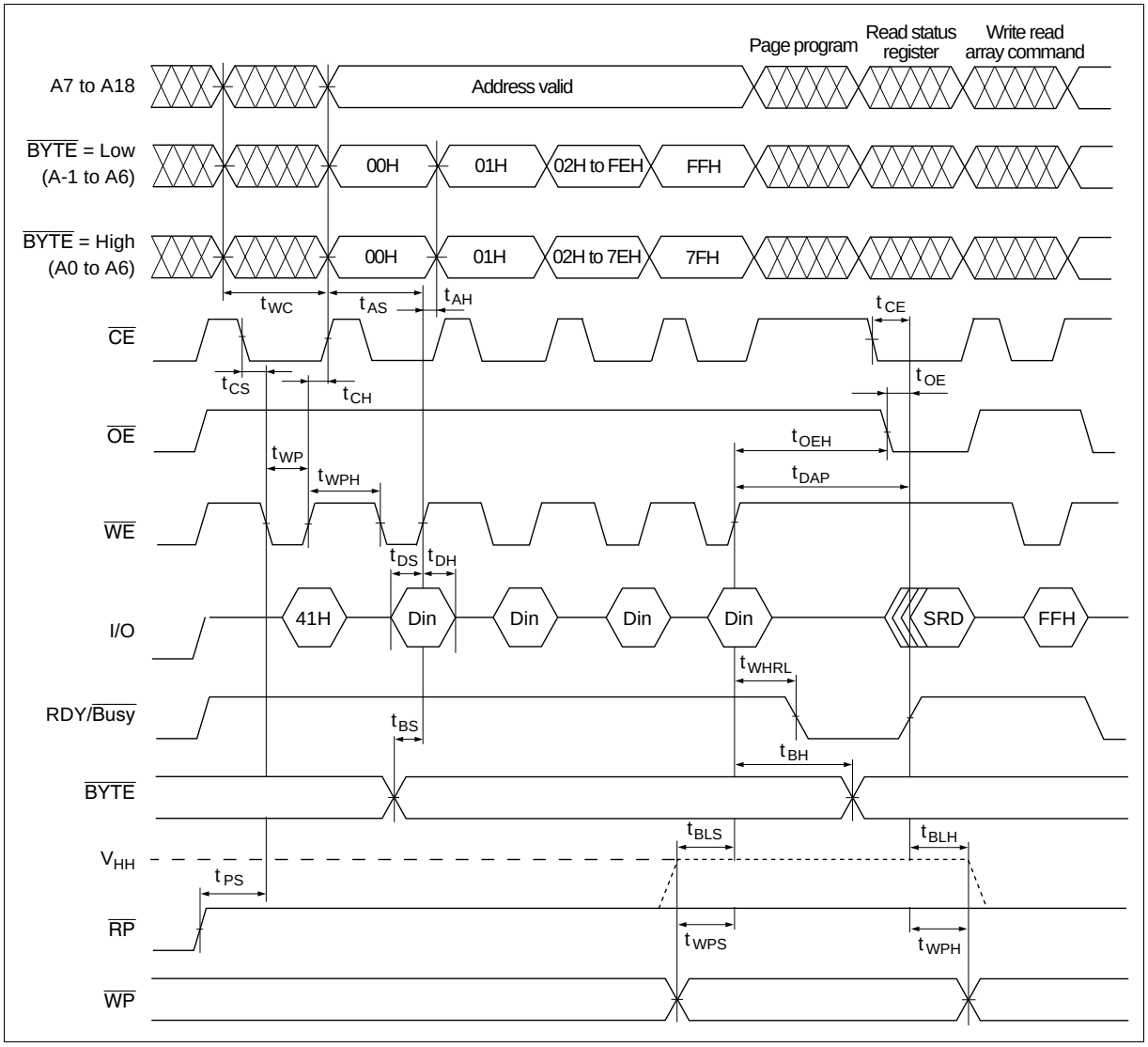
Note: Read operation parameters during command write operations mode are the same as during read timing waveform. Typical values at V_{CC} = 3.3 V, Ta = 25°C.

Erase and Program Performance

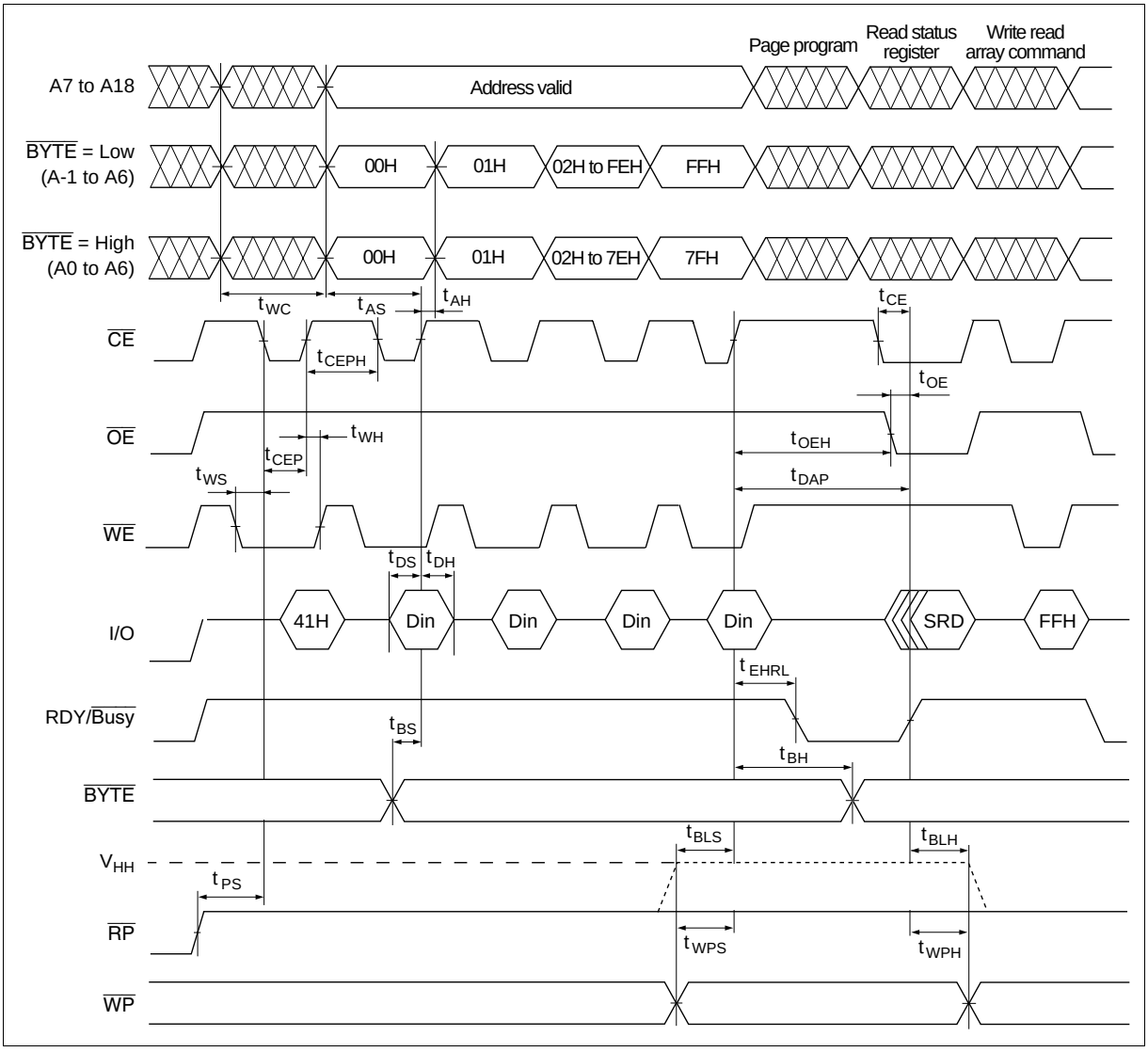
Parameter	Min	Typ	Max	Unit
Main block write time (Page mode)	—	6.4	20.4	s
Page write time	—	25	80	ms
Block erase time	—	50	600	ms

Note: Typical values at V_{CC} = 3.3 V, Ta = 25˚C. These values exclude system level overhead.

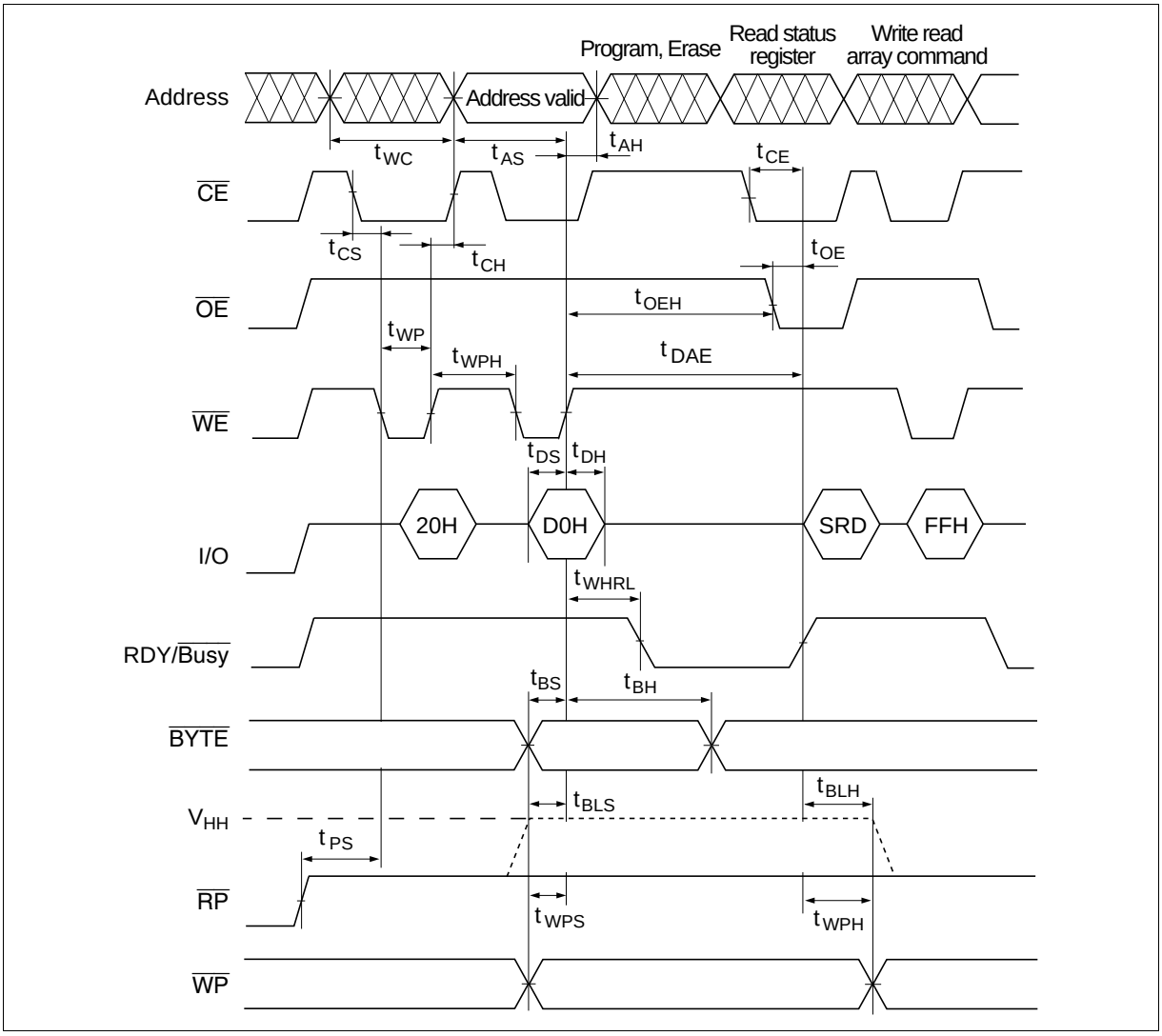
Page Program Timing Waveform ($\overline{WE}$ control)



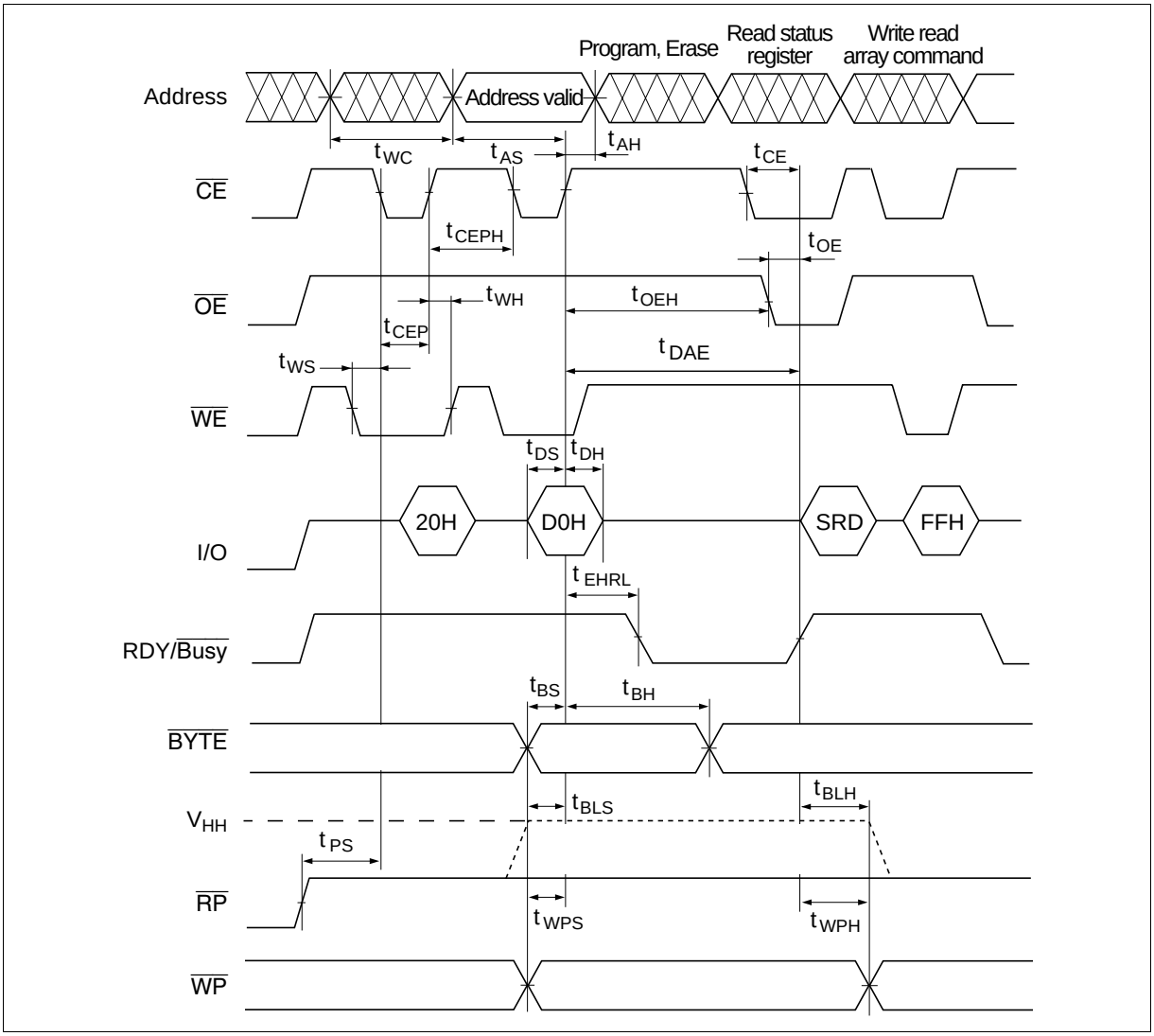
Page Program Timing Waveform ($\overline{CE}$ control)



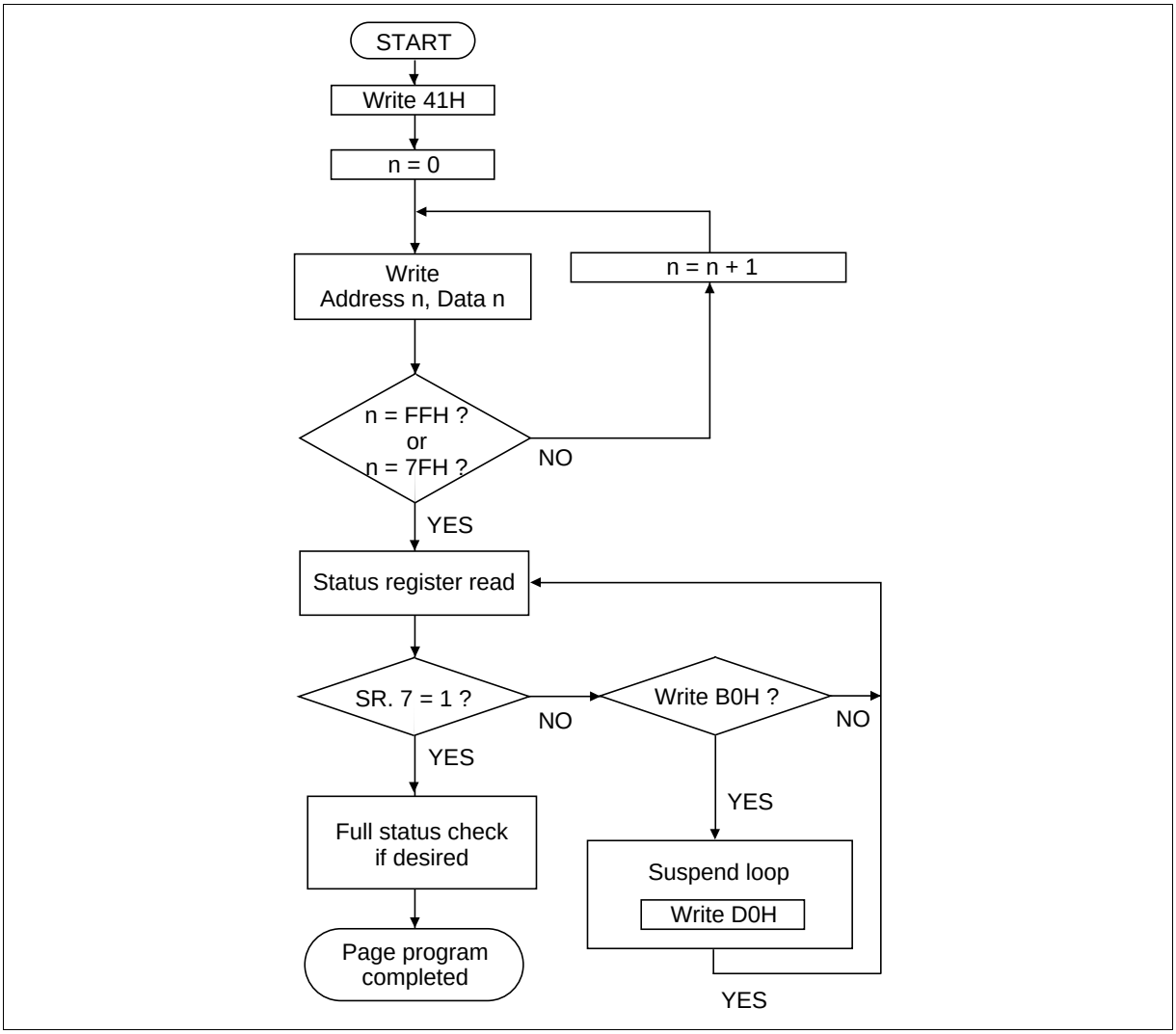
Write Timing Waveform for Erase Operations ($\overline{WE}$ control)



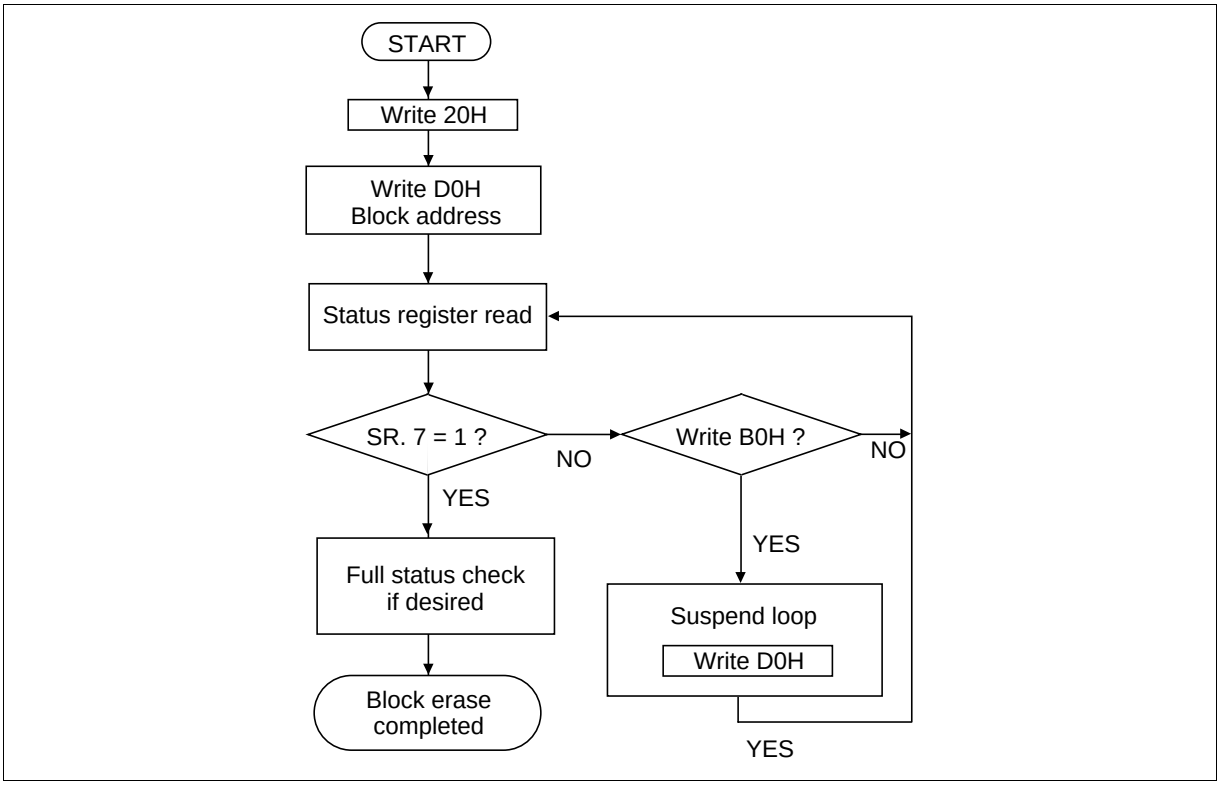
Write Timing Waveform for Erase Operations ($\overline{CE}$ control)



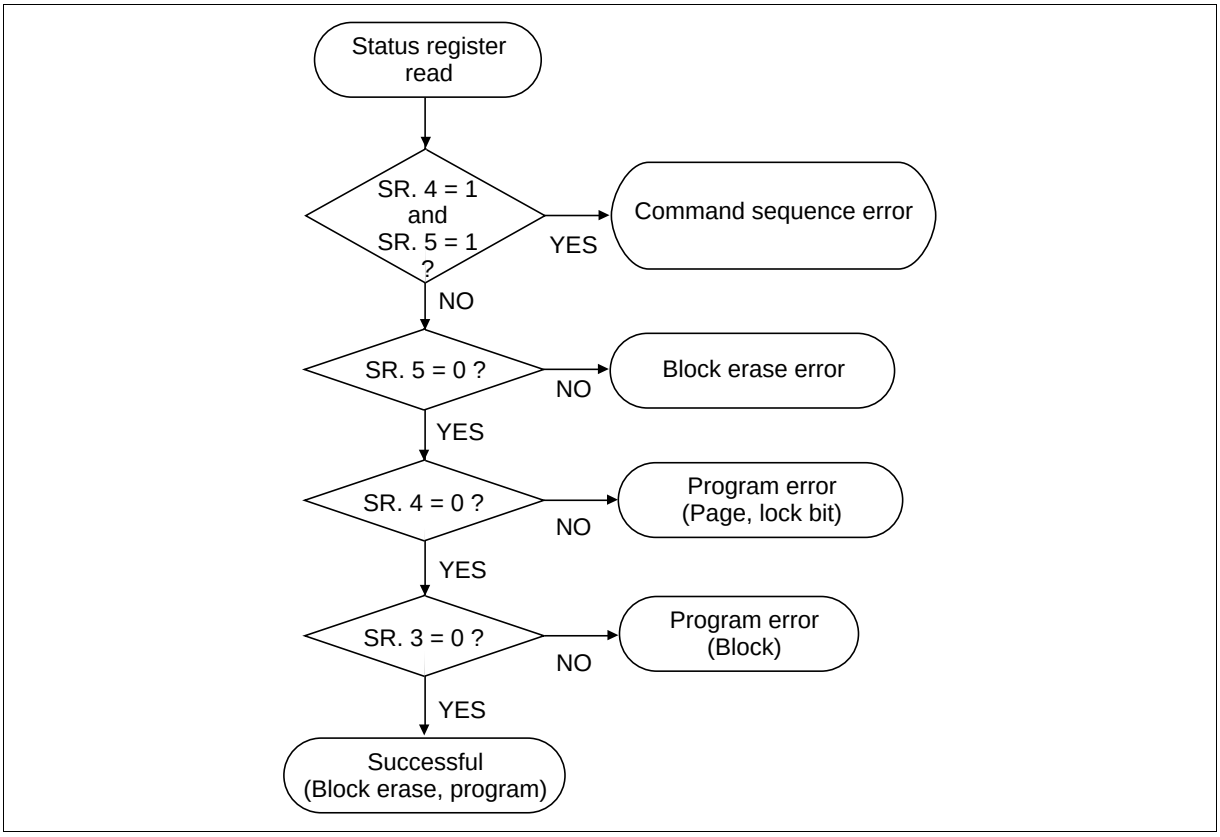
Page Program Flowchart



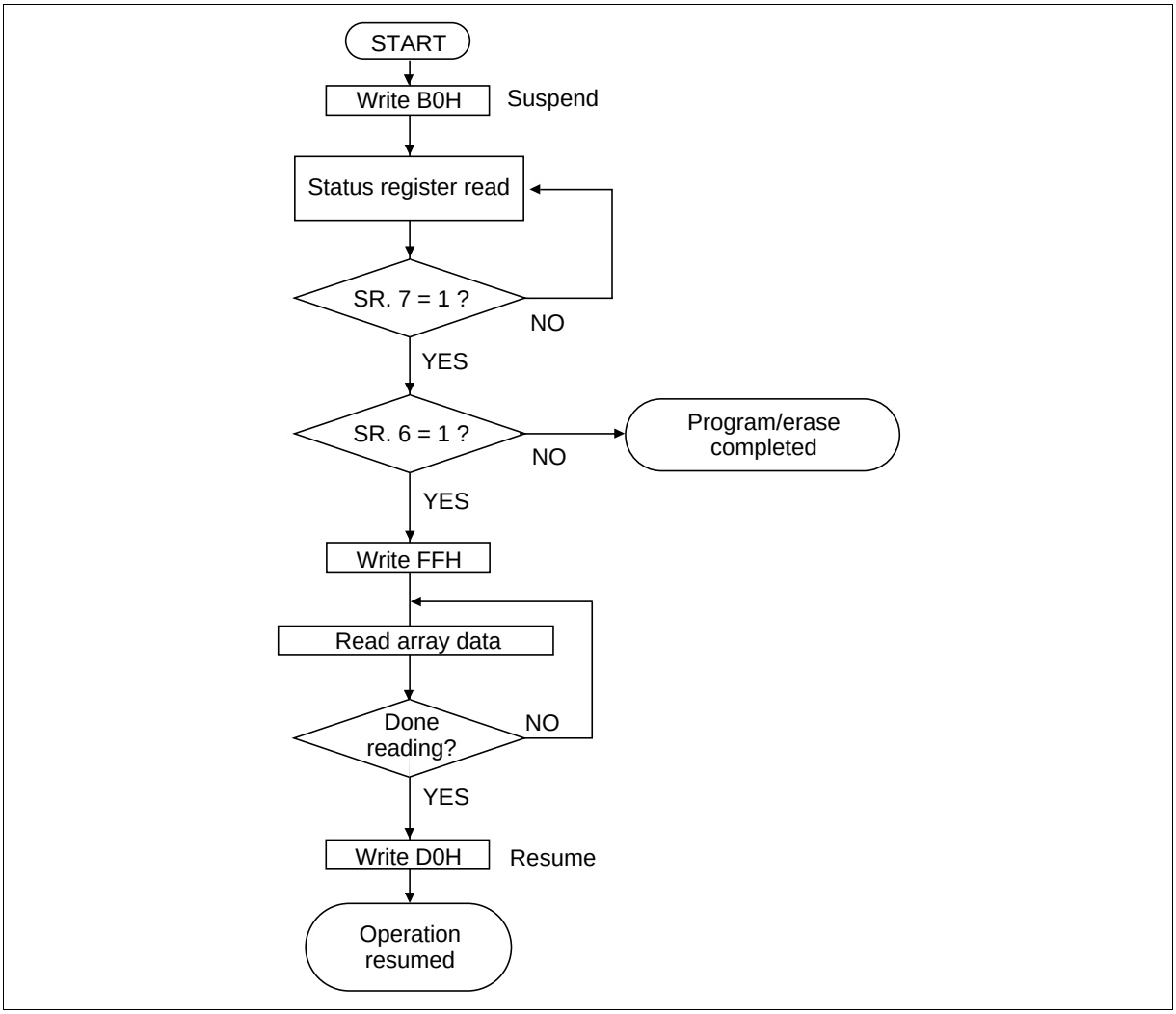
Block Erase Flowchart



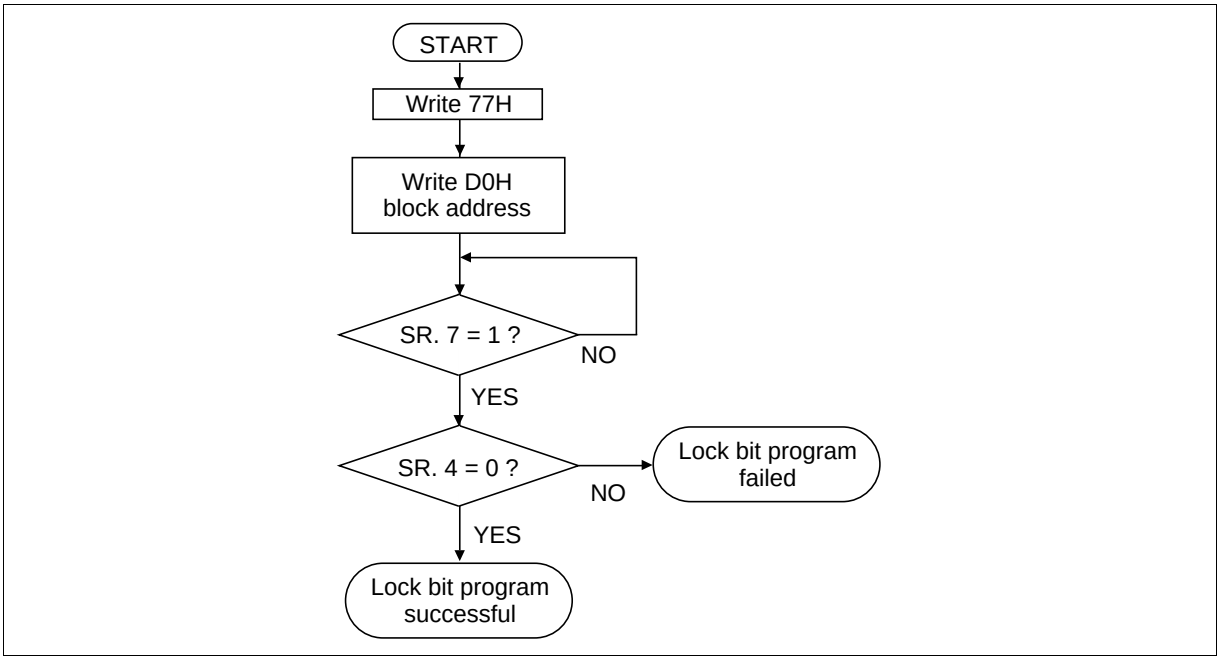
Full Status Check Procedure



Suspend/Resume Flowchart



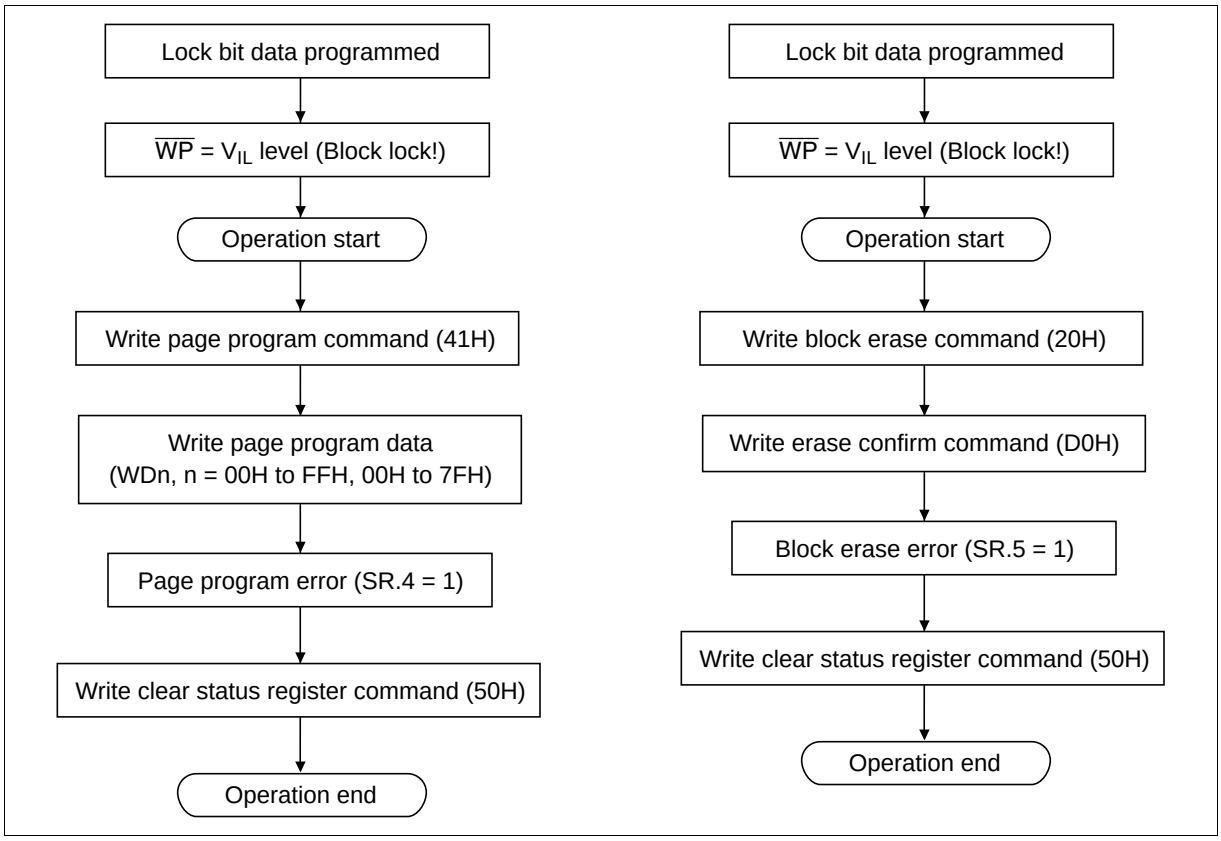
Lock Bit Program Flowchart



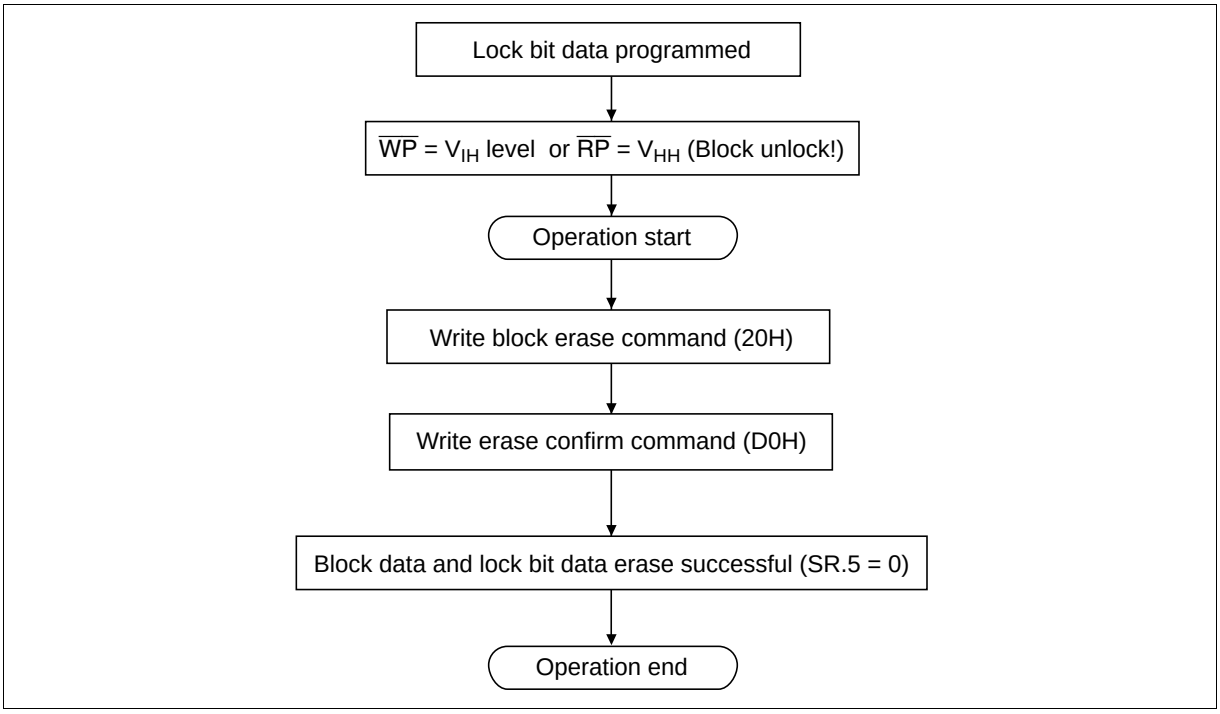
Data Protection Operation

Page programming and Block Erasing can be locked by programming a nonvolatile lock bit for each block. When $\overline{WP}$ is V_{IL} level, those locked blocks as reflected by the Block-Lock Status bits, are protected from inadvertent Page programming or Block Erasing.

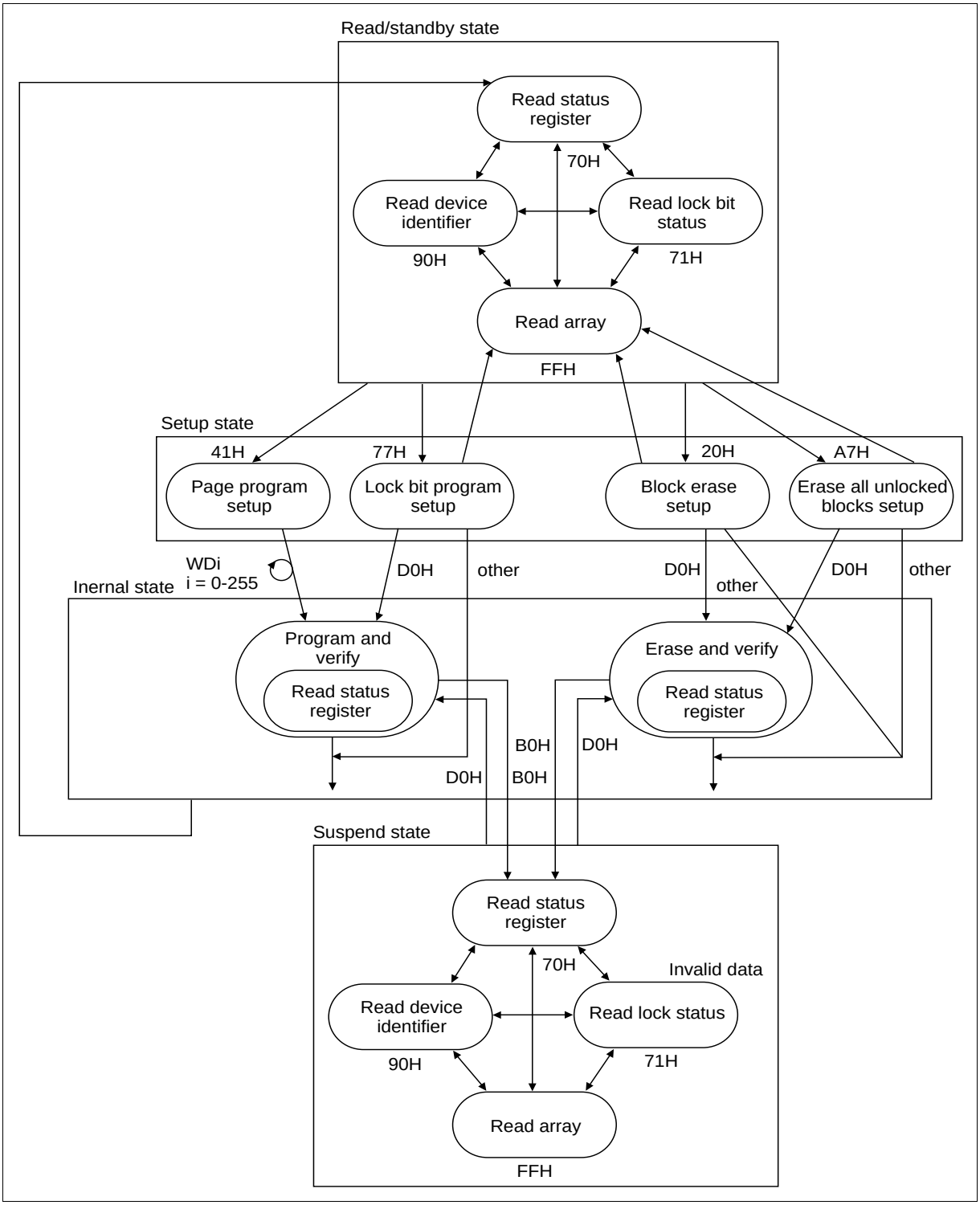
Programmed block data and Lock-Bit Data can be locked When $\overline{WP}$ is V_{IL} level.



Programmed block data and Lock-Bit Data can be erased by block erase command When $\overline{WP}$ is V_{IH} level or $\overline{RP}$ is V_{HH} level.



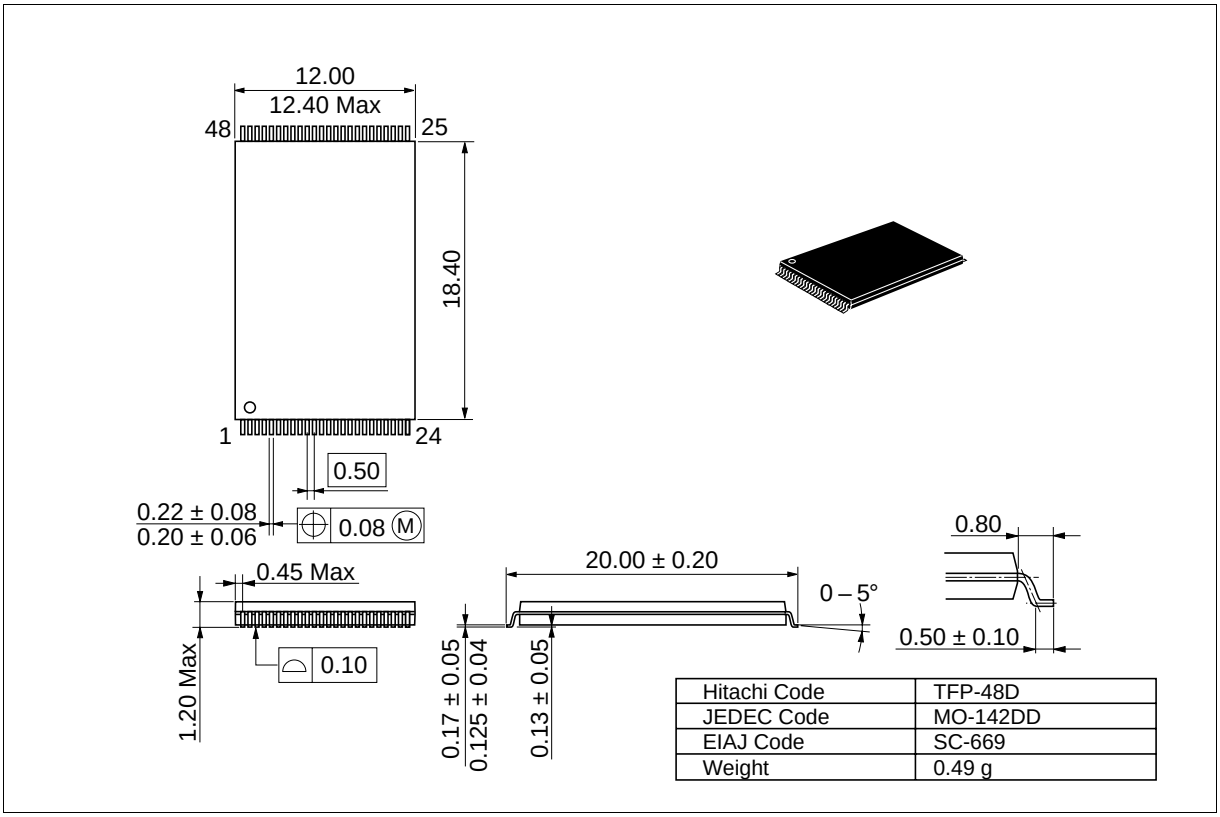
Operation Status and Effective Command



Package Dimensions

HN29WT800T/HN29WB800T Series (TFP-48D)

Unit: mm

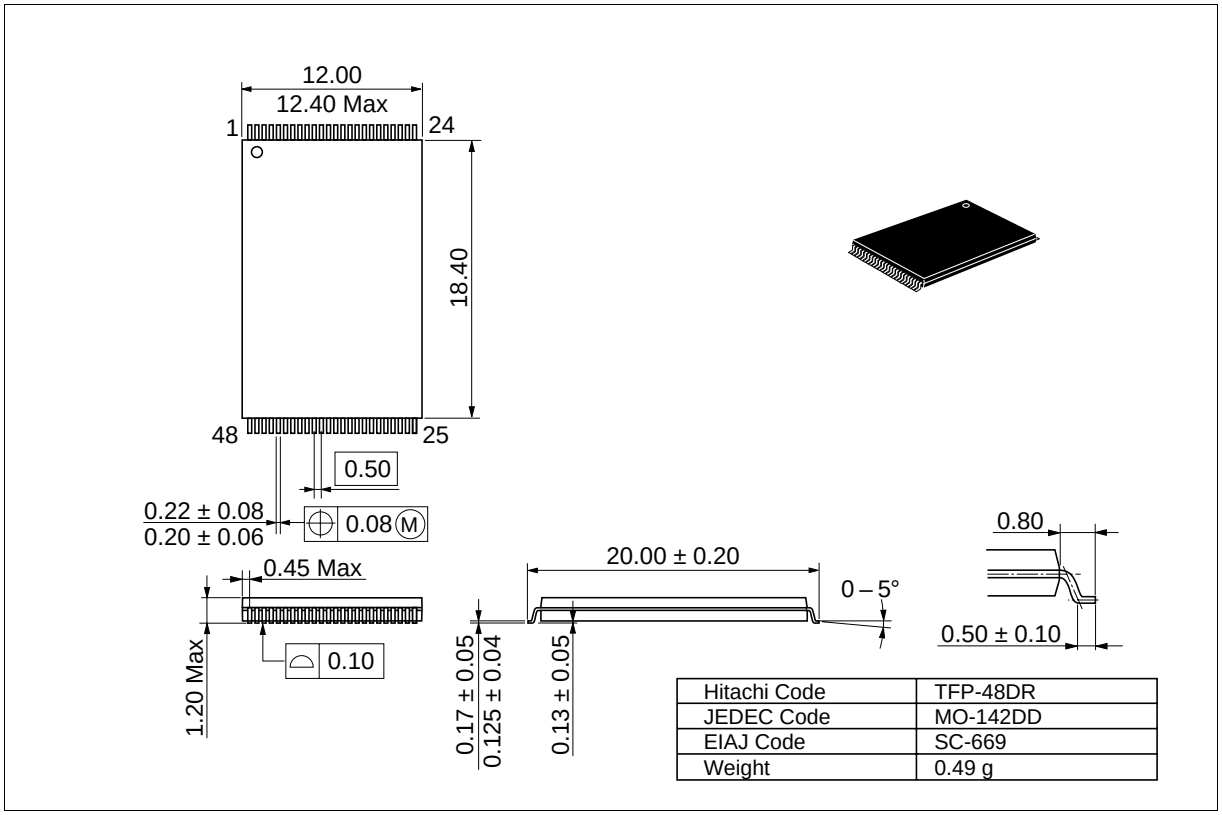


Hitachi Code	TFP-48D
JEDEC Code	MO-142DD
EIAJ Code	SC-669
Weight	0.49 g

Package Dimensions (cont.)

HN29WT800R/HN29WB800R Series (TFP-48DR)

Unit: mm



Hitachi Code	TFP-48DR
JEDEC Code	MO-142DD
EIAJ Code	SC-669
Weight	0.49 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 14, 1996	Initial issue	K. Izawa	T. Muto
1.0	May. 9, 1997	Deletion of HN29WT/WB800FP Series Addition of Top Boot Block Address Map and Bottom Boot Block Address Map Software Command Definition Deletion of Sleep command Deletion of notes8 Deletion of Block Locking (SOP Package) Change of Status Register Data (SRD) DC Characteristics V_{LKO} min: 1.5 V to 1.2 V V_{LKO} max: 2.5 V to — AC Characteristics Test Conditions (HN29WT/WB800-10/12): 1TTL gate + 50 pF to 1TTL gate + 100 pF Change of parameter name: t_{RWH} to t_{PS} Deletion of t_{RP} t_{PS} min: 0/0/0 ns 500/500/500 ns t_{DAP} max: 120/120/120 ms to 80/80/80 ms Erase and program performance Main block write time max: 38.4 s to 20.4 s Page write time max: 120 ms to 80 ms Change of Full Status Check Procedure and Operation Status and Effective Command Addition of Data Protection Operation		