HT45R35V
C/R to F Type 8-Bit OTP MCU

Technical Document

- Tools Information
- FAQs
- Application Note
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Features

- Operating voltage:
  f_{SYS}=4MHz: 2.2V~5.5V
  f_{SYS}=8MHz: 3.3V~5.5V
- 16 bidirectional I/O lines
- Two external interrupt inputs shared with I/O lines
- 8-bit programmable timer/event counter with overflow interrupt and 7-stage prescaler
- External RC oscillation converter
- On-chip crystal and RC oscillator
- Watchdog Timer
- 12 capacitor/resistor sensor input
- 2048×14 program memory
- 120×8 data memory RAM
- Power Down and Wake-up function reduce power consumption
- Up to 0.5μs instruction cycle with 8MHz system clock at V_{DD}=5V
- All instructions executed in one or two instruction cycles
- 14-bit table read instruction
- Four-level subroutine nesting
- Bit manipulation instruction
- 63 powerful instructions
- Low voltage reset function
- Integrated DC 24V to 5V LDO regulator
- Buzzer and filament 5V to 24V output level shifter
- 24-bit shift register/latch for VFD panel driving 24 grid/segment outputs
- Integrated 3-line serial VFD interface for grid/segment display control
- 52-pin QFP package type

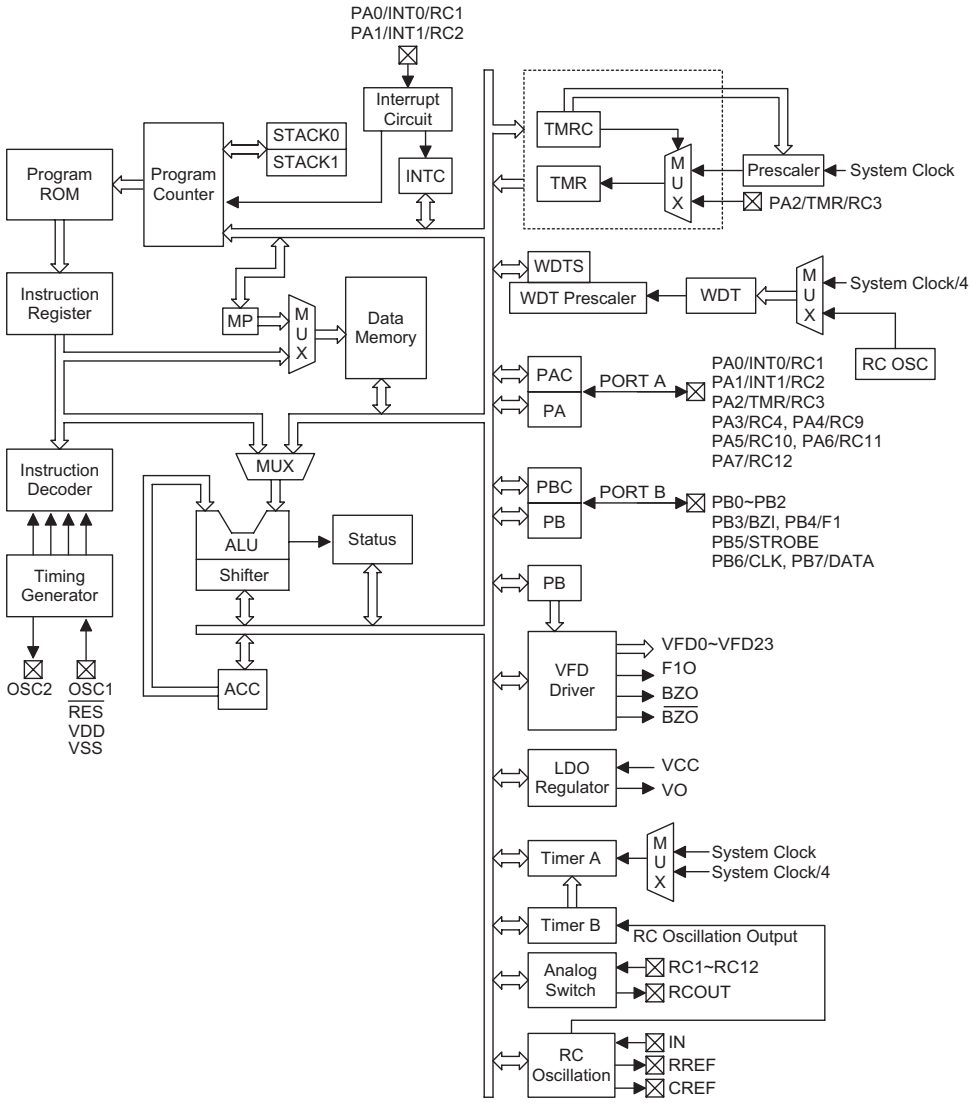
General Description

The HT45R35V is a C/R to F Type with 8-bit high performance RISC architecture microcontroller designed especially for VFD applications.

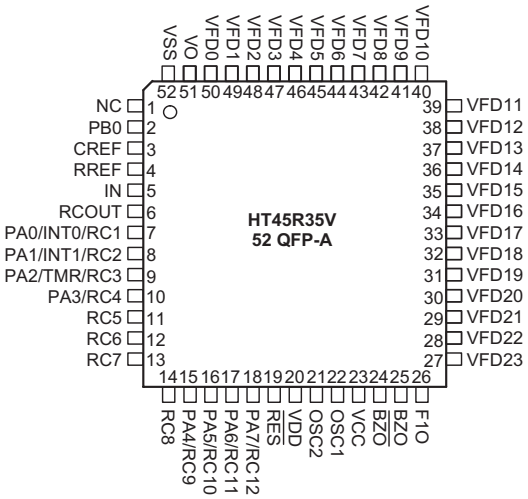
The usual Holtek MCU features such as power down and wake-up functions, oscillator options, etc. combine to ensure user applications require a minimum of external components.

The device is specifically designed for VFD applications that interface directly to VFD panels. The benefits of integrated C/R to F functions, in addition to low power consumption, high performance, I/O flexibility and low-cost, enhance the versatility of these devices to suit a wide range of VFD application possibilities such as household appliance timers, various consumer products, subsystem controllers, other home appliances etc.

Block Diagram



Pin Assignment



Pin Description

Pin Name	I/O	Options	Description
PA0/INT0/RC1 PA1/INT1/RC2 PA2/TMR/RC3 PA3/RC4 PA4/RC9 PA5/RC10 PA6/RC11 PA7/RC12	I/O	Pull-high* Wake-up	Bidirectional 8-bit I/O port. Each pin can be configured as a wake-up input via configuration options. Software instructions determine if the pin is a CMOS output or Schmitt trigger input. Pull-high resistors can be added to the each pin via a configuration option. Pins PA0 and PA1 are pin-shared with external interrupt input pins INT0 and INT1, respectively. Configuration options determine the interrupt enable/disable and the interrupt low/high trigger type. Pins PA2 is pin-shared with the external timer input pins TMR. Each Pin of PA0~PA3 and PA4~PA7 are pin-shared with RC1~RC4 and RC9~RC12 respectively via configuration options. RC1~RC4 and RC9~RC12 are capacitor or resistor connection pins.
PB0	I/O	Pull-high*	Bidirectional 1-bit I/O port. Software instructions determine if the pin is a CMOS output or Schmitt trigger input. Pull-high resistors can be added to the each pin via a configuration option.
PB1~PB2	—	—	These two pads are internal I/O and not bound out.
PB3/BZI PB4/F1 PB5/STROBW PB6/CLK PB7/DATA	I/O	Pull-high*	PB3~PB7 are used to control the VFD driver interface. Configuration options determine which pins on the port have pull-high resistors. The pins should only be used as outputs and as VFD interface pins and not as normal I/O pins.
RC5~RC8	II/O	—	Capacitor or resistor connection pins
RCOUT	I	—	Capacitor or resistor connection pin to RC OSC
IN	I	—	Oscillation input pin
RREF	O	—	Reference resistor connection pin
CREF	O	—	Reference capacitor connection pin
F1O	O	—	High voltage filament output signal

Pin Name	I/O	Options	Description
BZO $\overline{BZO}$	O	—	High voltage buzzer complement output signals
VO	—	—	LDO regulator output
VCC	—	—	High voltage positive power supply for driving the VFD filament, F1O, BZO and $\overline{BZO}$ outputs. An external 10uF capacitor is recommended to be connected to ground on the PCB to reduce surge voltages.
VFD0~VFD23	O	—	High voltage grid/segment output for VFD panel
$\overline{RES}$	I	—	Schmitt trigger reset input. Active low
VSS	—	—	Negative power supply, ground
VDD	—	—	Positive power supply
OSC1 OSC2	I O	Crystal or RC	OSC1, OSC2 are connected to an RC network or Crystal determined by a configuration option, for the internal system clock. In the case of the RC oscillator, OSC2 can be used to monitor the system clock. Its frequency is 1/4 system clock.

Note: 1. *All pull-high resistors are controlled by an option bit.

2. Pin PB3~PB7 are five internal pins only and not bound out and its port control register must setup this pin as an output.

3. PB3~PB7 individual pins can be selected to have a pull-high resistor.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+6.0V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

VCC Supply Voltage ..... 12V to 24V

I_{OH} Total ..... –100mA

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –40°C to 85°C

I_{OL} Total 150mA

Total Power Dissipation 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
		V_{DD}	V_{CC}	Conditions				
V_{DD}	Operating Voltage	—	—	f_{SYS}=4MHz	2.2	—	5.5	V
				f_{SYS}=8MHz	3.3	—	5.5	V
I_{DD1}	Operating Current (Crystal OSC, RC OSC)	3V	—	No load, f_{SYS}=4MHz	—	1	2	mA
		5V	—		—	3	5	mA
I_{DD2}	Operating Current (Crystal OSC, RC OSC)	5V	—	No load, f_{SYS}=8MHz	—	4	8	mA
I_{STB1}	Standby Current (WDT Enabled)	3V	—	No load, system HALT	—	—	5	μA
		5V	—		—	—	10	μA
I_{STB2}	Standby Current (WDT Disabled)	3V	—	No load, system HALT	—	—	1	μA
		5V	—		—	—	2	μA
V_{IL1}	Input Low Voltage for I/O Ports, TMR, INT0 and INT1	—	—	—	0	—	$0.3V_{DD}$	V

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
		V_{DD}	V_{CC}	Conditions				
V_{IH1}	Input High Voltage for I/O Ports, TMR, INT0 and INT1	—	—	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL2}	Input Low Voltage ($\overline{RES}$)	—	—	—	0	—	$0.4V_{DD}$	V
V_{IH2}	Input High Voltage ($\overline{RES}$)	—	—	—	$0.9V_{DD}$	—	V_{DD}	V
V_{LVR}	Low Voltage Reset	—	—	LVR enabled	2.7	3.0	3.3	V
I_{OL}	I/O, RREF and CREF Sink Current	3V	—	V_{OL}=0.1V_{DD}	4	8	—	mA
		5V	—		10	20	—	mA
I_{OH}	I/O, RREF and CREF Source Current	3V	—	V_{OH}=0.9V_{DD}	–2	–4	—	mA
		5V	—		–5	–10	—	mA
R_{PH}	Pull-high Resistance	3V	—	—	20	60	100	kΩ
		5V	—	—	10	30	50	kΩ
R_{PL}	RC1~RC12 Pull-low Resistance	3V	—	—	20	60	100	kΩ
		5V	—	—	10	30	50	kΩ
V_O	LDO Output Voltage	—	—	—	4.7	5.0	5.3	V
V_{CC}	VFD, F1O, BZO and $\overline{BZO}$ Output Supply Voltage	—	—	—	12	—	24	V
I_{OUT}	Maximum LDO Output Current	—	—	For V_{CC}≥5V	10	—	—	mA
ΔVLNR	Line Regulation	—	—	V_{IN}=(V_{OUT}+0.1V) to 24V, I_{OUT}=1mA	TBD	0.06	TBD	%/V
ΔVLDR	Load Regulation	—	—	I_{OUT}=100μA to 20mA, C_{OUT}=10pF	TBD	0.16	TBD	%/mA
VDRO	Dropout Voltage	—	—	I_{OUT}=1mA	25	30	35	mV
I_{CC1}	Logic Operating Current 1	5V	18V	No load, VFD outputs, all output low, CLK=100kHz	—	70	110	μA
			24V		—	TBD	TBD	μA
I_{CC2}	Logic Operating Current 2	5V	18V	No load, VFD outputs, all output high, CLK=100kHz	—	70	110	μA
			24V		—	TBD	TBD	μA
I_{CC3}	Buzzer Operating Current	5V	18V	No load, BZI input 50kHz	—	130	180	μA
			24V		—	TBD	TBD	μA
I_{CC4}	Filament Operating Current	5V	18V	No load, F1 input 50kHz	—	90	140	μA
			24V		—	TBD	TBD	μA
I_{STB}	Standby Current (LDO Always On, WDT Enable/Disable)	5V	18V	No load	—	65 (TBC)	105 (TBC)	μA
			24V		—	TBD	TBD	μA
I_{OL2}	F1O Sink Current	5V	18V	V_{OL}= 0.1V_{CC}	2.5	5.0	—	mA
			24V		TBD	TBD	—	mA
I_{OH2}	F1O Source Current	5V	18V	V_{OH}= 0.9V_{CC}	–15	–30	—	mA
			24V		TBD	TBD	—	mA
I_{OL3}	BZO/$\overline{BZO}$ Sink Current	5V	18V	V_{OL}= 0.1V_{CC}	15	30	—	mA
			24V		TBD	TBD	—	mA

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
		V_{DD}	V_{CC}	Conditions				
I_{OH3}	BZO/$\overline{BZO}$ Source Current	5V	18V	V_{OH}= 0.9V_{CC}	–15	–30	—	mA
			24V		TBD	TBD		mA
I_{OL4}	Grid/Segment Sink Current	5V	18V	V_{OL}= 0.1V_{CC}	2.5	5.0	—	mA
			24V		TBD	TBD	—	mA
I_{OH4}	Grid/Segment Source Current	5V	18V	V_{OH}= 0.9V_{CC}	–6	–12	—	mA
			24V		TBD	TBD	—	mA

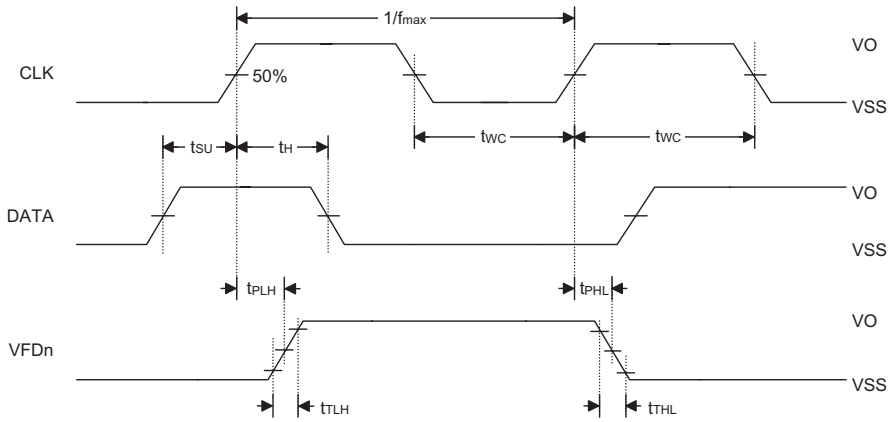
A.C. Characteristics

Ta=25°C

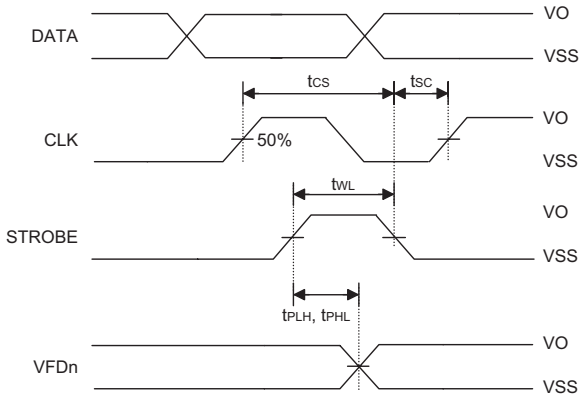
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Clock (Crystal OSC, RC OSC)	—	2.2V~5.5V	400	—	4000	kHz
		—	3.3V~5.5V	400	—	8000	kHz
f_{TIMER}	Timer I/P Frequency	—	2.2V~5.5V	0	—	4000	kHz
		—	3.3V~5.5V	0	—	8000	kHz
t_{WDTOSC}	Watchdog Oscillator Period	3V	—	45	90	180	μs
		5V	—	32	65	130	μs
t_{WDT1}	Watchdog Time-out Period (WDT RC OSC)	3V	Without WDT prescaler	11	23	46	ms
		5V		8	17	33	ms
t_{WDT2}	Watchdog Time-out Period (System Clock/4)	—	Without WDT prescaler	—	1024	—	t_{SYS}
t_{RES}	External Reset Low Pulse Width	—	—	1	—	—	μs
t_{SST}	System Start-up Timer Period	—	Wake-up from HALT	—	1024	—	t_{SYS}
t_{INT}	Interrupt Pulse Width	—	—	1	—	—	μs
t_{LVR}	Low Voltage Reset Time	—	—	0.25	1	2	ms
t_{PHL}, t_{PLH}	Propagation Delay Time (Clock to VFD Output)	—	V_{CC}=15V	—	100	200	ns
	Propagation Delay Time (Strobe to VFD Output)	—	V_{CC}=15V	—	100	200	ns
t_{THL}, t_{TLH}	Output Transition Time	—	V_{CC}=15V	—	40	80	ns
t_{SU}	Data Setup Time	—	V_{CC}=15V	—	10	20	ns
t_{CS}	Setup Time (Clock to Strobe)		V_{CC}=15V	—	10	20	ns
t_H	Hold Time (Data to Clock)		V_{CC}=15V	—	10	20	ns
t_{SC}	Hold Time (Clock to Strobe)		V_{CC}=15V	—	75	150	ns
t_r, t_f	Clock Input Rise or Fall Time	—	V_{CC}=15V	—	—	20	ns
t_{WC}	Clock Pulse Width	—	V_{CC}=15V	—	40	83	ns
t_{WL}	Strobe Pulse Width	—	V_{CC}=15V	—	35	70	ns
f_{max}	Maximum Clock Input Frequency	—	V_{CC}=15V	—	8	—	MHz

Note: *t_{SYS}=1/f_{SYS}

A.C. Waveforms



Data Propagation Delays, Setup and Hold Times



Strobe Propagation Delays, Setup and Hold Times

Functional Description

Execution Flow

The system clock for the microcontroller is derived from either a crystal or an RC oscillator. The system clock is internally divided into four non-overlapping clocks. One instruction cycle consists of four system clock cycles.

Instruction fetching and execution are pipelined in such a way that a fetch takes an instruction cycle while decoding and execution takes the next instruction cycle. However, the pipelining scheme causes each instruction to effectively execute in a cycle. If an instruction changes the program counter, two cycles are required to complete the instruction.

Program Counter – PC

The program counter, PC controls the sequence in which the instructions stored in program ROM are executed and its contents specify full range of program memory.

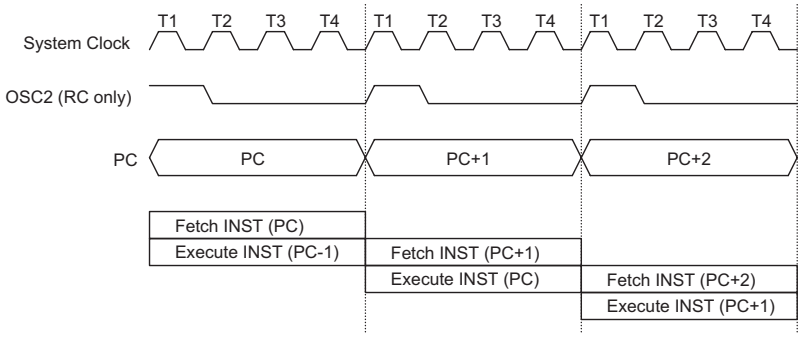
After accessing a program memory word to fetch an instruction code, the contents of the program counter are incremented by one. The program counter then points to the memory word containing the next instruction code.

When executing a jump instruction, a conditional skip execution, loading the PCL register, a subroutine call, an initial reset, an internal interrupt, an external interrupt or return from a subroutine, the PC manipulates the program transfer by loading the address corresponding to each instruction.

The conditional skip is activated by instructions. Once the condition is met, the next instruction, fetched during the current instruction execution, is discarded and a dummy cycle replaces it to get the proper instruction. Otherwise the program will proceed with the next instruction.

The lower byte of the program counter, PCL is a readable and writable register. Moving data into the PCL performs a short jump. The destination must be within the current Program Memory Page.

When a control transfer takes place, an additional dummy cycle is required.



Execution Flow

Mode	Program Counter										
	*10	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
Initial Reset	0	0	0	0	0	0	0	0	0	0	0
External Interrupt 0	0	0	0	0	0	0	0	0	1	0	0
External Interrupt 1	0	0	0	0	0	0	0	1	0	0	0
Timer/Event Counter Overflow	0	0	0	0	0	0	0	1	1	0	0
External RC Oscillation Converter Interrupt	0	0	0	0	0	0	1	0	0	0	0
Skip	Program Counter+2										
Loading PCL	*10	*9	*8	@7	@6	@5	@4	@3	@2	@1	@0
Jump, Call Branch	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0
Return from Subroutine	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

Program Counter

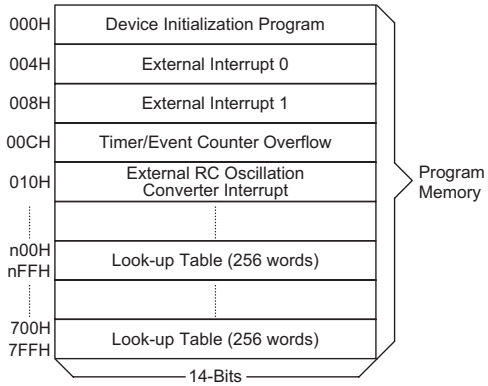
Note: *10~*0: Program Counter bits
#10~#0: Instruction code bits
S10~S0: Stack register bits
@7~@0: PCL bits

Program Memory

The program memory is used to store the program instructions which are to be executed. It also contains data, table, and interrupt entries, and is organized into 2048×14 bits, addressed by the program counter and table pointer.

Certain locations in the program memory are reserved for special usage:

- Location 000H
  This area is reserved for program initialisation. After a device reset, the program always begins execution at location 000H.
- Location 004H
  This location is reserved for the external interrupt 0 service program. If the INT0 input pin is activated, the interrupt is enabled and the stack is not full, the program begins execution at this location.
- Location 008H
  This location is reserved for the external interrupt 1 service program. If the INT1 input pin is activated, the interrupt is enabled and the stack is not full, the program begins execution at this location.
- Location 00CH
  This location is reserved for the Timer/Event Counter interrupt service program. If a Timer interrupt results from a Timer/Event Counter overflow, and the interrupt is enabled and the stack is not full, the program begins execution at this location.



Note: n ranges from 0 to 7

Program Memory

- Location 010H
  This location is reserved for the external RC oscillation converter interrupt service program. If an interrupt results from an external RC oscillation converter, and if the interrupt is enabled and the stack is not full, the program begins execution at this location.
- Table location
  Any location in the program memory can be used as a look-up table. The instructions "TABRDC [m]" (the current page, 1 page=256 words) and "TABRDL [m]" transfer the contents of the lower-order byte to the specified data memory, and the higher-order byte to TBLH. Only the destination of the lower-order byte in the table is well-defined, the other bits of the table word are transferred to the lower portion of TBLH, and the remaining 2 bits are read as "0". The Table Higher-order byte register, TBLH, is read only. The table pointer, TBLP, is a read/write register, which indicates the table location. Before accessing the table, the location must be placed in TBLP. The TBLH register is read only and cannot be restored. If the main routine and the ISR (Interrupt Service Routine) both employ the table read instruction, the contents of the TBLH in the main routine are likely to be changed by the table read instruction used in the ISR and errors may occur. Therefore, using the table read instruction in the main routine and also in the ISR should be avoided. However, if the table read instruction has to be used in both the main routine and in the ISR, the interrupt should be disabled prior to the table read instruction execution. The interrupt should not be re-enabled until TBLH has been backed up. All table related instructions require two cycles to complete the operation. These areas may function as normal program memory depending upon the requirements.

Stack Register – STACK

This is a special part of the memory which is used to save the contents of the program counter only. The stack is organised into 4-levels and is neither part of the data nor part of the program space, and is neither readable nor writable. The activated level is indexed by the stack pointer, SP and is neither readable nor writeable. At a subroutine call or interrupt acknowledgment, the contents of the program counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled

Instruction	Table Location										
	*10	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
TABRDC [m]	P10	P9	P8	@7	@6	@5	@4	@3	@2	@1	@0
TABRDL [m]	1	1	1	@7	@6	@5	@4	@3	@2	@1	@0

Table Location

Note: *10~*0: Table location bits
P10~P8: Current program counter bits
@7~@0: Table pointer bits

by a return instruction, RET or RETI, the program counter is restored to its previous value from the stack. After a device reset, the stack pointer will point to the top of the stack.

If the stack is full and a non-masked interrupt takes place, the interrupt request flag will be recorded but the acknowledgment will be inhibited. When the stack pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. In a similar case, if the stack is full and a "CALL" is subsequently executed, stack overflow occurs and the first entry will be lost as only the most recent 4 return addresses are stored.

Data Memory – RAM

The data memory has a capacity of 146×8 bits. The data memory is divided into two functional groups: special function registers and general purpose data memory (120×8). Most are read/write, but some are read only. The general purpose data memory, addressed from 28H to 7FH at Bank 0 and from 40H to 5FH at Bank 1, is used for data and control information under instruction commands.

All of the data memory areas can handle arithmetic, logic, increment, decrement and rotate operations directly. Except for some dedicated bits, each bit in the data memory can be set and reset by the "SET [m].i" and "CLR [m].i" bit manipulation instructions. They are also indirectly accessible through the memory pointer registers (MP0;01H, MP1;02H).

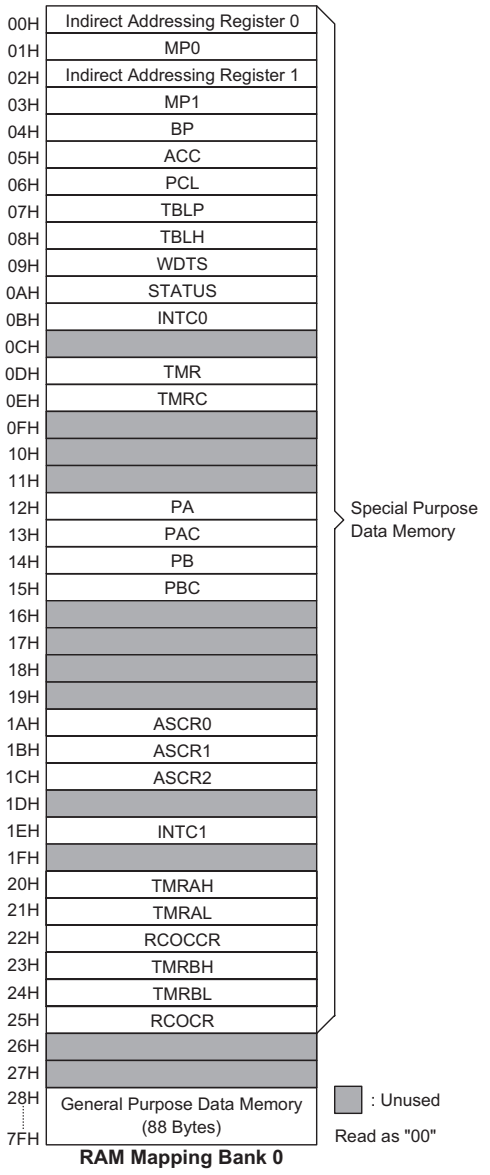
Bank 1 must be addressed indirectly using the memory pointer MP1 and the indirect addressing register IAR1. Any direct addressing or any indirect addressing using MP0 and IAR0 will always result in data from Bank 0 being accessed.

Indirect Addressing Register

The method of indirect addressing allows data manipulation using memory pointers instead of the usual direct memory addressing method where the actual memory address is defined. Any action on the indirect addressing registers will result in corresponding read/write operations to the memory location specified by the corresponding memory pointers. This device contains two indirect addressing registers known as IAR0 and IAR1 and two memory pointers MP0 and MP1. Note that these indirect addressing registers are not physically implemented and that reading the indirect addressing registers indirectly will return a result of "00H" and writing to the registers indirectly will result in no operation.

The two memory pointers, MP0 and MP1, are physically implemented in the data memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant indirect addressing registers is carried out, the actual address that the microcontroller is directed to is the address specified by the related memory pointer.

Bit 7 of the memory pointers are not implemented. However, it must be noted that when the memory pointers in this device is read, a value of "1" will be read.



RAM Mapping

Bank Pointer – BP

When using instructions to access the general purpose data memory in Bank 0 or Bank 1, it is necessary to ensure that the correct area is selected. The general purpose data memory is sub-divided into two banks, Bank 0 and Bank 1 for this device. Selecting the correct data memory area is achieved by using the bank pointer. If data in Bank 0 or Bank 1 is to be accessed, the BP must be set to the values ″00H″ or ″01H″ respectively, however, it must be noted that data in Bank 1 can only be addressed indirectly using the MP1 memory pointer and the IAR1 indirect addressing register.

Any direct addressing or any indirect addressing using MP0 and IAR0 will always result in data from Bank 0 being accessed. The data memory is initialized to Bank 0 after a reset, except for the WDT time-out reset in the Power Down Mode, in which case, the data memory bank remains unchanged.

It should be noted that the special function data memory is not affected by the bank selection, which means that the special function registers can be accessed from within either Bank 0 or Bank 1.

Accumulator

The accumulator is closely related to ALU operations. It is also mapped to location ″05H″ of the data memory and can carry out immediate data operations. The data movement between two data memory locations must pass through the accumulator.

Arithmetic and Logic Unit – ALU

This circuit performs 8-bit arithmetic and logic operations. The ALU provides the following functions:

- Arithmetic operations – ADD, ADC, SUB, SBC, DAA
- Logic operations – AND, OR, XOR, CPL
- Rotation – RL, RR, RLC, RRC
- Increment and Decrement – INC, DEC
- Branch decision – SZ, SNZ, SIZ, SDZ ....

The ALU not only saves the results of a data operation but also changes the status register.

Status Register – STATUS

This 8-bit register contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). It also records the status information and controls the operation sequence.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition operations related to the status register may give different results from those intended. The TO flag can be affected only by a system power-up, a WDT time-out or executing the ″CLR WDT″ or ″HALT″ instruction.

The PDF flag can be affected only by executing a ″HALT″ or ″CLR WDT″ instruction or a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

In addition, on entering the interrupt sequence or executing the subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status are important and if the subroutine can corrupt the status register, precautions must be taken to save it properly.

Bit No.	Label	Function
0	C	C is set if the operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.
1	AC	AC is set if the operation results in a carry out of the low nibbles in addition or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
2	Z	Z is set if the result of an arithmetic or logic operation is zero; otherwise Z is cleared.
3	OV	OV is set if the operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
4	PDF	PDF is cleared by system power-up or executing the ″CLR WDT″ instruction. PDF is set by executing the ″HALT″ instruction.
5	TO	TO is cleared by system power-up or executing the ″CLR WDT″ or ″HALT″ instruction. TO is set by a WDT time-out.
6~7	—	Unused bit, read as ″0″

Status (0AH) Register

Interrupt

The devices provides two external interrupts, one internal 8-bit timer/event counter interrupt and one external RC oscillation converter interrupt. The interrupt control register 0, INTC0, and interrupt control register 1, INTC1, both contain the interrupt control bits that are used to set the enable/disable and interrupt request flags.

Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the EMI bit will be cleared automatically. However this scheme may prevent further interrupt nesting. Other interrupt requests may happen during this interval but only the interrupt request flag is recorded. If a certain interrupt requires servicing within the service routine, the EMI bit and the corresponding bit of the INTC0 and INTC1 registers may be set to allow interrupt nesting.

If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full.

All interrupts have a wake-up capability. As an interrupt is serviced, a control transfer occurs by pushing the program counter onto the stack, followed by a branch to a subroutine at a specified location in the program memory. Only the program counter is pushed onto the stack. If the contents of the accumulator or status register are altered by the interrupt service program, this may corrupt the desired control sequence, therefore their contents should be saved in advance.

External interrupts are triggered by an edge transition on pins INT0 or INT1. A configuration option enables these pins as interrupts and selects if they are active on high to low or low to high transitions. If active their related interrupt request flag, EIF0; bit 4 in INTC0, and EIF1; bit 5 in INTC0, will be set. After the interrupt is enabled, the stack is not full, and the external interrupt is active, a subroutine call to location ″04H″ or ″08H″ will occur. The interrupt request flags, EIF0 or EIF1, and the EMI bit will all be cleared to disable other interrupts.

The internal Timer/Event Counter interrupt is initialised by setting the Timer/Event Counter interrupt request flag, TF; bit 6 in INTC0. A timer interrupt will be generated when the timer overflows. After the interrupt is enabled, and the stack is not full, and the TF bit is set, a subroutine call to location ″0CH″ will occur. The related interrupt request flag, TF, is reset, and the EMI bit is cleared to disable other interrupts.

The external RC oscillation converter interrupt is initialized by setting the external RC oscillation converter interrupt request flag, RCOCF; bit 4 of INTC1. This is caused by a Timer A or Timer B overflow. When the interrupt is enabled, and the stack is not full and the RCOCF bit is set, a subroutine call to location ″10H″ will occur. The related interrupt request flag, RCOCF, will be reset and the EMI bit cleared to disable further interrupts.

During the execution of an interrupt subroutine, other interrupt acknowledgments are held until the ″RETI″ instruction is executed or the EMI bit and the related interrupt control bit are set to 1, if the stack is not full. To return from the interrupt subroutine, a ″RET″ or ″RETI″ instruction may be invoked. RETI will set the EMI bit to enable an interrupt service, but RET will not.

Bit No.	Label	Function
0	EMI	Controls the master (global) interrupt (1= enabled; 0= disabled)
1	EEI0	Controls the external interrupt 0 (1= enabled; 0= disabled)
2	EEI1	Controls the external interrupt 1 (1= enabled; 0= disabled)
3	ETI	Controls the Timer/Event Counter interrupt (1= enabled; 0= disabled)
4	EIF0	External interrupt 0 request flag (1= active; 0= inactive)
5	EIF1	External interrupt 1 request flag (1= active; 0= inactive)
6	TF	Internal Timer/Event Counter request flag (1= active; 0= inactive)
7	—	Unused bit, read as ″0″

INTC0 (0BH) Register

Bit No.	Label	Function
0	ERCOCI	Controls the external RC oscillation converter interrupt (1= enabled; 0= disabled)
1~3, 5~7	—	Unused bit, read as ″0″
4	RCOCF	External RC oscillation converter request flag (1= active; 0= inactive)

INTC1 (1EH) Register

Interrupts, occurring in the interval between the rising edges of two consecutive T2 pulses, will be serviced on the latter of the two T2 pulses, if the corresponding interrupts are enabled. In the case of simultaneous requests the following table shows the priority that is applied. These can be masked by resetting the EMI bit.

Interrupt Source	Priority	Vector
External Interrupt 0	1	04H
External Interrupt 1	2	08H
Timer/Event Counter Overflow	3	0CH
External RC Oscillation Converter Interrupt	4	10H

Interrupt Priority

The EMI, EEI0, EEI1, ETI and ERCOCI bits are all used to control the enable/disable status of interrupts. These bits prevent the requested interrupt from being serviced. Once the interrupt request flags, TF, RCOCF, EIF1 and EIF0, are all set, they remain in the INTC1 or INTC0 registers respectively until the interrupts are serviced or cleared by a software instruction.

It is recommended that a program does not use the "CALL subroutine" within the interrupt subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately in some applications. If only one stack is left and enabling the interrupt is not well controlled, the original control sequence may be damaged once the "CALL" is executed in the interrupt subroutine.

Oscillator Configuration

Various oscillator options offer the user a wide range of functions according to their various application requirements. Two types of system clocks can be selected while various clock source options for the Watchdog Timer are provided for maximum flexibility. All oscillator options are selected through the configuration options.

The two methods of generating the system clock are:

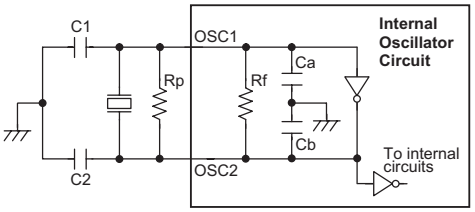
- External crystal/resonator oscillator
- External RC oscillator

One of these two methods must be selected using the configuration options.

More information regarding the oscillator is located in Application Note HA0075E on the Holtek website.

External Crystal/Resonator Oscillator

The simple connection of a crystal across OSC1 and OSC2 will create the necessary phase shift and feedback for oscillation, and will normally not require external capacitors. However, for some crystals and most



Note: 1. Rp is normally not required.
2. Although not shown OSC1/OSC2 pins have a parasitic capacitance of around 7pF.

Crystal/Resonator Oscillator

resonator types, to ensure oscillation and accurate frequency generation, it may be necessary to add two small value external capacitors, C1 and C2. The exact values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer's specification. The external parallel feedback resistor, Rp, is normally not required but in some cases may be needed to assist with oscillation start up.

Internal Ca, Cb, Rf Typical Values @ 5V, 25°C		
Ca	Cb	Rf
TBD	TBD	TBD

Oscillator Internal Component Values

Crystal Oscillator C1 and C2 Values			
Crystal Frequency	C1	C2	CL
12MHz	TBD	TBD	TBD
8MHz	TBD	TBD	TBD
4MHz	TBD	TBD	TBD
1MHz	TBD	TBD	TBD
Note: 1. C1 and C2 values are for guidance only. 2. CL is the crystal manufacturer specified load capacitor value.			

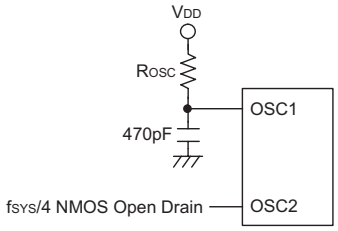
Crystal Recommended Capacitor Values

Resonator C1 and C2 Values		
Resonator Frequency	C1	C2
3.58MHz	TBD	TBD
1MHz	TBD	TBD
455kHz	TBD	TBD
Note: C1 and C2 values are for guidance only.		

Resonator Recommended Capacitor Values

External RC Oscillator

Using the external system RC oscillator requires that a resistor, with a value between 24kΩ and 1.5MΩ, is connected between OSC1 and VDD, and a capacitor is connected to ground. The generated system clock divided by 4 will be provided on OSC2 as an output which can be used for external synchronization purposes. Note that as the OSC2 output is an NMOS open-drain type, a pull high resistor should be connected if it to be used to monitor the internal frequency. Although this is a cost effective oscillator configuration, the oscillation frequency can vary with VDD, temperature and process variations and is therefore not suitable for applications where timing is critical or where accurate oscillator frequencies are required.For the value of the external resistor ROSC refer to the Holtek website for typical RC Oscillator vs. Temperature and VDD characteristics graphics. Note that it is the only microcontroller internal circuitry together with the external resistor, that determine the frequency of the oscillator. The external capacitor shown on the diagram does not influence the frequency of oscillation.



External RC Oscillator

Watchdog Timer Oscillator

The WDT oscillator is a fully self-contained free running on-chip RC oscillator with a typical period of 65μs at 5V requiring no external components. When the device enters the Power Down Mode, the system clock will stop running but the WDT oscillator continues to free-run and to keep the watchdog active. However, to preserve power in certain applications the WDT oscillator can be disabled via a configuration option.

Watchdog Timer – WDT

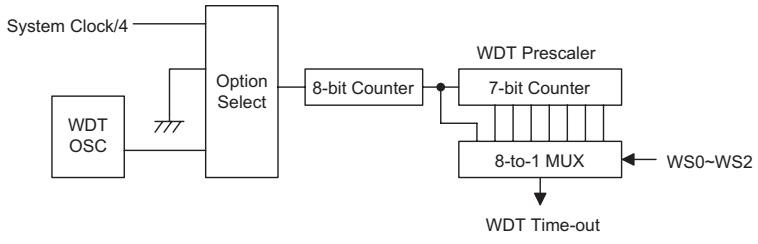
The WDT clock can be sourced from its own dedicated internal oscillator (WDT oscillator), or from the or instruction clock, which is the system clock divided by 4. The choice is determined via a configuration option. The WDT timer is designed to prevent a software malfunction or sequence from jumping to an unknown location with unpredictable results. The Watchdog Timer can be disabled by a configuration option. If the Watchdog Timer is disabled, any executions related to the WDT result in no operation.

The WDT clock source is first divided by 256. If the internal WDT oscillator is used ,this gives a nominal time-out period of approximately 17ms at 5V. This time-out period may vary with temperatures, VDD and process variations. By using the WDT prescaler, longer time-out periods can be realised. Writing data to the WS2, WS1, WS0 bits in the WDTS register, can give different time-out periods. If WS2, WS1 and WS0 are all equal to 1, the division ratio will be 1:128, and the maximum time-out period will be 2.1s at 5V. If the internal WDT oscillator is disabled, the WDT clock may still come from the instruction clock and operate in the same manner except that in the Power Down state the WDT will stop counting and lose its protecting purpose. The high nibble and bit 3 of the WDTS can be used for user defined flags.

If the device operates in a noisy environment, using the internal WDT oscillator is the recommended choice, since the HALT instruction will stop the system clock.

WS2	WS1	WS0	Division Ratio
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

WDTS (09H) Register



Watchdog Timer

The WDT overflow under normal operation will generate a ″chip reset″ and set the status bit ″TO″. But in the Power Down mode, the overflow will generate a ″warm reset″, where only the Program Counter and Stack Pointer are reset to zero. To clear the contents of the WDT, including the WDT prescaler, three methods can be used; an external reset (a low level to $\overline{RES}$), a software instruction and a ″HALT″ instruction. The software instruction includes ″CLR WDT″ instruction and the instruction pair – ″CLR WDT1″ and ″CLR WDT2″. Of these two types of instruction, only one can be active depending on the configuration option – ″CLR WDT times selection option″. If the ″CLR WDT″ is selected, i.e. CLRWDT times equal one, any execution of the ″CLR WDT″ instruction will clear the WDT. In the case that ″CLR WDT1″ and ″CLR WDT2″ are chosen, i.e. CLRWDT times equal two, these two instructions must be executed to clear the WDT; otherwise, the WDT may reset the chip as a result of a time-out.

Power Down Operation

The Power Down mode is initialized by the ″HALT″ instruction and results in the following...

- The system oscillator will be turned off but the WDT oscillator keeps running, if the internal WDT oscillator has been selected as the WDT source clock.
- The contents of the on chip RAM and registers remain unchanged.
- The WDT and WDT prescaler will be cleared and will resume counting, if the internal WDT oscillator has been selected as the WDT source clock
- All of the I/O ports will maintain their original status.
- The PDF flag is set and the TO flag is cleared.

The system can leave the Power Down mode by means of an external reset, an interrupt, an external falling edge signal on port A or a WDT overflow. An external reset causes a device initialisation and the WDT overflow performs a ″warm reset″. After the TO and PDF flags are examined, the reason for the device reset can be determined. The PDF flag is cleared by a system power-up or executing the ″CLR WDT″ instruction and is set when a ″HALT″ instruction is executed. The TO flag is set if a WDT time-out occurs, and causes a wake-up that only resets the program counter and stack pointer; the other registers maintain their their original status.

The port A and interrupt methods of wake-up can be considered as a continuation of normal execution. Each bit in port A can be independently selected by configuration options to wake-up the device. When awakened from an I/O port stimulus, the program will resume execution at the next instruction. If it is awakened due to an interrupt, two sequences may happen. If the related interrupt is disabled or the interrupt is enabled but the stack is full, the program will resume execution at the next instruction. If the interrupt is enabled and the stack is not full, the regular interrupt response takes place. If an interrupt request flag is set to ″1″ before entering the Power Down Mode, the wake-up function of the related interrupt will be disabled. Once a wake-up event occurs, it takes 1024 t_{SYS} (system clock periods) to resume normal operation. A dummy period is therefore inserted after wake-up. If the wake-up results from an interrupt acknowledgment, the actual interrupt subroutine execution will be delayed by one or more cycles. If the wake-up results in the next instruction execution, this will be executed immediately after the dummy period is finished.

To minimise power consumption, all the I/O pins should be carefully managed before entering the Power Down mode.

Reset

There are three ways in which a reset can occur:

- $\overline{RES}$ reset during normal operation
- $\overline{RES}$ reset during HALT
- WDT time-out reset during normal operation

A WDT time-out, when the device is in the Power Down mode, is different from other device reset conditions, in that it can perform a "warm reset" that resets only the Program Counter and the Stack Poiner, leaving the other circuits in their original state. Some registers remain unchanged during other reset conditions. Most registers are reset to their "initial condition" when the reset conditions are met. By examining the PDF and TO flags, the program can distinguish between the different device reset types.

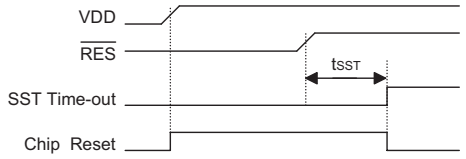
TO	PDF	RESET Conditions
0	0	$\overline{RES}$ reset during power-up
u	u	$\overline{RES}$ reset during normal operation
0	1	$\overline{RES}$ wake-up HALT
1	u	WDT time-out during normal operation
1	1	WDT wake-up HALT

Note: "u" means "unchanged"

To guarantee that the system oscillator is started and stabilised, the SST or System Start-up Timer, provides an extra-delay of 1024 system clock pulses when the system is reset (power-up, WDT time-out or $\overline{RES}$ reset) or when the system awakens from a Power Down state.

When a system reset occurs, the SST delay is added during the reset period. Any wake-up the Power Down mode will enable the SST delay.

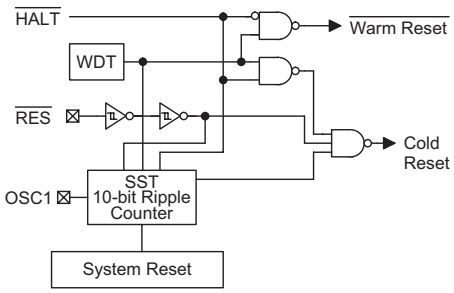
An extra option load time delay is added during a system reset (power-up, WDT time-out during normal mode or a $\overline{RES}$ reset).



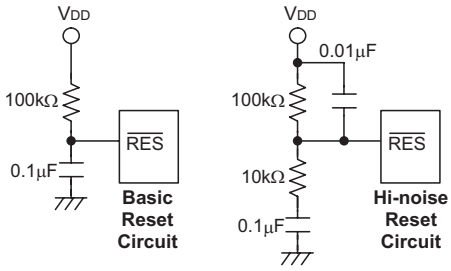
Reset Timing Chart

The functional unit device reset status are shown below.

Program Counter	000H
Interrupt	Disable
Prescaler	Clear
WDT	Clear. After master reset, WDT begins counting
Timer/Event Counter	Off
Input/Output Ports	Input mode
Stack Pointer	Points to the top of the stack



Reset Configuration



Reset Circuit

Note: Most applications can use the Basic Reset Circuit as shown, however for applications with extensive noise, it is recommended to use the Hi-noise Reset Circuit.

The states of the registers is summarized in the table.

Register	Reset (Power-on)	WDT Time-out (Normal Operation)	$\overline{RES}$ Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*
MP0	-xxx xxxx	-uuu uuuu	-uuu uuuu	-uuu uuuu	-uuu uuuu
MP1	-xxx xxxx	-uuu uuuu	-uuu uuuu	-uuu uuuu	-uuu uuuu
BP	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
Program Counter	000H	000H	000H	000H	000H
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	--xx xxxx	--uu uuuu	--uu uuuu	--uu uuuu	--uu uuuu
WDTS	0000 0111	0000 0111	0000 0111	0000 0111	uuuu uuuu
STATUS	--00 xxxx	--1u uuuu	--uu uuuu	--01 uuuu	--11 uuuu
INTC0	-000 0000	-000 0000	-000 0000	-000 0000	-uuu uuuu
TMR	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRC	00-0 1000	00-0 1000	00-0 1000	00-0 1000	uu-u uuuu
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PB	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PBC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
ASCR0	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
ASCR1	---- 1111	---- 1111	---- 1111	---- 1111	---- uuuu
ASCR2	--11 1111	--11 1111	--11 1111	--11 1111	--uu uuuu
INTC1	---0 ---0	---0 ---0	---0 ---0	---0 ---0	---u ---u
TMRAH	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRAL	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
RCOCCR	0000 1---	0000 1---	0000 1---	0000 1---	uuuu u---
TMRBH	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRBL	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
RCOCR	1xxx --00	1xxx --00	1xxx --00	1xxx --00	uuuu --uu

Note: "*" means "warm reset"
"u" means "unchanged"
"x" means "unknown"
"-" stands for unimplemented

If the configuration options select PA0~PA7 to be RC inputs, then the corresponding bits in the PA data register and PA control register will be unimplemented and will be read as zero.

If the configuration options select PA0~PA7 to be normal I/O pins, then bit 0~bit3 in the ASCR0 and ASCR1 registers will be unimplemented and will be read as zero.

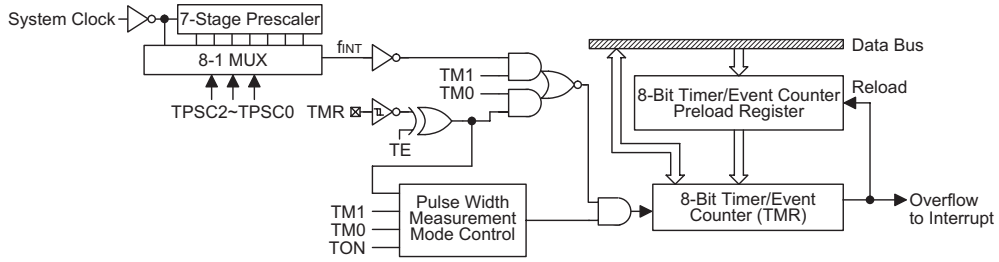
Timer/Event Counter

An 8-bit timer/event counter, known as Timer/Event Counter, is implemented in the microcontroller. The Timer/Event Counter contains an 8-bit programmable count-up counter whose clock may come from an external source or from the system clock. Using the external clock input allows the user to count external events, measure time internals or pulse widths, or generate an accurate time base. Using the internal clock allows the user to generate an accurate time base.

There are 2 registers related to the Timer/Event Counter, TMR and TMRC. Two physical registers are mapped to the TMR location; writing to TMR places the start value of the Timer/Event Counter in a preload register while reading TMR retrieves the contents of the Timer/Event Counter. The TMRC is a timer/event counter control register, which defines the timer operating conditions.

The TM0, TM1 bits define the operating mode. The event count mode is used to count external events, which means the clock source comes from an external TMR pin. The timer mode functions as a normal timer with the clock source coming from the f_{INT} clock. The pulse width measurement mode can be used to measure the high or low level duration of an external signal on the TMR pin. The counting is based on the f_{INT} clock source. In the event counting or timer mode, once the timer/event counter starts counting, it will count from the current contents in the Timer/Event Counter to FFH. Once overflow occurs, the counter is reloaded from the Timer/Event Counter preload register and an interrupt request flag TF; bit 5 of INTC0, is generated at the same time.

In the pulse width measurement mode, with the TON and TE bits equal to one, once the TMR pin has received a transient from low to high, or high to low if the TE bit is 0, it will start counting until the TMR pin returns to its original level and resets the TON bit. The measured result will remain in the Timer/Event Counter even if the activated transient occurs again. Therefore, only a single shot measurement can be made. The TON bit must be set again by software for further measurements



Timer/Event Counter

Bit No.	Label	Function
0~2	TPSC0~TPSC2	To define the prescaler stages, TPSC2, TPSC1, TPSC0= 000: $f_{INT}=f_{SYS}$ 001: $f_{INT}=f_{SYS}/2$ 010: $f_{INT}=f_{SYS}/4$ 011: $f_{INT}=f_{SYS}/8$ 100: $f_{INT}=f_{SYS}/16$ 101: $f_{INT}=f_{SYS}/32$ 110: $f_{INT}=f_{SYS}/64$ 111: $f_{INT}=f_{SYS}/128$
3	TE	To define the TMR active edge of the timer/event counter (0=active on low to high; 1=active on high to low)
4	TON	To enable or disable timer counting (0=disabled; 1=enabled)
5	—	Unused bit, read as ″0″
6 7	TM0 TM1	To define the operating mode, TM1, TM0= 01=Event count mode (external clock) 10=Timer mode (internal clock) 11=Pulse width measurement mode 00=Unused

TMRC (0EH) Register

to be made. Note that, in this operating mode, the Timer/Event Counter starts counting not according to the logic level but according to the transient edges. In the case of a counter overflow, the counter is reloaded from the Timer/Event Counter preload register and issues an interrupt request just like the other two modes.

To enable a counting operation, the Timer ON bit, TON; bit 4 of TMRC, should be set to "1". In the pulse width measurement mode, the TON will be cleared automatically after the measurement cycle is completed. But in the other two modes, the TON can only be reset by instructions. The Timer/Event Counter overflow is one of the wake-up sources. No matter what the operation mode is, writing a 0 to ETI can disable the interrupt service.

If the Timer/Event Counter is switched off, then writing data to the Timer/Event Counter preload register will also directly reload that data to the Timer/Event Counter. But if the Timer/Event Counter is already running, data written to it will only be loaded into the Timer/Event Counter preload register. The Timer/Event Counter will continue to operate until an overflow occurs. When the Timer/Event Counter is read, the clock will be blocked to avoid errors. As clock blocking may results in a counting error, this must be taken into consideration by the programmer. Bit0~Bit2 of the TMRC register can be used to define the pre-scaling stages of the internal clock source of the Timer/Event Counter.

External RC Oscillation Converter

An external RC oscillation mode is implemented in the device. The RC oscillation converter contains two 16-bit programmable count-up counters.

The RC oscillation converter is comprised of the TMRAL, TMRAH, TMRBL, TMRBH registers when the RCO bit, bit 1 of RCOCR register, is "1". The RC oscillation converter Timer B clock source may come from an external RC oscillator. The Timer A clock source comes from the system clock or from the system clock/4, determined by the RCOCCR register.

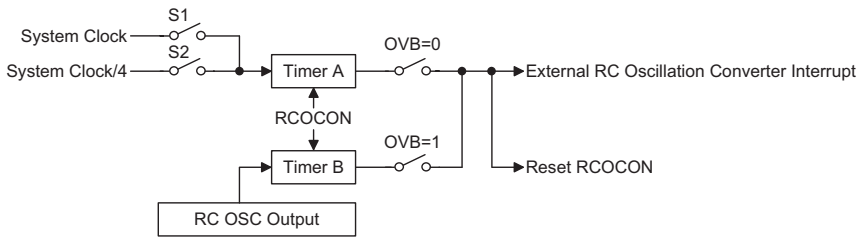
There are six registers related to the RC oscillation converter, i.e., TMRAH, TMRAL, RCOCCR, TMRBH, TMRBL and RCOCR. The internal timer clock is the input to TMRAH and TMRAL, the external RC oscillation is the input to TMRBH and TMRBL. The OVB bit, bit 0 of the RCOCR register, decides whether Timer A overflows or Timer B overflows, then the RCOCF bit is set and an external RC oscillation converter interrupt occurs. When the RC oscillation converter mode Timer A or Timer B overflows, the RCOCON bit is reset to "0" and stops counting. Writing to TMRAH/TMRBH places the start value in Timer A/Timer B while reading TMRAH/TMRBH obtains the contents of Timer A/Timer B. Writing to TMRAL/TMRBL only writes the data into a low byte buffer. However writing to TMRAH/TMRBH will write the data and the contents of the low byte buffer into

Bit No.	Label	Function
0~2	—	Unused bit, read as "0"
3	—	Undefined bit, this bit can read/write
4	RCOCON	Enable or disable external RC oscillation converter counting (0=disabled; 1=enabled)
5 6 7	RCOM0 RCOM1 RCOM2	Define the Timer A clock source, RCOM2, RCOM1, RCOM0= 000=System clock 001=System clock/4 010=Unused 011=Unused 100=Unused 101=Unused 110=Unused 111=Unused

RCOCCR (22H) Register

Bit No.	Label	Function
0	OVB	In the RC oscillation converter mode, this bit is used to define the timer/event counter interrupt, which comes from Timer A overflow or Timer B overflow. (0=Timer A overflow; 1=Timer B overflow)
1	RCO	Define RC oscillation converter mode. (0=Disable RC oscillation converter mode; 1=Enable RC oscillation converter mode)
2~3	—	Unused bit, read as "0"
4~7	RW	4-bit read/write registers for user defined.

RCOCR (25H) Register



External RC Oscillation Converter

the Timer A/Timer B (16-bit) simultaneously. Timer A/Timer B is changed by writing to TMRAH/TMRBH but writing to TMRAL/TMRBL will keep the Timer A/Timer B unchanged.

Reading TMRAH/TMRBH will also latch the TMRAL/TMRBL into the low byte buffer to avoid false timing problem. Reading TMRAL/TMRBL returns the contents of the low byte buffer. Therefore, the low byte of Timer A/Timer B can not be read directly. It must read TMRAH/TMRBH first to ensure that the low byte contents of Timer A/Timer B are latched into the buffer.

The resistor and capacitor form an oscillation circuit and input to TMRBH and TMRBL. The RCOM0, RCOM1 and RCOM2 bits of RCOCCR define the clock source of Timer A. It is recommended that the clock source of Timer A uses the system clock or the instruction clock.

If the RCOCON bit, bit 4 of RCOCCR, is set to "1", Timer A and Timer B will start counting until Timer A or Timer B overflows, the timer/event counter will then generate an interrupt request flag which is RCOCF; bit 4 of INTC1. The Timer A and Timer B will stop counting and will reset the RCOCON bit to "0" at the same time. If the RCOCON bit is "1", TMRAH, TMRAL, TMRBH and TMRBL cannot be read or written.

External RC oscillation converter mode example program - Timer A overflow:

```
clr RCOCCR
mov a, 00000010b              ; Enable External RC oscillation mode and set Timer A overflow
mov RCOCR,a
clr intc1.4                   ; Clear External RC Oscillation Converter interrupt request flag
mov a, low (65536-1000)       ; Give timer A initial value
mov tmral, a                  ; Timer A count 1000 time and then overflow
mov a, high (65536-1000)
mov tmrah, a
mov a, 00h                    ; Give timer B initial value
mov tmrbl, a
mov a, 00h
mov tmrbh, a
mov a, 00110000b              ; Timer A clock source=fSYS/4 and timer on
mov RCOCCR, a
p10:
clr wdt
snz intc1.4                   ; Polling External RC Oscillation Converter interrupt request flag
jmp p10
clr intc1.4                   ; Clear External RC Oscillation Converter interrupt request flag
                              ; Program continue
```

Analog Switch

There are 12 analog switch lines in the device for RC1~RC12, and three corresponding Analog Switch Control registers, which are ASCR0, ASCR1 and ASCR2.

If the configuration options select PA0~PA3 to be normal I/O pins, then the corresponding bit 0~bit3 bits in the ASCR0 register will be unimplemented and will be read as zero.

Bit No.	Label	Function
0	AS1ON	Defines RC1 analog switch is on or off. AS1ON= 0=Analog switch 1 on, and RC1 is disconnected to pull-low 1=Analog switch 1 off, and RC1 is connected to pull-low or not according ASPLON0 register
1	AS2ON	Defines RC2 analog switch is on or off. AS2ON= 0=Analog switch 2 on, and RC2 is disconnected to pull-low 1=Analog switch 2 off, and RC2 is connected to pull-low or not according ASPLON0 register
2	AS3ON	Defines RC3 analog switch is on or off. AS3ON= 0=Analog switch 3 on, and RC3 is disconnected to pull-low 1=Analog switch 3 off, and RC3 is connected to pull-low or not according ASPLON1 register
3	AS4ON	Defines RC4 analog switch is on or off. AS4ON= 0=Analog switch 4 on, and RC4 is disconnected to pull-low 1=Analog switch 4 off, and RC4 is connected to pull-low or not according ASPLON1 register
4	AS5ON	Defines RC5 analog switch is on or off. AS5ON= 0=Analog switch 5 on, and RC5 is disconnected to pull-low 1=Analog switch 5 off, and RC5 is connected to pull-low or not according ASPLON2 register
5	AS6ON	Defines RC6 analog switch is on or off. AS6ON= 0=Analog switch 6 on, and RC6 is disconnected to pull-low 1=Analog switch 6 off, and RC6 is connected to pull-low or not according ASPLON2 register
6	AS7ON	Defines RC7 analog switch is on or off. AS7ON= 0=Analog switch 7 on, and RC7 is disconnected to pull-low 1=Analog switch 7 off, and RC7 is connected to pull-low or not according ASPLON3 register
7	AS8ON	Defines RC8 analog switch is on or off. AS8ON= 0=Analog switch 8 on, and RC8 is disconnected to pull-low 1=Analog switch 8 off, and RC8 is connected to pull-low or not according ASPLON3 register

ASCR0 (1AH) Register

If the configuration options select PA4~PA7 to be normal I/O pins, then the corresponding bit 0~bit3 bits in the ASCR1 register will be unimplemented and will be read as zero.

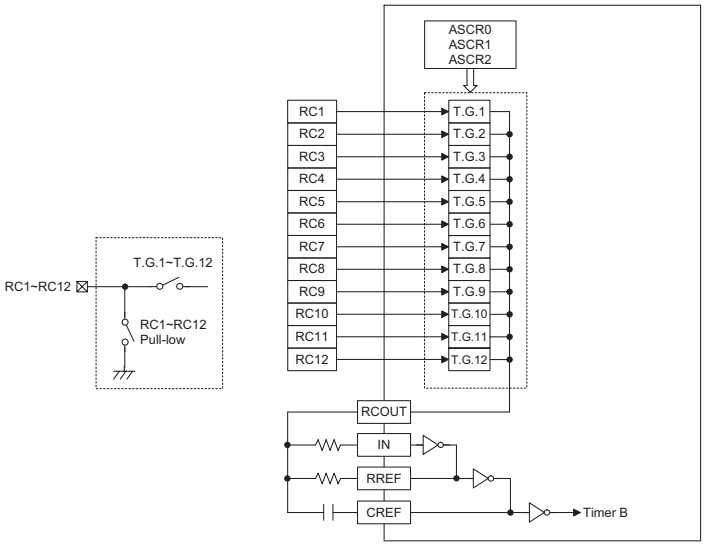
Bit No.	Label	Function
0	AS9ON	Defines RC9 analog switch is on or off. AS9ON= 0=Analog switch 9 on, and RC9 is disconnected to pull-low 1=Analog switch 9 off, and RC9 is connected to pull-low or not according ASPLON4 register
1	AS10ON	Defines RC10 analog switch is on or off. AS10ON= 0=Analog switch 10 on, and RC10 is disconnected to pull-low 1=Analog switch 10 off, and RC10 is connected to pull-low or not according ASPLON4 register
2	AS11ON	Defines RC11 analog switch is on or off. AS11ON= 0=Analog switch 11 on, and RC11 is disconnected to pull-low 1=Analog switch 11 off, and RC11 is connected to pull-low or not according ASPLON5 register
3	AS12ON	Defines RC12 analog switch is on or off. AS12ON= 0=Analog switch 12 on, and RC12 is disconnected to pull-low 1=Analog switch 12 off, and RC12 is connected to pull-low or not according ASPLON5 register
4~7	—	Unused bit, read as ″0″

ASCR1 (1BH) Register

If the configuration options select PA0~PA7 to be normal I/O pins, then the corresponding bits in the ASCR2 register, bit 0, bit1, bit4 and bit5, must be set to "0" to disable the RC1/RC2, RC3/RC4, RC9/RC10 or RC11/RC12 pull-low resistors. These bits are set to "0" or "1" by software.

Bit No.	Label	Function
0	ASPLON0	Defines RC1 pull-low and RC2 pull-low is non-pull-low. ASPLON0= 0=RC1 and RC2 are non-pull-low 1=RC1 and RC2 are pull-low or not according RC1, RC2 analog is on or off. RC1/RC2 is connected to pull-low when ASPLON0=1 and AS1ON/AS2ON analog switch is off.
1	ASPLON1	Defines RC3 pull-low and RC4 pull-low is non-pull-low. ASPLON1= 0=RC3 and RC4 are non-pull-low 1=RC3 and RC4 are pull-low or not according RC3, RC4 analog is on or off. RC3/RC4 is connected to pull-low when ASPLON1=1 and AS3ON/AS4ON analog switch is off.
2	ASPLON2	Defines RC5 pull-low and RC6 pull-low is non-pull-low. ASPLON2= 0=RC5 and RC6 are non-pull-low 1=RC5 and RC6 are pull-low or not according RC5, RC6 analog is on or off. RC5/RC6 is connected to pull-low when ASPLON2=1 and AS5ON/AS6ON analog switch is off.
3	ASPLON3	Defines RC7 pull-low and RC8 pull-low is non-pull-low. ASPLON3= 0=RC7 and RC8 are non-pull-low 1=RC7 and RC8 are pull-low or not according RC7, RC8 analog is on or off. RC7/RC8 is connected to pull-low when ASPLON3=1 and AS7ON/AS8ON analog switch is off.
4	ASPLON4	Defines RC9 pull-low and RC10 pull-low is non-pull-low. ASPLON4= 0=RC9 and RC10 are non-pull-low 1=RC9 and RC10 are pull-low or not according RC9, RC10 analog is on or off. RC9/RC10 is connected to pull-low when ASPLON4=1 and AS9ON/AS10ON analog switch is off.
5	ASPLON5	Defines RC11 pull-low and RC12 pull-low is non-pull-low. ASPLON5= 0=RC11 and RC12 are non-pull-low 1=RC11 and RC12 are pull-low or not according RC11, RC12 analog is on or off. RC11/RC12 is connected to pull-low when ASPLON5=1 and AS11ON/AS12ON analog switch is off.
6~7	—	Unused bit, read as "0"

ASCR2 (1CH) Register



Analog Switch

Input/Output Ports

There are 9 bidirectional input/output lines in the microcontroller, all located within port PA and PB. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, that is, the inputs must be ready at the T2 rising edge of the "MOV A,[m]" instruction. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Each I/O line has its own control register, known as PAC and PBC, to control the input/output configuration. With this control register, the pin status is either a CMOS output or a Schmitt trigger input, but can be reconfigured dynamically, under software control. To function as an input, the corresponding bit in the control register must be written with a "1". The input source also depends on the control register. If the control register bit is "1", the input will read the pad state. If the control register bit is "0", the contents of the latches will move to the internal bus. The latter is possible in the read-modify-write instruction.

When setup as an output the output types are CMOS.

After a device reset, the I/O ports will be initially all setup as inputs, and will therefore be in a high state if the configuration options have selected pull-high resistors, otherwise they will be in a floating condition. Each bit of these input/output latches can be set or cleared by the "SET [m].i" and "CLR [m].i" instructions.

Some instructions first input data and then follow the output operations. For example, "SET [m].i", "CLR [m].i", "CPL [m]", "CPLA [m]" read the entire port states into the CPU, execute the defined operations (bit-operation), and then write the results back to the latches or the accumulator.

Each line of port A has the capability of waking-up the device.

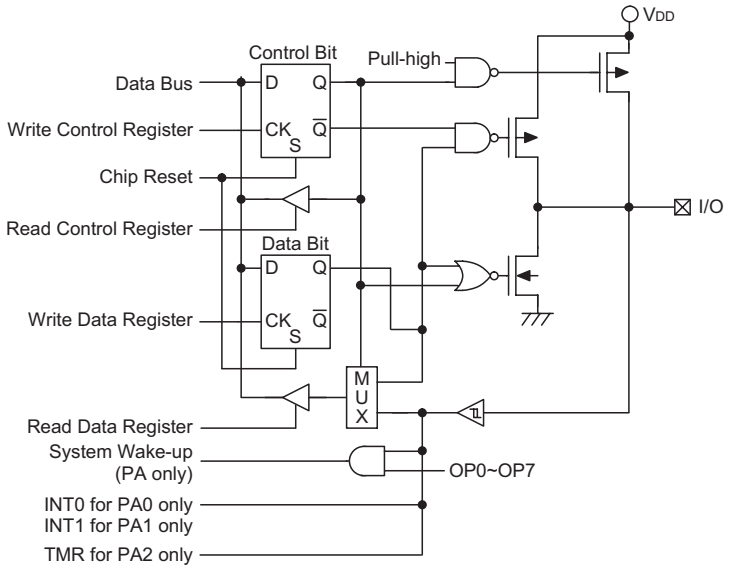
Each line of port A and port B has a pull-high option. Once the pull-high option is selected, the I/O line will have a pull-high resistor connected. Otherwise, the pull-high resistors are absent. It should be noted that a non-pull-high I/O line operating in an input mode will be in a floating state.

The PA0, PA1 and PA2 are pin-shared with INT0, INT1 and TMR pins, respectively. Pins PA0~PA3 and PA4~PA7 are pin-shared with RC1~RC4 and RC9~RC12, respectively. If configuration options select PA0~PA7 to be RC input pins, then the corresponding bits in the PA data register and PA control register will be unimplemented.

It is recommended that unused or not bonded out I/O lines should be set as output pins using software instruction to avoid consuming power under input floating state.

VFD Driver

The device includes a VFD driver function to drive VFD panel high voltage filaments and buzzer. The microcontroller communicates serially with the VFD driver transmitting the display data into a 24-bit shift register within the driver. This VFD driver converts the shift register into VFD panel driving signals and makes the necessary voltage level shifting. The microcontroller will only transmit data to the VFD driver, no data is transmitted from the VFD driver to the microcontroller.



Input/Output Ports

VFD Interface

A five line interface exists between the microcontroller and the VFD driver as shown in the diagram.

Data transmission between the microcontroller and the VFD interface is conducted via a three line interface using the CLK, DATA and STROBE lines. As data communication is only one way the microcontroller I/O pins must bet setup as outputs.

The buzzer control input BZI will be transformed into a complementary pair of outputs BZO and $\overline{BZO}$ by a converter in the VFD driver. These complementary buzzer outputs will also be level shifted to a higher voltage by the converter. The VFD driver filament control input, F1, will also be shifted to a high voltage output called F1O, that can be used to switch the filaments on and off.

24-bit Shift Register/Latch

Data transmitted from the microcontroller is transmitted serially and will be first written into a 24-bit shift register located within the VFD driver. These 24-bits are used to control the VFD panel segments, VFD0~VFD15, and grid, VFD16~VFD23, lines. The control method is as follows:

- Use the ″DATA″ and ″CLK″ lines to shift data into the internal 24-bit shift register. Data is clocked into the shift-register on the positive clock edge. This data corresponds to the desired VFD0~VFD23 output display data. The VFD outputs will only change if the STROBE line is high. If the STROBE line is low, only the shift register data will be modified and the VFD outputs will remain the same.
- Use the ″STROBE″ line to latch the shift-register data to the VFD0~VFD23 outputs. When the STROBE line is high, the shift register data will be latched to the VFD lines. Note that the STROBE line is level and not edge triggered.

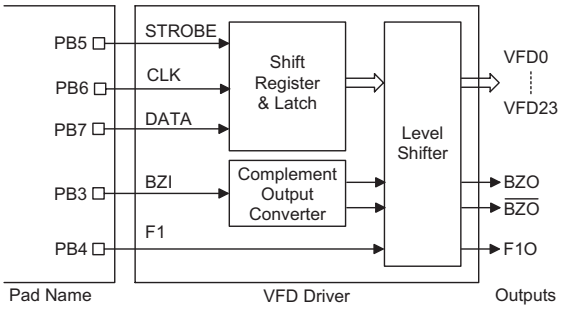
The accompanying table shows the 24-bit shift register/latch function truth table:

Clock	Strobe	Data	VFD0	VFDn
↑	0	X	No change	No change
↑	1	0	0	VFDn-1
↑	1	1	1	VFDn-1
↓	1	1	No change	No change

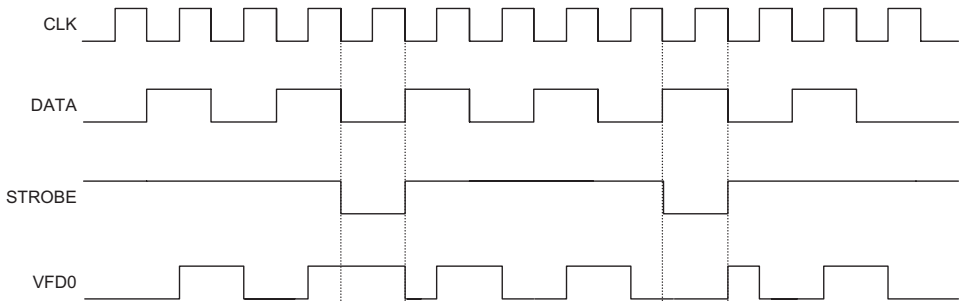
Note: ″X″ means don't care
″VFDn″ means VFD1~VFD23

Programming Considerations

After power on all the I/O lines will be automatically setup as inputs. However as lines PB3~PB7 are used to drive the VFD and buzzer interface, they should be setup as outputs after power is applied to the device. Allowing the VFD interface control lines to be setup as inputs will create an incorrect VFD display and buzzer operation. It is advised that the configuration options select pull-high resistors to be connected to these lines to keep the lines at a fixed high level when power is initially applied and until the lines can be setup as outputs.



VFD Driver



VFD Display Control Timing Diagram

Programming Example

The following example shows how the VFD display data is programmed by the microcontroller.

```
strobe      equ pb.5
clk         equ pb.6
data        equ pb.7
data_2_register:       ; send data to vfd driver
     mov    a,024d     ; shift register counter
     mov    count,a
     clr    strobe     ; strobe = 0
data_2_register_1:
     clr    clk        ; clk = 0
     set    data       ; data = 1
     snz    vfd_grid.7
     clr    data       ; data = 0
     rlc    vfd_segl   ; shift data to vfd[7:0]
     rlc    vfd_segh   ; shift data to vfd[15:8]
     rlc    vfd_grid   ; shift data to vfd[22:16]
     set    clk        ; clk = 1 (rising edge)
     sdz    count
     jmp    data_2_register_1
     set    strobe     ; strobe = 1, vfd output
     ret
```

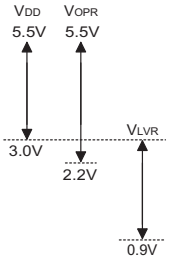
Low Voltage Reset – LVR

The microcontroller provides a low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V~V_{LVR}, such as when changing a battery, the LVR will automatically reset the device internally.

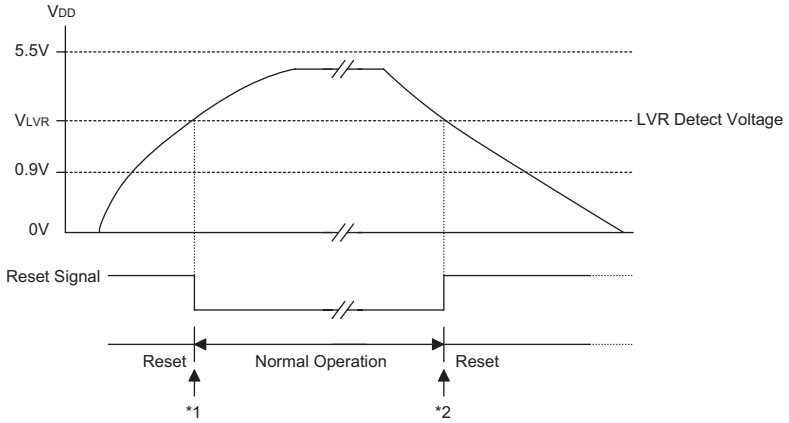
The LVR includes the following specifications:

- The low voltage (0.9V~V_{LVR}) has to remain in its original state for longer than t_{LVR}. If the low voltage state does not exceed t_{LVR}, the LVR will ignore it and will not perform a reset function.
- The LVR uses an "OR" function with the external $\overline{RES}$ signal to perform a chip reset.

The relationship between V_{DD} and V_{LVR} is shown below.



Note: V_{OPR} is the voltage range for proper chip operation at 4MHz system clock.



Low Voltage Reset

Note: *1: To make sure that the system oscillator has stabilized, the SST provides an extra delay of 1024 system clock pulses before starting the normal operation.

*2: Since low voltage has to be maintained its original state for longer than t_{LVR}, therefore a t_{LVR} delay enters the reset mode.

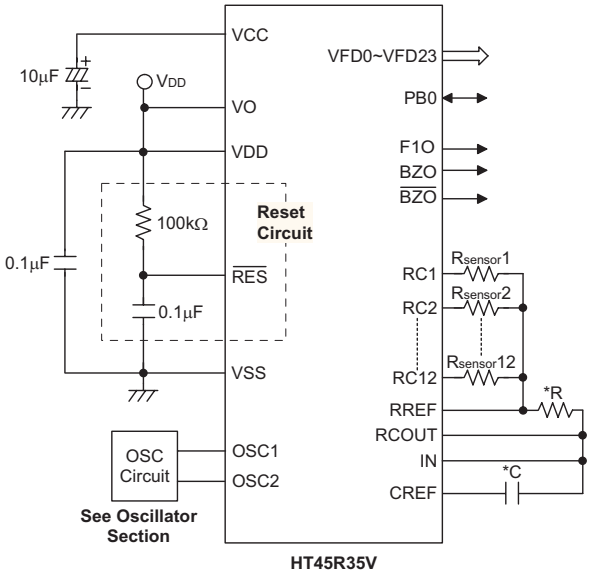
Options

The following table shows the various options within the microcontroller. All of the options must be defined to ensure proper system functioning.

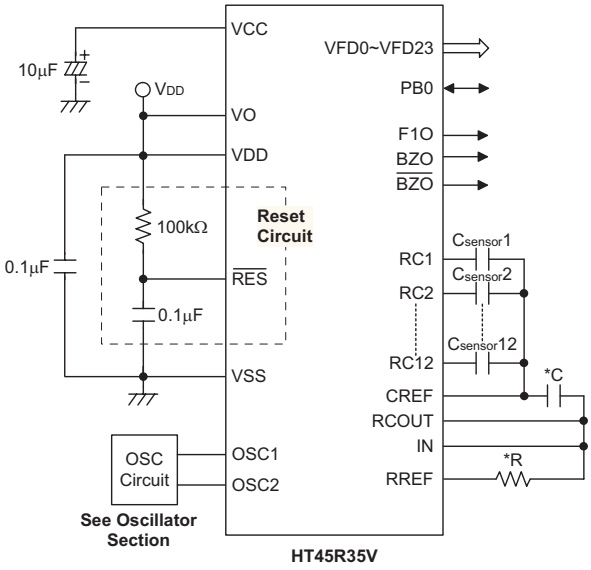
No.	Function	Description
1	Wake up PA0~PA7 (bit option)	None wake-up or wake-up
2	Pull high PA0~PA7, PB0 and PB3~PB7 (bit option)	None pull-high or pull-high
3	WDT clock source	WDTOSC or $f_{SYS}/4$
4	WDT	Enable or disable
5	CLRWDT	1 or 2 instructions
6	LVR	Enable or disable
7	OSC	X′tal mode or RC mode
8	INT0 trigger edge	Disable, rising edge, falling edge or double edge
9	INT1 trigger edge	Disable, rising edge, falling edge or double edge
10	I/O or RC connection pins	PA0 or RC1, PA1 or RC2, PA2 or RC3, PA3 or RC4, PA4 or RC9, PA5 or RC10, PA6 or RC11, PA7 or RC12

Application Circuits

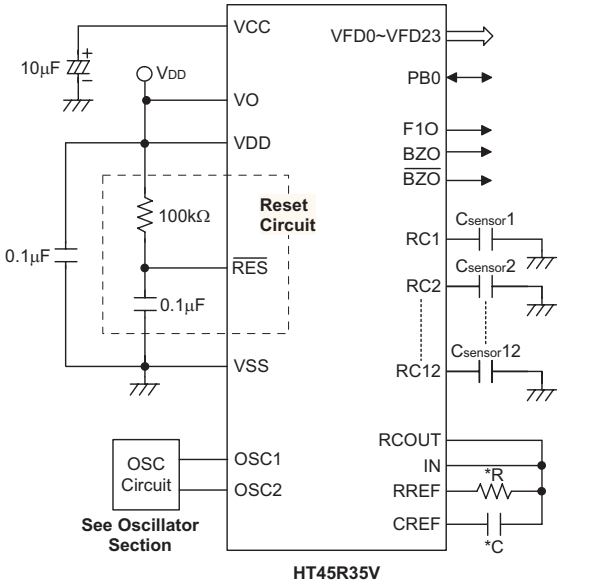
R to F Application Circuit



C to F Application Circuit 1



C to F Application Circuit 2



Note: 1. The "*R" resistance and "*C" capacitance should be consideration for the frequency of RC OSC.

2. $R_{sensor}1$~$R_{sensor}12$ are the resistance sensors.

3. $C_{sensor}1$~$C_{sensor}12$ are the capacitance sensors.

Instruction Set

Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontrollers, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5μs and branch or call instructions would be implemented within 1μs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be ″CLR PCL″ or ″MOV PCL, A″. For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

Logical and Rotate Operations

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application where rotate data operations are used is to implement multiplication and division calculations.

Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction RET in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

Instruction Set Summary

The following table depicts a summary of the instruction set categorised according to function and can be consulted as a basic instruction reference using the following listed conventions.

Table conventions:

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV
ADDM A,[m]	Add ACC to Data Memory	1Note	Z, C, AC, OV
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV
ADCM A,[m]	Add ACC to Data memory with Carry	1Note	Z, C, AC, OV
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	1Note	Z, C, AC, OV
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	1Note	Z, C, AC, OV
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	1Note	C
Logic Operation			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	1Note	Z
ORM A,[m]	Logical OR ACC to Data Memory	1Note	Z
XORM A,[m]	Logical XOR ACC to Data Memory	1Note	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	1Note	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	1Note	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	1Note	Z

Mnemonic	Description	Cycles	Flag Affected
Rotate			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	1Note	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	1Note	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	1Note	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	1Note	C
Data Move			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	1Note	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of Data Memory	1Note	None
SET [m].i	Set bit of Data Memory	1Note	None
Branch			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	1Note	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	1note	None
SZ [m].i	Skip if bit i of Data Memory is zero	1Note	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	1Note	None
SIZ [m]	Skip if increment Data Memory is zero	1Note	None
SDZ [m]	Skip if decrement Data Memory is zero	1Note	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	1Note	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	1Note	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
Table Read			
TABRDC [m]	Read table (current page) to TBLH and Data Memory	2Note	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2Note	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	1Note	None
SET [m]	Set Data Memory	1Note	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer	1	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	1Note	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.
2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.
3. For the ″CLR WDT1″ and ″CLR WDT2″ instructions the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after both ″CLR WDT1″ and ″CLR WDT2″ instructions are consecutively executed. Otherwise the TO and PDF flags remain unchanged.

Instruction Definition

ADC A,[m]	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + [m] + C
Affected flag(s)	OV, Z, AC, C
ADCM A,[m]	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	[m] ← ACC + [m] + C
Affected flag(s)	OV, Z, AC, C
ADD A,[m]	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + [m]
Affected flag(s)	OV, Z, AC, C
ADD A,x	Add immediate data to ACC
Description	The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + x
Affected flag(s)	OV, Z, AC, C
ADDM A,[m]	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	[m] ← ACC + [m]
Affected flag(s)	OV, Z, AC, C
AND A,[m]	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″AND″ [m]
Affected flag(s)	Z
AND A,x	Logical AND immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″AND″ x
Affected flag(s)	Z
ANDM A,[m]	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″AND″ [m]
Affected flag(s)	Z

CALL addr	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack ← Program Counter + 1 Program Counter ← addr
Affected flag(s)	None
CLR [m]	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] ← 00H
Affected flag(s)	None
CLR [m].i	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i ← 0
Affected flag(s)	None
CLR WDT	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT2 and must be executed alternately with CLR WDT2 to have effect. Repetitively executing this instruction without alternately executing CLR WDT2 will have no effect.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT1 and must be executed alternately with CLR WDT1 to have effect. Repetitively executing this instruction without alternately executing CLR WDT1 will have no effect.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

CPL [m] Complement Data Memory

Description Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa.

Operation $[m] \leftarrow \overline{[m]}$

Affected flag(s) Z

CPLA [m] Complement Data Memory with result in ACC

Description Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation $ACC \leftarrow \overline{[m]}$

Affected flag(s) Z

DAA [m] Decimal-Adjust ACC for addition with result in Data Memory

Description Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.

Operation $[m] \leftarrow ACC + 00H$ or
$[m] \leftarrow ACC + 06H$ or
$[m] \leftarrow ACC + 60H$ or
$[m] \leftarrow ACC + 66H$

Affected flag(s) C

DEC [m] Decrement Data Memory

Description Data in the specified Data Memory is decremented by 1.

Operation $[m] \leftarrow [m] - 1$

Affected flag(s) Z

DECA [m] Decrement Data Memory with result in ACC

Description Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.

Operation $ACC \leftarrow [m] - 1$

Affected flag(s) Z

HALT Enter power down mode

Description This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.

Operation $TO \leftarrow 0$
$PDF \leftarrow 1$

Affected flag(s) TO, PDF

INC [m]	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	[m] ← [m] + 1
Affected flag(s)	Z
INCA [m]	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC ← [m] + 1
Affected flag(s)	Z
JMP addr	Jump unconditionally
Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	Program Counter ← addr
Affected flag(s)	None
MOV A,[m]	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	ACC ← [m]
Affected flag(s)	None
MOV A,x	Move immediate data to ACC
Description	The immediate data specified is loaded into the Accumulator.
Operation	ACC ← x
Affected flag(s)	None
MOV [m],A	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	[m] ← ACC
Affected flag(s)	None
NOP	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None
OR A,[m]	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "OR" [m]
Affected flag(s)	Z

OR A,x Logical OR immediate data to ACC

Description: Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.

Operation: ACC ← ACC ″OR″ x

Affected flag(s): Z

ORM A,[m] Logical OR ACC to Data Memory

Description: Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.

Operation: [m] ← ACC ″OR″ [m]

Affected flag(s): Z

RET Return from subroutine

Description: The Program Counter is restored from the stack. Program execution continues at the restored address.

Operation: Program Counter ← Stack

Affected flag(s): None

RET A,x Return from subroutine and load immediate data to ACC

Description: The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.

Operation: Program Counter ← Stack
ACC ← x

Affected flag(s): None

RETI Return from interrupt

Description: The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.

Operation: Program Counter ← Stack
EMI ← 1

Affected flag(s): None

RL [m] Rotate Data Memory left

Description: The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.

Operation: [m].(i+1) ← [m].i; (i = 0~6)
[m].0 ← [m].7

Affected flag(s): None

RLA [m] Rotate Data Memory left with result in ACC

Description: The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation: ACC.(i+1) ← [m].i; (i = 0~6)
ACC.0 ← [m].7

Affected flag(s): None

RLC [m] Rotate Data Memory left through Carry

Description: The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.

Operation:
[m].(i+1) ← [m].i; (i = 0~6)
[m].0 ← C
C ← [m].7

Affected flag(s): C

RLCA [m] Rotate Data Memory left through Carry with result in ACC

Description: Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation:
ACC.(i+1) ← [m].i; (i = 0~6)
ACC.0 ← C
C ← [m].7

Affected flag(s): C

RR [m] Rotate Data Memory right

Description: The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.

Operation:
[m].i ← [m].(i+1); (i = 0~6)
[m].7 ← [m].0

Affected flag(s): None

RRA [m] Rotate Data Memory right with result in ACC

Description: Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation:
ACC.i ← [m].(i+1); (i = 0~6)
ACC.7 ← [m].0

Affected flag(s): None

RRC [m] Rotate Data Memory right through Carry

Description: The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.

Operation:
[m].i ← [m].(i+1); (i = 0~6)
[m].7 ← C
C ← [m].0

Affected flag(s): C

RRCA [m] Rotate Data Memory right through Carry with result in ACC

Description: Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation:
ACC.i ← [m].(i+1); (i = 0~6)
ACC.7 ← C
C ← [m].0

Affected flag(s): C

SBC A,[m] Subtract Data Memory from ACC with Carry

Description The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation ACC ← ACC – [m] – $\overline{C}$

Affected flag(s) OV, Z, AC, C

SBCM A,[m] Subtract Data Memory from ACC with Carry and result in Data Memory

Description The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation [m] ← ACC – [m] – $\overline{C}$

Affected flag(s) OV, Z, AC, C

SDZ [m] Skip if decrement Data Memory is 0

Description The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation [m] ← [m] – 1
Skip if [m] = 0

Affected flag(s) None

SDZA [m] Skip if decrement Data Memory is zero with result in ACC

Description The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.

Operation ACC ← [m] – 1
Skip if ACC = 0

Affected flag(s) None

SET [m] Set Data Memory

Description Each bit of the specified Data Memory is set to 1.

Operation [m] ← FFH

Affected flag(s) None

SET [m].i Set bit of Data Memory

Description Bit i of the specified Data Memory is set to 1.

Operation [m].i ← 1

Affected flag(s) None

SIZ [m] Skip if increment Data Memory is 0

Description The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation [m] ← [m] + 1
Skip if [m] = 0

Affected flag(s) None

SIZA [m] Skip if increment Data Memory is zero with result in ACC

Description The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation ACC ← [m] + 1
Skip if ACC = 0

Affected flag(s) None

SNZ [m].i Skip if bit i of Data Memory is not 0

Description If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.

Operation Skip if [m].i $\neq$ 0

Affected flag(s) None

SUB A,[m] Subtract Data Memory from ACC

Description The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation ACC ← ACC – [m]

Affected flag(s) OV, Z, AC, C

SUBM A,[m] Subtract Data Memory from ACC with result in Data Memory

Description The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation [m] ← ACC – [m]

Affected flag(s) OV, Z, AC, C

SUB A,x Subtract immediate data from ACC

Description The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation ACC ← ACC – x

Affected flag(s) OV, Z, AC, C

SWAP [m]	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	[m].3~[m].0 ↔ [m].7 ~ [m].4
Affected flag(s)	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC.3 ~ ACC.0 ← [m].7 ~ [m].4 ACC.7 ~ ACC.4 ← [m].3 ~ [m].0
Affected flag(s)	None
SZ [m]	Skip if Data Memory is 0
Description	If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if [m] = 0
Affected flag(s)	None
SZA [m]	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	ACC ← [m] Skip if [m] = 0
Affected flag(s)	None
SZ [m].i	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i = 0
Affected flag(s)	None
TABRDC [m]	Read table (current page) to TBLH and Data Memory
Description	The low byte of the program code (current page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

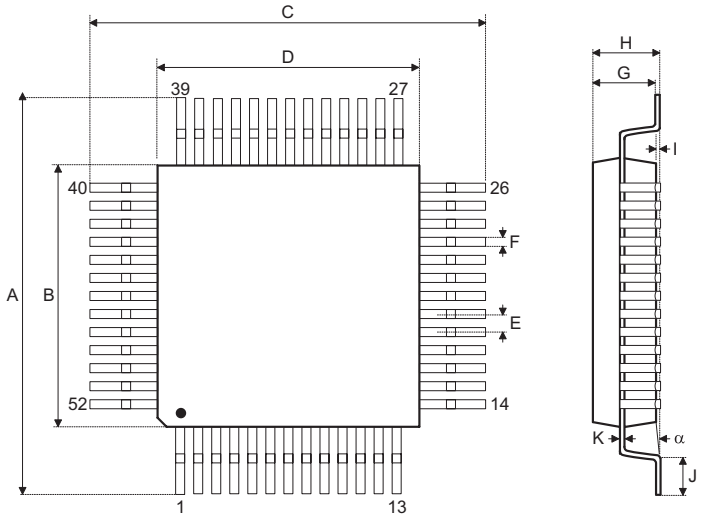
XOR A,[m]	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ [m]
Affected flag(s)	Z

XORM A,[m]	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″XOR″ [m]
Affected flag(s)	Z

XOR A,x	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ x
Affected flag(s)	Z

Package Information

52-pin QFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	17.3	—	17.5
B	13.9	—	14.1
C	17.3	—	17.5
D	13.9	—	14.1
E	—	1	—
F	—	0.4	—
G	2.5	—	3.1
H	—	—	3.4
I	—	0.1	—
J	0.73	—	1.03
K	0.1	—	0.2
α	0°	—	7°

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