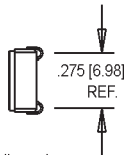
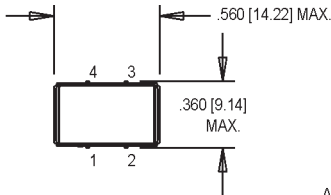


K1526D Series

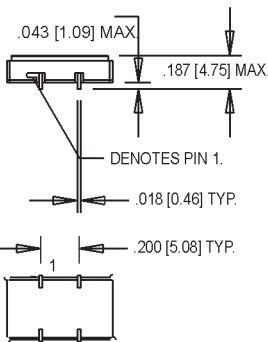
9x14 mm, 5.0 Volt, CMOS/TTL, VCXO



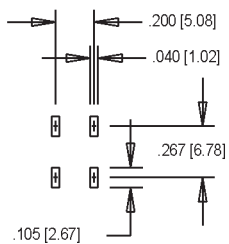
- Former **Champion** Product
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation



All dimensions in inches [mm].



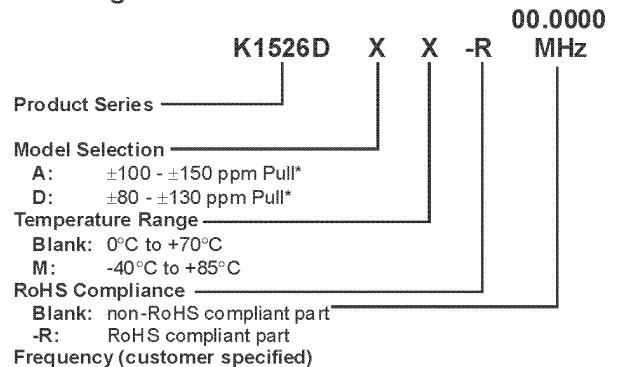
SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Voltage Control
2	Ground & Gnd Plane
3	Output
4	+Vdd

Ordering Information



* Above 40 MHz, pull is ±100 ppm or ±80 ppm minimum (no maximum)
M3026Sxxx - Contact factory for datasheet.

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	2		40	MHz		
Operating Temperature	T _A	(See ordering information)					
Storage Temperature	T _S	-40		+125	°C		
Frequency Stability Overall	ΔF/F	Inclusive of Calibration, Temperature, Voltage, Load, and Aging					
0°C to +70°C				±25	ppm		
-40°C to +85°C				±50	ppm		
Aging 1 st Year		-3		+3	ppm		
Thereafter (per year)		-1		+1	ppm		
Pullability/APR		(See ordering information)					
Control Voltage	V _c	0.5	2.5	4.5	V		
Linearity				5	%	Positive Monotonic Slope	
2.000 to 33.000 MHz				10	%		
33.001 to 40.000 MHz							
Modulation Bandwidth	f _m	20			KHz	±3dB	
Input Impedance	Z _{in}	50k			Ohms	@ 10 kHz	
Input Voltage	V _{dd}	4.5	5.0	5.5	V		
Input Current	I _{dd}			26	mA		
Output Type						HCMOS/TTL	
Load		5 TTL or 15 pF HCMOS				See Note 1	
Symmetry (Duty Cycle)						See Note 2	
TTL & CMOS < 33 MHz		45		55	%		
CMOS ≥ 33 MHz		40		60	%		
Logic "1" Level	V _{oh}	4.5			V		
Logic "0" Level	V _{ol}			0.5	V		
Output Current				±16	mA		
Rise/Fall Time	T _r /T _f			4	ns		
Start up Time				10	ms		
Phase Jitter @ 26 MHz	φ _J		4		ps RMS	Integrated 12 kHz – 20 MHz	
Phase Noise (Typical) @ 26 MHz		10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier dBc/Hz
		-65	-95	-115	-130	-140	
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)					
	Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
	Hermeticity	Per MIL-STD-202, Method 112, (1x10 ⁻⁸ atm. cc/s of Helium)					
	Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)					
	Solderability	Per EIAJ-STD-002					
Max Soldering Conditions	See solder profile, Figure 1						

- TTL load – see load circuit diagram #1. HCMOS load – see load circuit diagram #2.
- Symmetry is measured at 1.4 V with TTL load, and at 50% V_{dd} with HCMOS load.

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MtronPTI Lead Free Solder Profile



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