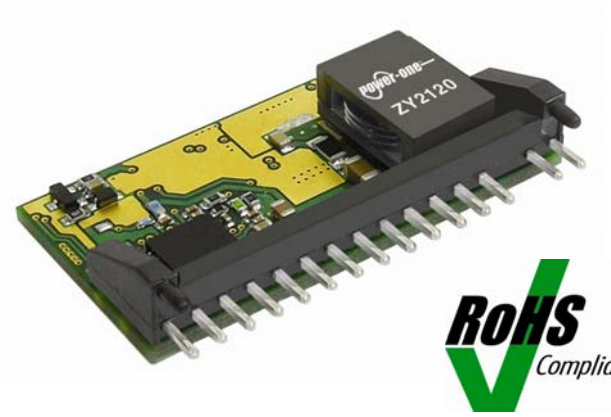
# ZY2120 20A No-Bus POL Data Sheet
## 8V to 14V Input • 0.5V to 5.5V Output
## Preliminary Data Sheet

**Member of the maXyz Family**




### Applications

- Low voltage, high density systems with Intermediate Bus Architectures (IBA)
- Point-of-load regulators for high performance DSP, FPGA, ASIC, and microprocessor applications
- Industrial computing, servers, and storage
- Broadband, networking, optical, and wireless communications systems
- Active memory bus terminators

### Benefits

- Integrates digital power conversion with intelligent power management
- Eliminates the need for external power management components and communication bus
- Completely programmable via pin strapping and one external resistor
- One part that covers all applications
- Reduces board space, system cost and complexity, and time to market

### Features

- RoHS lead free and lead-solder-exempt products are available
- Wide input voltage range: 8V–14V
- High continuous output current: 20A
- Wide programmable output voltage range: 0.5V–5.5V
- Active digital current share
- Output voltage margining
- Overcurrent and overtemperature protections
- Overvoltage and undervoltage protections, and Power Good signal tracking the output voltage setpoint
- Tracking during turn-on and turn-off with guaranteed slew rates
- Sequenced and cascaded modes of operation
- Single-wire line for frequency synchronization between multiple POLs
- Programmable feedback loop compensation
- Differential output voltage sense
- Enable control
- Flexible fault management and propagation
- Start-up into the load pre-biased up to 100%
- Current sink capability
- Real-time current measurements, monitoring, and reporting
- Industry standard size through-hole single-in-line package: 1.6”x0.41”
- Low height of 0.84”
- Wide operating temperature range: 0 to 70ºC
- UL 60950-1, 1st Edition CAN/CSA-C22.2 No. 60950-1-03, 1st Edition EN 60950-1/A11:2004, IEC 60950-1:2001 (pending)

### Description

The ZY2120 is an intelligent, fully programmable step-down point-of-load DC-DC module integrating digital power conversion and power management. The ZY2120 eliminates the need for external components for sequencing, tracking, protection, monitoring, and reporting. Performance parameters of the ZY2120 are programmable by pin strapping and an external resistor, and can be changed by the user at any time during product development and service without a need for a communication bus.

### Reference Documents

No-Bus™ POL Converters. Application Note
Z-One® POL Converters. Eutectic Solder Process Application Note
Z-One® POL Converters. Lead-Free Process Application Note

## 1. Ordering Information

| ZY | 21 | 20 | y | – | zz |
|---|---|---|---|---|---|
| **Product family:** Z-One Module | **Series:** No-Bus POL Converter | **Output Current:** 20A | **RoHS compliance:** **No suffix** - RoHS compliant with Pb solder exemption[1] **G** - RoHS compliant for all six substances | **Dash** | **Packaging Option[2]:** **R1** – 48 pcs Tray **Q1** – 1 pc sample for evaluation only |

[1] The solder exemption refers to all the restricted materials except lead in solder. These materials are Cadmium (Cd), Hexavalent chromium (Cr6+), Mercury (Hg), Polybrominated biphenyls (PBB), Polybrominated diphenylethers (PBDE), and Lead (Pb) used anywhere except in solder.
[2] Packaging option is used only for ordering and not included in the part number printed on the POL converter label.

Example: **ZY2120G-R1**: A 48-piece tray of RoHS compliant POL converters. Each POL converter is labeled ZY2120G.

## 2. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the POL converter.

| Parameter | Conditions/Description | Min | Max | Units |
|---|---|---|---|---|
| Operating Temperature | Case temperature (see Thermal Reference Points in Figure 14) | 0 | 125 | °C |
| Input Voltage | 250ms Transient | | 15 | VDC |

## 3. Environmental and Mechanical Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Ambient Temperature Range | | 0 | | 70 | °C |
| Storage Temperature (Ts) | | -55 | | 125 | °C |
| Weight | | | | 10 | grams |
| Operating Vibration (sinusoidal) | Frequency Range<br>Magnitude<br>Sweep Rate<br>Repetitions in each axis (Min-Max-Min Sweep) | 5<br>0.5<br>1<br>2 | | 500 | Hz<br>G<br>oct/min<br>sweeps |
| Non-Operating Shock (half sine) | Acceleration<br>Duration<br>Number of shocks in each axis | 50<br>11<br>10 | | | G<br>ms |
| MTBF | Calculated Per Telcordia Technologies SR-332 | 48.5 | | | MHrs |
| Peak Reflow Temperature | ZY2120 | | | 220 | °C |
| Peak Reflow Temperature | ZY2120G | | 245 | 260 | °C |
| Lead Plating | ZY2120 and ZY2120G | 100% Matte Tin | | | |
| Moisture Sensitivity Level | JEDEC J-STD-020C | 3 | | | |

## 4. Electrical Specifications

Specifications apply at the input voltage from 8V to 14V, output load from 0 to 20A, ambient temperature from 0°C to 70°C, output capacitance consisting of 110µF ceramic and 220µF tantalum, and the CCA=1 unless otherwise noted.

### 4.1 Input Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Input voltage ($V_{IN}$) | | 8 | | 14 | VDC |
| Undervoltage Lockout Threshold | Ramping Up<br>Ramping Down | 6.0<br>5.0 | 7.0<br>6.0 | 8.0<br>7.0 | VDC<br>VDC |
| Input Current | $V_{IN}$=12V, POL is OFF<br>$V_{IN}$=12V, POL is ON, No Load | | 20<br>100 | 40<br>150 | mADC<br>mADC |
| Maximum Input Current | $V_{IN}$=8V, $V_{OUT}$=5V, $I_{OUT}$=20A | | | 13.8 | ADC |

### 4.2 Output Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Output Current ($I_{OUT}$) | $V_{IN\ MIN}$ to $V_{IN\ MAX}$ | -20[1] | | 20 | ADC |
| Output Voltage Range ($V_{OUT}$) | Programmable with a resistor between TRIM and MARGIN pins<br>Default (no resistor) | 0.5 | <br>0.5 | 5.5 | VDC<br>VDC |
| Output Voltage Setpoint Accuracy[2] | $V_{IN}$=12V, $I_{OUT}$=0.5*$I_{OUT\ MAX}$, room temperature | ±1.5% or 20mV whichever is greater | | | %$V_{OUT}$ |
| Line Regulation[3] | $V_{IN\ MIN}$ to $V_{IN\ MAX}$ | | ±0.5 | | %$V_{OUT}$ |
| Load Regulation[3] | 0 to $I_{OUT\ MAX}$ | | ±0.5 | | %$V_{OUT}$ |
| Dynamic Regulation<br>Peak Deviation<br>Settling Time | 50% - 75% - 50% load step<br>Slew rate 1A/µs, $C_{OUT}$=330µF<br>to 10% of peak deviation | | <br>200<br>50 | | <br>mV<br>µs |
| Output Voltage Peak-to-Peak Ripple and Noise<br>BW=20MHz<br>Full Load | $V_{IN}$=12V, $V_{OUT}$=1.0V<br>$V_{IN}$=12V, $V_{OUT}$=2.5V<br>$V_{IN}$=12V, $V_{OUT}$=5.0V | | <br>20<br>25<br>40 | | <br>mV<br>mV<br>mV |
| Efficiency<br>$F_{SW}$=500kHz<br>Full Load<br>Room temperature | $V_{OUT}$=0.5V<br>$V_{OUT}$=1.0V<br>$V_{OUT}$=2.5V<br>$V_{OUT}$=3.3V<br>$V_{OUT}$=5.0V | | <br>71<br>81.5<br>89.5<br>91<br>93 | | <br>%<br>%<br>%<br>%<br>% |
| Temperature Coefficient | $V_{IN}$=12V, $I_{OUT}$=0.5*$I_{OUT\ MAX}$ | | 20 | | ppm/°C |
| Switching Frequency | | 450 | 500 | 550 | kHz |

[1] At the negative output current (bus terminator mode) efficiency of the ZY2120 degrades resulting in increased internal power dissipation. Maximum allowable negative current is limited to 20A.
[2] Digital PWM has an inherent quantization uncertainty of ±6.25mV that is not included in the specified static regulation parameters.

### 4.3 Protection Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| **Output Overcurrent Protection** | | | | | |
| Type | | Non-Latching, 130ms period | | | |
| Threshold | | 105 | 125 | 170 | $\%I_{OUT}$ |
| **Output Overvoltage Protection** | | | | | |
| Type | | Latching | | | |
| Threshold | Follows the output voltage setpoint | | 130[1] | | $\%V_{O.SET}$ |
| Threshold Accuracy | Measured at $V_{O.SET}$=2.5V | -2 | | 2 | $\%V_{OVP.SET}$ |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | µs |
| **Output Undervoltage Protection** | | | | | |
| Type | | Non-Latching, 130ms period | | | |
| Threshold | Follows the output voltage setpoint | | 75 | | $\%V_{O.SET}$ |
| Threshold Accuracy | Measured at $V_{O.SET}$=2.5V | -2 | | 2 | $\%V_{UVP.SET}$ |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | µs |
| **Overtemperature Protection** | | | | | |
| Type | | Non-Latching, 130ms period | | | |
| Turn Off Threshold | Temperature is increasing | | 120 | | °C |
| Turn On Threshold | Temperature is decreasing after module was shut down by OTP | | 110 | | °C |
| Threshold Accuracy | | -5 | | 5 | °C |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | µs |
| **Power Good Signal (PGOOD pin)** | | | | | |
| Logic | $V_{OUT}$ is inside the PG window and stable<br>$V_{OUT}$ is outside of the PG window or ramping up/down | High<br>Low | | | N/A |
| Lower Threshold | Follows the output voltage setpoint | | 90 | | $\%V_{O.SET}$ |
| Upper Threshold | Follows the output voltage setpoint | | 110 | | $\%V_{O.SET}$ |
| Delay | From instant when threshold is exceeded until status of PG pin changes | | 6 | | µs |
| Threshold Accuracy | Measured at $V_{O.SET}$=2.5V | -2 | | 2 | $\%V_{O.SET}$ |

[1] Minimum OVP threshold is 1.0V

### 4.4 Feature Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| **Current Share (CS pin)** | | | | | |
| Type | | Active, Single Line | | | |
| Current Share Accuracy | $I_{OUT\ MIN} \geq 20\% * I_{OUT\ NOM}$ | | | ±20 | $\%I_{OUT}$ |
| **Tracking** | | | | | |
| Rising Slew Rate | Proportional to SYNC frequency | | 0.1 | | V/ms |
| Falling Slew Rate | Proportional to SYNC frequency | | -0.5 | | V/ms |
| **Enable (EN pin)** | | | | | |
| EN Pin Polarity | | Positive (enables the output when EN pin is open or pulled high) | | | |
| EN High Threshold | | 2.3 | | | VDC |
| EN Low Threshold | | | | 1.0 | VDC |
| Open Circuit Voltage | | | 3.3 | | VDC |
| Turn-On Delay | From EN pin changing state to $V_{OUT}$ starting to ramp up | | 0 | | ms |
| Turn-Off Delay | From EN pin changing state to $V_{OUT}$ reaching 0V | | 11 | | ms |
| **Feedback Loop Compensation (CCA pin)** | | | | | |
| CCA pin is open | Recommended $C_{OUT}$/ESR range, combination of ceramic + tantalum | 50/5 + 220/40 | 100/5 + 470/40 | 400/5 + 2000/20 | µF/mΩ µF/mΩ |
| CCA pin is connected to GND | Recommended $C_{OUT}$/ESR range, ceramic | 100/5 | 220/5 | 400/5 | µF/mΩ |
| **Output Current Monitoring (CS pin)** | | | | | |
| Output Current Monitoring Accuracy | $30\% * I_{OUT\ NOM} < I_{OUT} < I_{OUT\ NOM}$ $V_{IN}$=12V | -20 | | +20 | $\%I_{OUT}$ |
| Conversion Ratio | Duty Cycle of the negative pulse corresponding to 100% of nominal current | | 82 | | % |
| **Remote Voltage Sense (-VS and +VS pins)** | | | | | |
| Type | | Differential | | | |
| Voltage Drop Compensation | Between +VS and VOUT | | | 300 | mV |
| Voltage Drop Compensation | Between -VS and PGND | | | 100 | mV |

## 4.5 Signal Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| VDD | Internal supply voltage | 3.15 | 3.3 | 3.45 | V |
| **SYNC Line** | | | | | |
| ViL_s | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_s | HIGH level input voltage | 0.75 x VDD | | VDD + 0.5 | V |
| Vhyst_s | Hysteresis of input Schmitt trigger | 0.25 x VDD | | 0.45 x VDD | V |
| IoL_s | LOW level sink current V(SYNC)=0.5V | 14 | | 60 | mA |
| Ipu_s | Pull-up current source V(SYNC)=0V | 300 | | 1000 | µA |
| Tr_s | Maximum allowed rise time 10/90%VDD | | | 300 | ns |
| Cnode_s | Added node capacitance | | 5 | 10 | pF |
| Freq_s | Clock frequency of external SYNC line | 475 | | 525 | kHz |
| Tsynq | Sync pulse duration | 22 | | 28 | % of clock cycle |
| T0 | Data=0 pulse duration | 72 | | 78 | % of clock cycle |
| **Inputs: CCA, EN, IM** | | | | | |
| Iup_x | Pull-up current source V(X)=0 | 25 | | 110 | µA |
| ViL_x | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_x | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_x | Hysteresis of input Schmitt trigger | 0.1 x VDD | | 0.3 x VDD | V |
| RdnL_x | External pull down resistance pin forced low | | | 10 | kΩ |
| **Power Good and OK Inputs/Outputs** | | | | | |
| Iup_PG | Pull-up current source V(PG)=0 | 25 | | 110 | µA |
| Iup_OK | Pull-up current source V(OK)=0 | 175 | | 725 | µA |
| ViL_x | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_x | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_x | Hysteresis of input Schmitt trigger | 0.1 x VDD | | 0.3 x VDD | V |
| IoL_x | LOW level sink current at 0.5V | 4 | | 20 | mA |
| **Current Share/Sense Bus** | | | | | |
| Iup_CS | Pull-up current source at V(CS)=0V | 0.84 | | 3.10 | mA |
| ViL_CS | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_CS | HIGH level input voltage | 0.75 x VDD | | VDD+0.5 | V |
| Vhyst_CS | Hysteresis of input Schmitt trigger | 0.25 x VDD | | 0.45 x VDD | V |
| IoL_CS | LOW level sink current V(CS)=0.5V | 14 | | 60 | mA |
| Tr_CS | Maximum allowed rise time 10/90% VDD | | | 100 | ns |

## 5. Typical Performance Characteristics

### 5.1 Efficiency Curves

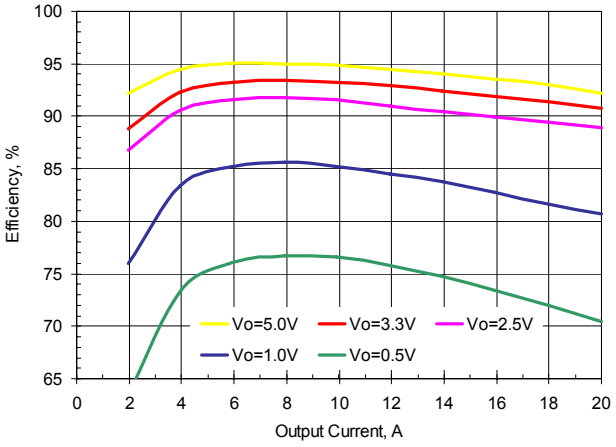



**Figure 1. Efficiency vs. Load. Vin=8V, Fsw=500kHz**

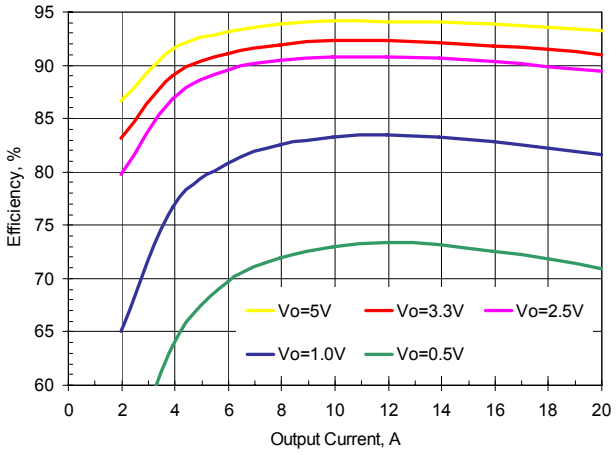



**Figure 2. Efficiency vs. Load. Vin=12V, Fsw=500kHz**

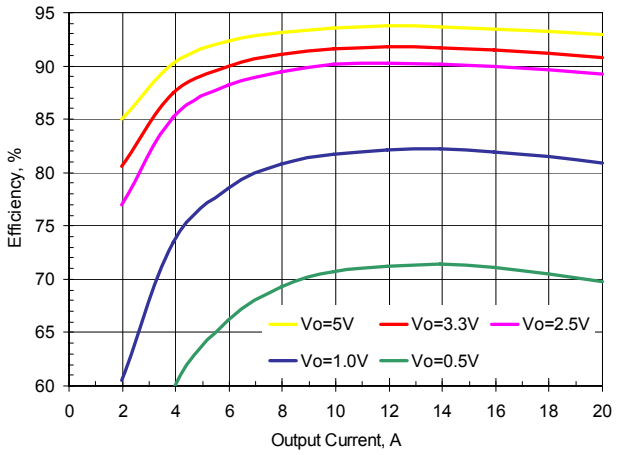



**Figure 3. Efficiency vs. Load. Vin=14V, Fsw=500kHz**

## 5.2 Turn-On Characteristics

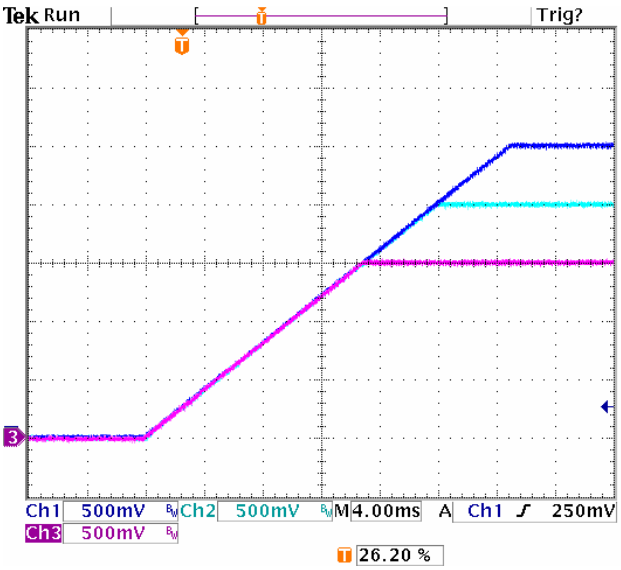



**Figure 4. Tracking Turn-On.**
**Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3**

## 5.3 Turn-Off Characteristics

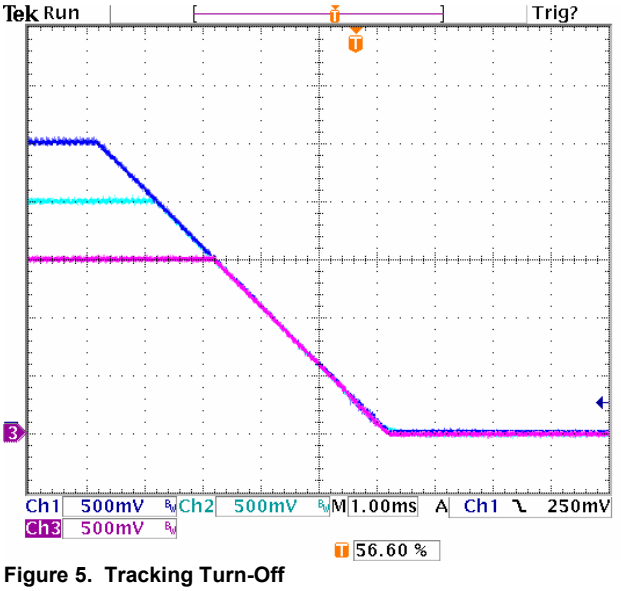



**Figure 5. Tracking Turn-Off**
**Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3**

## 5.4 Transient Response

The pictures below show the deviation of the output voltage in response to the 50%-75%-50% step load at 1.0A/µs. The transient response was tested with different combinations of the output capacitance and CCA settings.

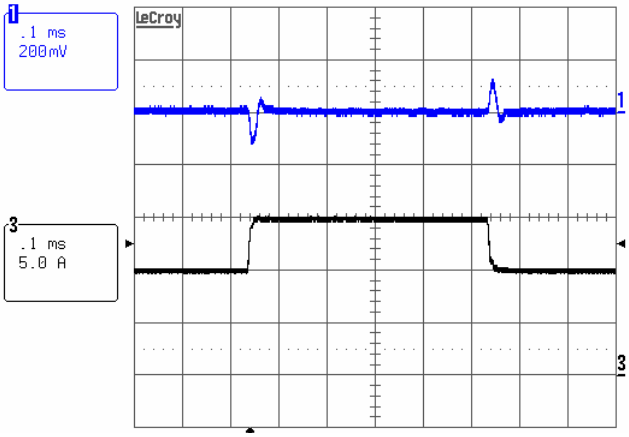



**Figure 6. Vin=12V, Vout=2.5V. Cout=5x22µF ceramics and 220µF tantalum. CCA=1**

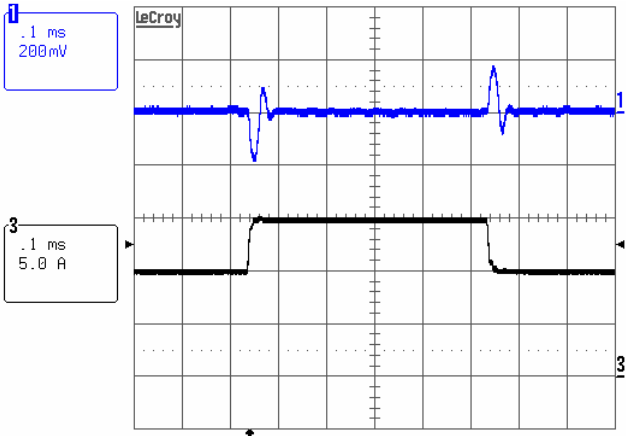



**Figure 7. Vin=12V, Vout=2.5V. Cout=5x22µF ceramics. CCA=0**

## 5.5 Thermal Derating Curves

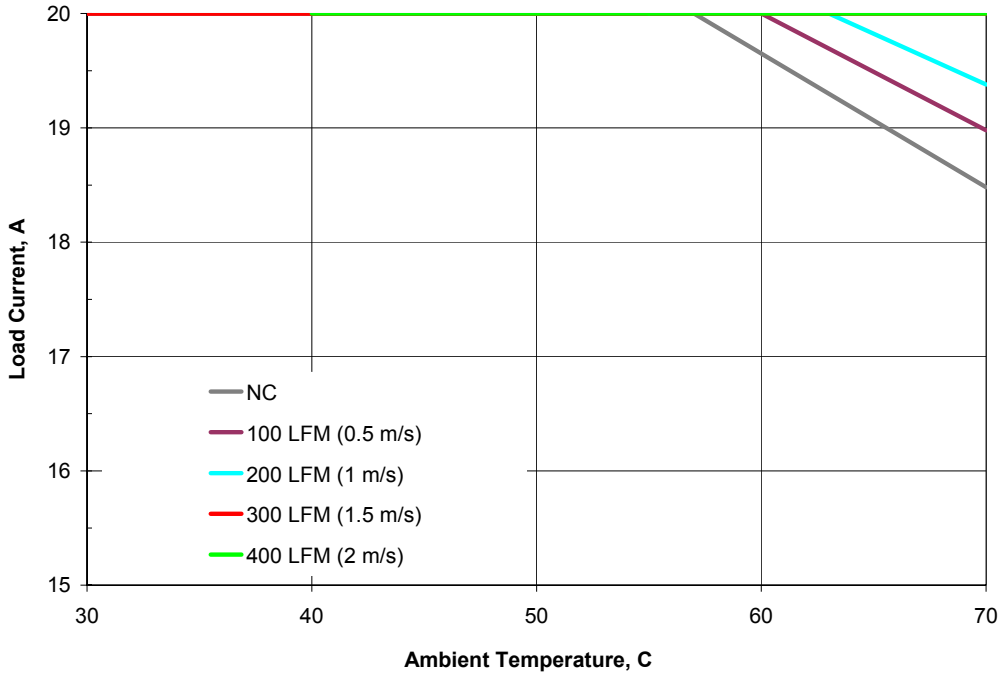



**Figure 8. Thermal Derating Curves. Vin=12V, Vout=2.5V**

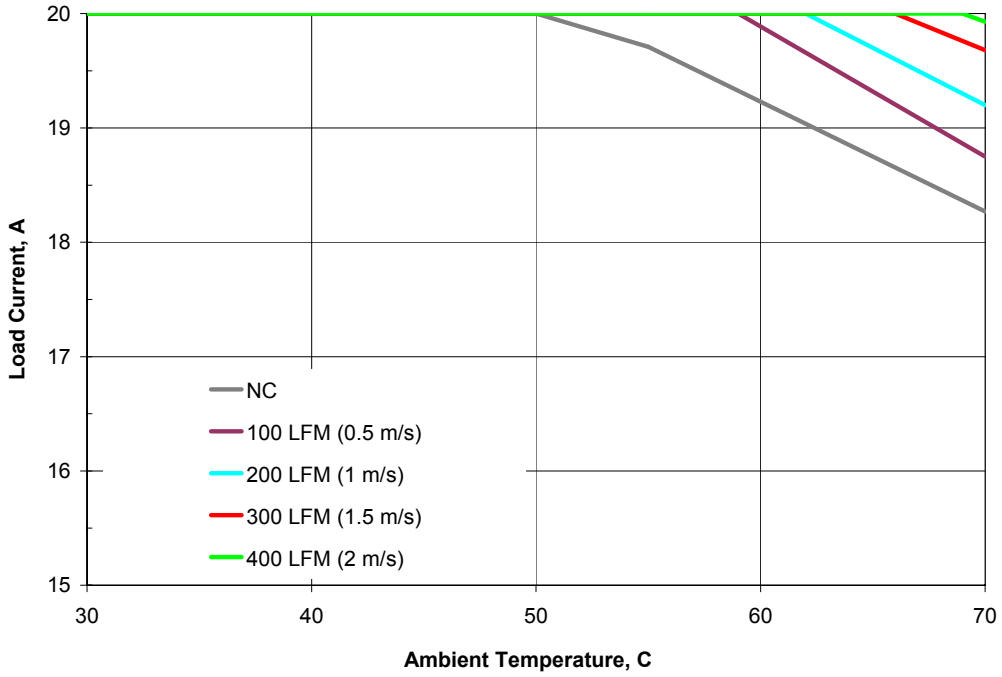



**Figure 9. Thermal Derating Curves. Vin=12V, Vout=3.3V**

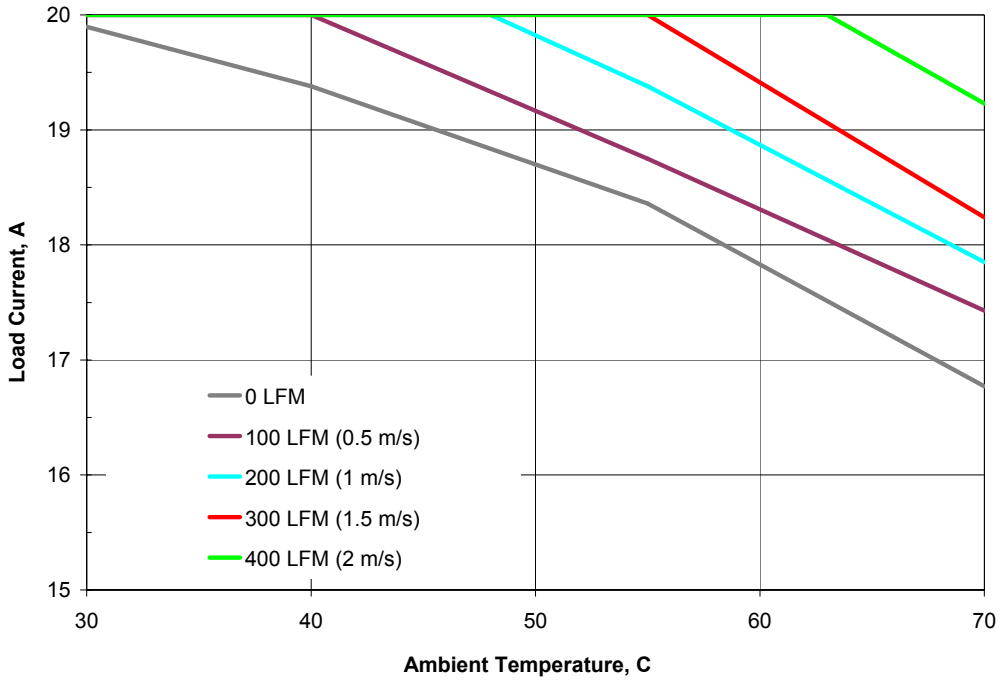



**Figure 10. Thermal Derating Curves. Vin=12V, Vout=5.0V**

## 6. Typical Application

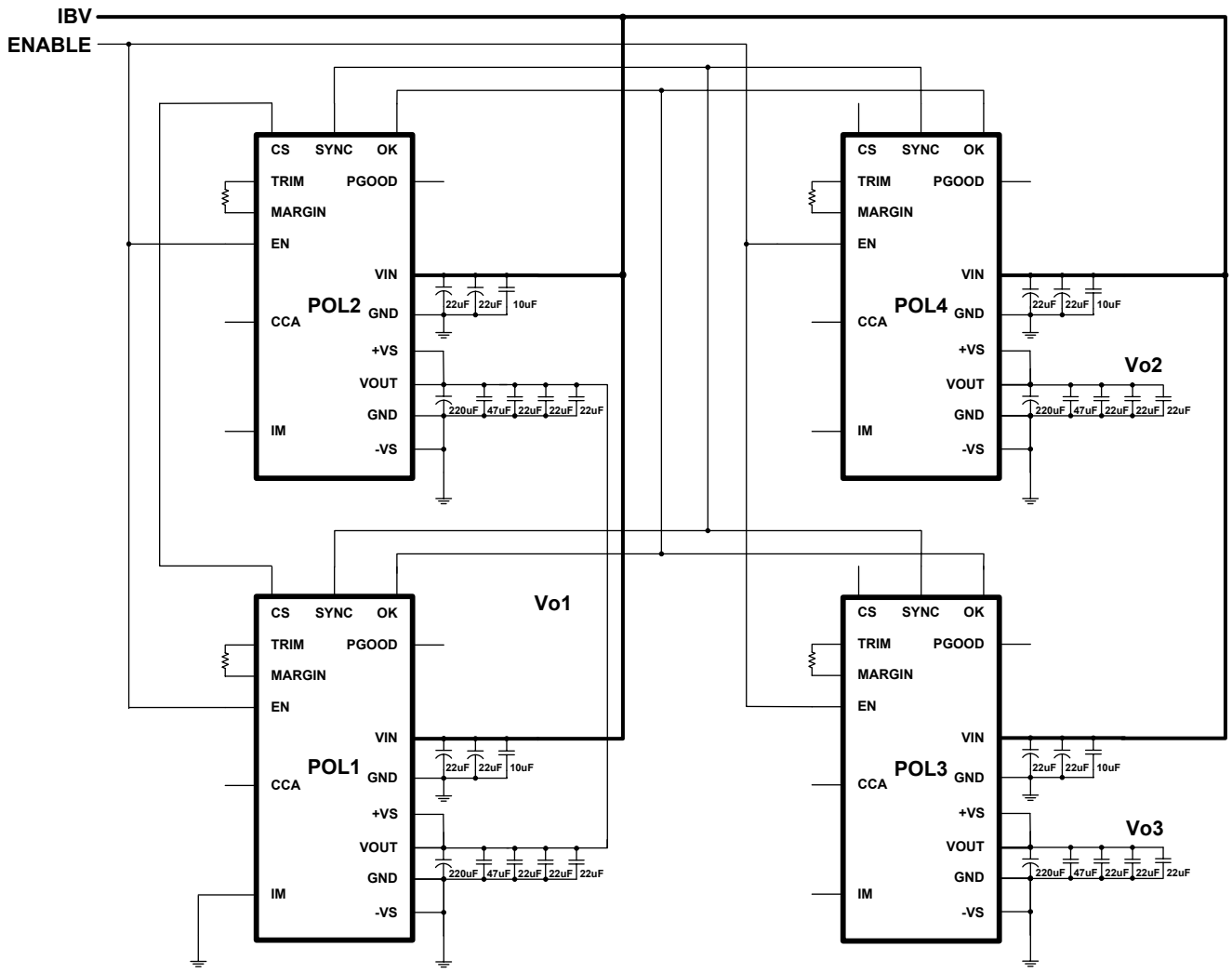



**Figure 11. Complete Schematic of Application with Three Independent Outputs. Intermediate Bus Voltage is from 8V to 14V.**

In this application four POL converters are configured to deliver three independent output voltages. POL1 and POL2 are connected in parallel for increased output current. Output voltages are programmed with the resistors connected between TRIM and MARGIN pins of individual converters.

POL1 is configured as a master (IM pin is grounded) and all other POL converters are synchronized to the switching frequency of POL1.

All converters are controlled by the common ENABLE signal. Turn-on and turn-off processes of the system are illustrated by pictures in Figure 4 and Figure 5.

## 7. Pin Assignments and Description

| Pin Name | Pin Number | Pin Type | Buffer Type | Pin Description | Notes |
|---|---|---|---|---|---|
| OK | 6 | I/O | PU | Fault Status | Connect OK pin to other Z-POLS. Leave open if not used |
| SYNC | 4 | I/O | PU | Frequency Synchronization Line | Connect SYNC pin to other Z-POLS or to an external clock generator |
| PGOOD | 11 | I/O | PU | Power Good | |
| CS | 3 | I/O | PU | Current Share/Sense | Connect CS pin to other ZY2120s connected in paralle. |
| IM | 9 | I | PU | Master Mode | Connect to GND to make the POL the clock master or leave open to synchronize to an external clock |
| CCA | 10 | I | PU | Compensation Coefficient Address | Connect to GND for logic 0 or leave open for logic 1 |
| MARGIN | 8 | A | | Output Voltage Margining | To program the output voltage, connect a resistor between MARGIN and TRIM |
| EN | 5 | I | PU | Enable | POL is ON when the pin is high or floating. POL is OFF when the pin is low or connected to GND |
| TRIM | 7 | A | | Output Voltage Trim | To program the output voltage, connect a resistor between MARGIN and TRIM |
| -VS | 16 | I | A | Negative Voltage Sense | Connect to the negative point close to the load |
| +VS | 12 | I | A | Positive Voltage Sense | Connect to the positive point close to the load |
| VOUT | 13 | P | | Output Voltage | |
| GND | 2,15 | P | | Power Ground | |
| VIN | 1 | P | | Input Voltage | |

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up

## 8. Pin and Feature Description

### 8.1 OK, Fault Status

The open drain input/output with the internal pull-up resistor. The POL converter pulls its OK pin low, if a fault occurs. Pulling low the OK input by an external circuitry turns off the POL converter.

### 8.2 SYNC, Frequency Synchronization Line

The bidirectional input/output with the internal pull-up resistor. If the POL converter is configured as a master, the SYNC line propagates clock to other POL converters. If the POL converter is configured as a slave, the internal clock recovery circuit synchronizes the POL converter to the clock of the SYNC line.

### 8.3 IM, Interleave Mode

The input with the internal pull-up resistor. When the pin is left floating, the switching frequency is determined by an external clock applied to the SYNC pin. Pulling the IM pin low configures a POL converter as a master. The master determines the clock on the SYNC line.

### 8.4 PG, Power Good

The open drain input/output with the internal pull-up resistor. The pin is pulled low by the POL converter, if the output voltage is outside of the window defined by the Power Good High and Low thresholds.

### 8.5 CCA, Compensation Coefficient Address

Inputs with internal pull-ups to select one of 2 sets of digital filter coefficients optimized for different characteristics of output capacitance.

### 8.6 CS, Current Share/Sense Bus

The open drain digital input/output with the internal pull-up resistor. The duty cycle of the digital signal is proportional to the output current of the POL converter. External capacitive loading of the pin shall be avoided.

### 8.7 MARGIN, Output Voltage Margining

The output of the 2V internal voltage reference that is used to program the output voltage of the POL converter.

### 8.8 TRIM, Output Voltage Trim

The input of the TRIM comparator for the output voltage programming.

The output voltage is programmed by a single resistor connected between MARGIN and TRIM pins.

**Table 1. Trim Resistor Values**

| $V_{out}$ [V] | $R_{TRIM}$ [kΩ] | The Closest Standard Value [kΩ] |
|---|---|---|
| 0.50 | Open | |
| 0.75 | 126.7 | 127 |
| 1.0 | 90 | 90.9 |
| 1.5 | 53.3 | 53.6 |
| 1.8 | 41.1 | 41.2 |
| 2.5 | 24 | 24.3 |
| 3.3 | 13.3 | 13 .3 |
| 5.0 | 2 | 2 |

### 8.9 EN, Enable

The input with the internal pull-up resistor. The POL converter is turned off, when the pin is pulled low

### 8.10 –VS and +VS

The differential voltage input of the POL converter feedback loop.

## 9. Application Information

### 9.1 Output Voltage Programming

Resistance of the trim resistor is determined from the equation below:

$$R_{TRIM} = \frac{20 \times (5.5 - V_{OUT})}{V_{OUT}}, \text{ kΩ}$$

where $V_{OUT}$ is the desired output voltage in Volts.

If the $R_{TRIM}$ is open or the TRIM pin is shorted to PGND, the $V_{OUT}$=0.5V.

### 9.2 Output Voltage Margining

Margining can be implemented by changing the resistance between the REF and TRIM pins.

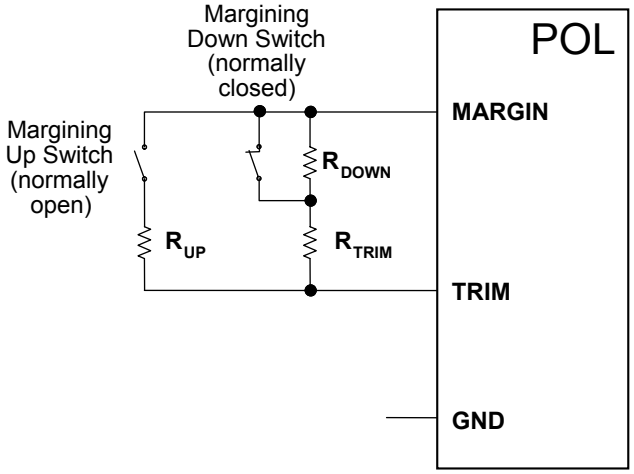



**Figure 12. Margining Configuration**

In the schematic shown in Figure 12, the nominal output voltage is set with the trim resistor $R_{TRIM}$ calculated from the equation in the paragraph 9.1. Resistors $R_{UP}$ and $R_{DOWN}$ are added to margin the output voltage up and down respectively and determined from the equations below.

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left( \frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ kΩ}$$

$$R_{DOWN} = (20 + R_{TRIM}) \times \left( \frac{\Delta V\%}{100 - \Delta V\%} \right), \text{ kΩ}$$

where $R_{TRIM}$ is the value of the trim resistor in kΩ and ΔV% is the absolute value of desired margining expressed in percents of the nominal output voltage.

During normal operation the resistors are removed from the circuit by the switches. The "Margining Down" switch is normally closed shorting the resistor $R_{DOWN}$ while the "Margining Up" switch is normally open disconnecting the resistor $R_{UP}$.

An alternative configuration of the margining circuit is shown in Figure 13. In the configuration both switches are normally open that may be advantageous in some implementations.

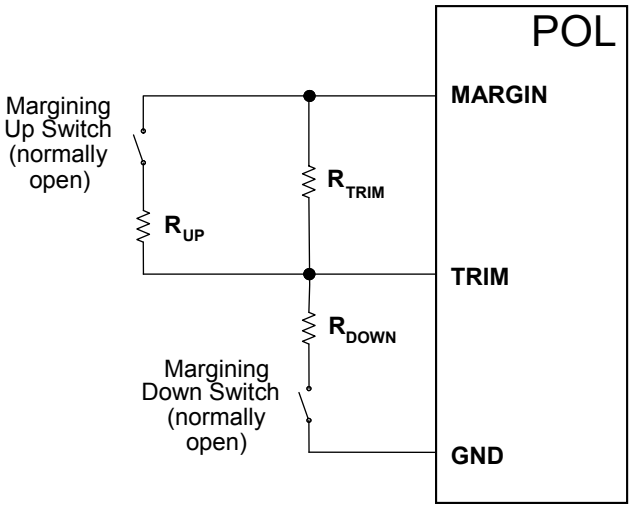



**Figure 13. Alternative Margining Configuration**

$R_{UP}$ and $R_{DOWN}$ for this configuration are determined from the following equations:

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left( \frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ kΩ}$$

$$R_{DOWN} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left( \frac{100 - \Delta V\%}{\Delta V\%} \right), \text{ kΩ}$$

**Caution**: Noise injected into the TRIM node may affect accuracy of the output voltage and stability of the POL converter. Always minimize the PCB trace length from the TRIM pin to external components to avoid noise pickup.

Refer to *No-Bus™ POL Converters. Application Note* on www.power-one.com for more application information on this and other product features.

## 10. Mechanical Drawings

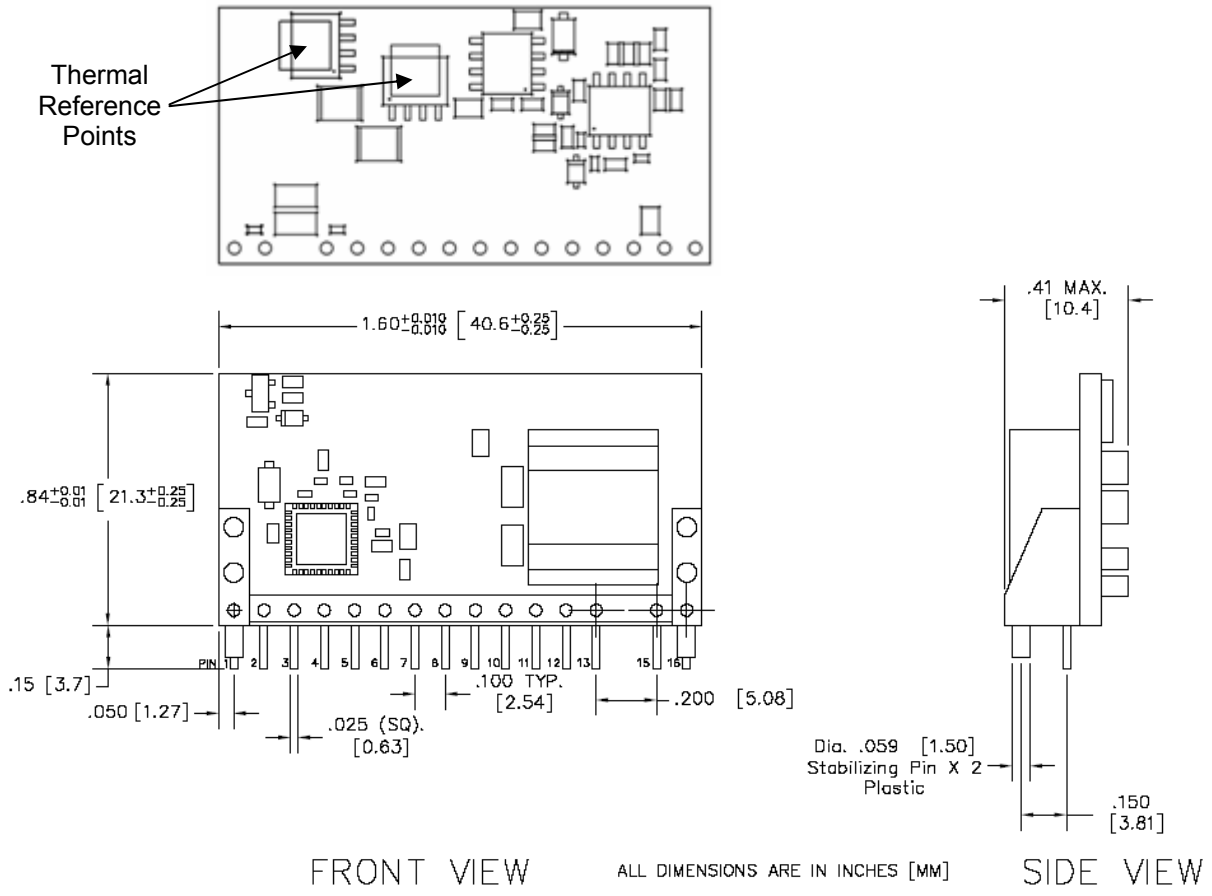



**Figure 14. Mechanical Drawing**

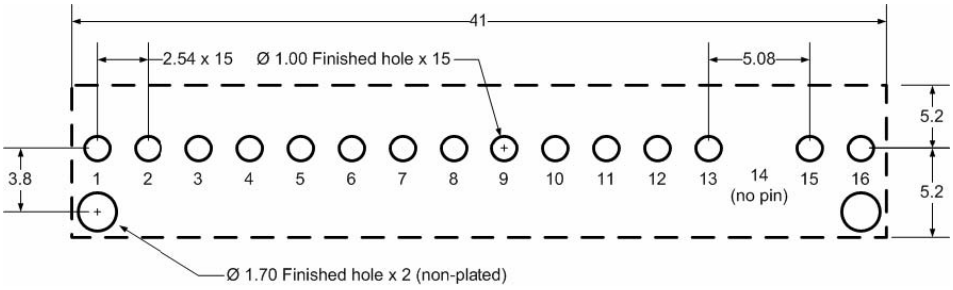



**Figure 15. Recommended Footprint – Top View (all dimensions in mm)**

**Notes:**

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