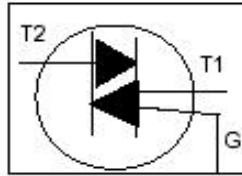
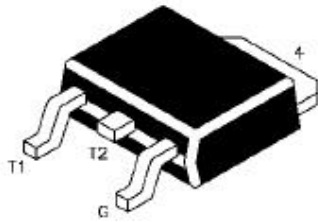


**TRIAC**

**CJD136**



**DPAK (TO-252)  
Plastic Package**

**For use in high bidirectional transient and blocking voltage applications, and for high thermal cycling performance. Typical Applications include Motor Control, Industrial and Domestic Lighting, Heating and Static Switching.**

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITION	VALUE	UNIT
Repetitive Peak Off State Voltage	$*V_{DRM}$		600	V
RMS on State Current	$I_{T(RMS)}$	full sine wave, $T_{mb} \leq 107^{\circ}C$	4.0	A
Non Repetitive Peak on State Current	$I_{TSM}$	full sine wave, $T_J=25^{\circ}C$ prior to $t=20ms$ $t=16.7ms$	25 27	A A
$I^2t$ for Fusing	$I^2t$	$t=10ms$	3.1	$A^2s$
Repetitive Rate of Rise of on State Current After Triggering	$di_T/dt$	$I_{TM}=6A, I_G=0.2A, di_G/dt=0.2A/\mu s$  T2+ G+ T2+ G- T2- G- T2- G+	50 50 50 10	A/ $\mu s$ A/ $\mu s$ A/ $\mu s$ A/ $\mu s$
Peak Gate Current	$I_{GM}$		2.0	A
Peak Gate Voltage	$V_{GM}$		5.0	V
Peak Gate Power	$P_{GM}$		5.0	W
Average Gate Power	$P_{G(AV)}$	Over any 20ms period	0.5	W
Storage Temperature	$T_{stg}$		- 40 to +150	$^{\circ}C$
Operating Junction Temperature	$T_j$		125	$^{\circ}C$

\*The rate of rise of current should not exceed 3A/ $\mu s$

**THERMAL RESISTANCE**

Junction to Mounting Base	$R_{th(j-mb)}$	full cycle half cycle	3.0 max 3.7 max	K/W K/W
Junction to Ambient (typical)	$R_{th(j-a)}$	in free air	60 typ	K/W

**ELECTRICAL CHARACTERISTICS ( $T_J=25^{\circ}C$  unless specified otherwise)**

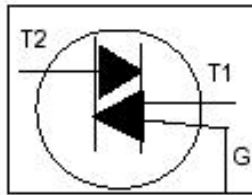
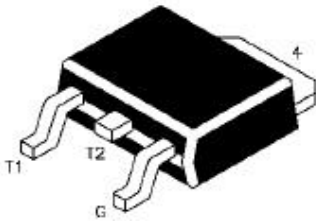
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Gate Trigger Current	$I_{GT}$	$V_D=12V, I_T=0.1A$  T2+ G+ T2+ G- T2- G- T2- G+		35 35 35 70	mA mA mA mA

**MARKING**

CDIL  
CJD136  
MX XY

XY= Date Code

CJD136Rev171104E



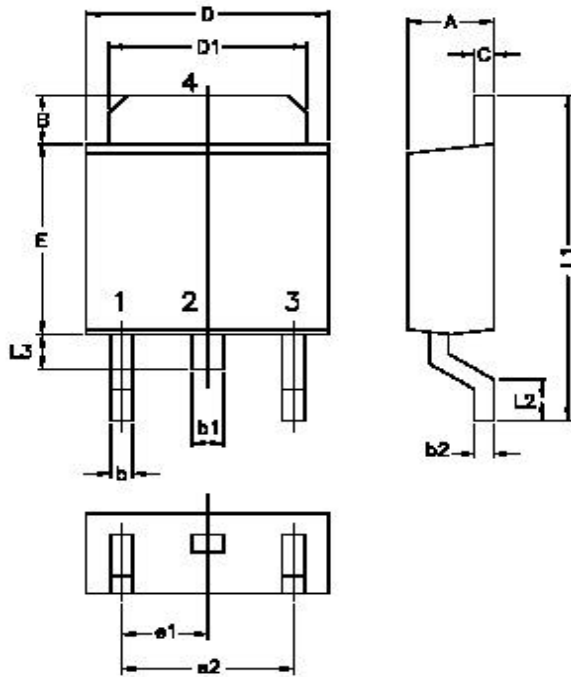
**ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C unless specified otherwise)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Latching Current	I <sub>L</sub>	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A			
		T2+ G+		20	mA
		T2+ G-		30	mA
		T2- G-		20	mA
		T2- G+		30	mA
Holding Current	I <sub>H</sub>	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A		15	mA
On State Voltage	V <sub>T</sub>	I <sub>T</sub> =5A		1.7	V
Gate Trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> =12V, I <sub>T</sub> =0.1A		1.5	V
		V <sub>D</sub> =400V, I <sub>T</sub> =0.1A, T <sub>J</sub> =125°C	0.25		V
Off State Leakage Current	I <sub>D</sub>	V <sub>D</sub> =max, V <sub>DRM</sub> =max, T <sub>J</sub> =125°C		0.5	mA

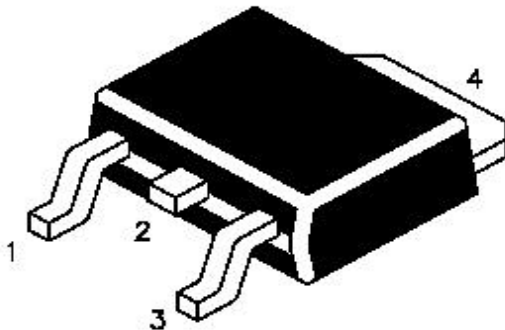
**DYNAMIC CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Critical Rate of Rise of off State Voltage	dV <sub>D</sub> /dt	V <sub>DM</sub> =67% V <sub>DRM</sub> =max, T <sub>J</sub> =125°C, exponential waveform, gate open circuit	100			V/μs
Critical Rate of Change of Commutating Voltage	dV <sub>com</sub> /dt	V <sub>DM</sub> =400V, T <sub>J</sub> =95°C, I <sub>T(RMS)</sub> =4A, dI <sub>com</sub> /dt=1.8A/ms, gate open circuit		50		V/μs
Gate Controlled turn on time	t <sub>gt</sub>	I <sub>TM</sub> =6A, V <sub>D</sub> =V <sub>DRM</sub> max, I <sub>G</sub> =0.1A, dI <sub>G</sub> /dt=5A/μs		2.0		μs

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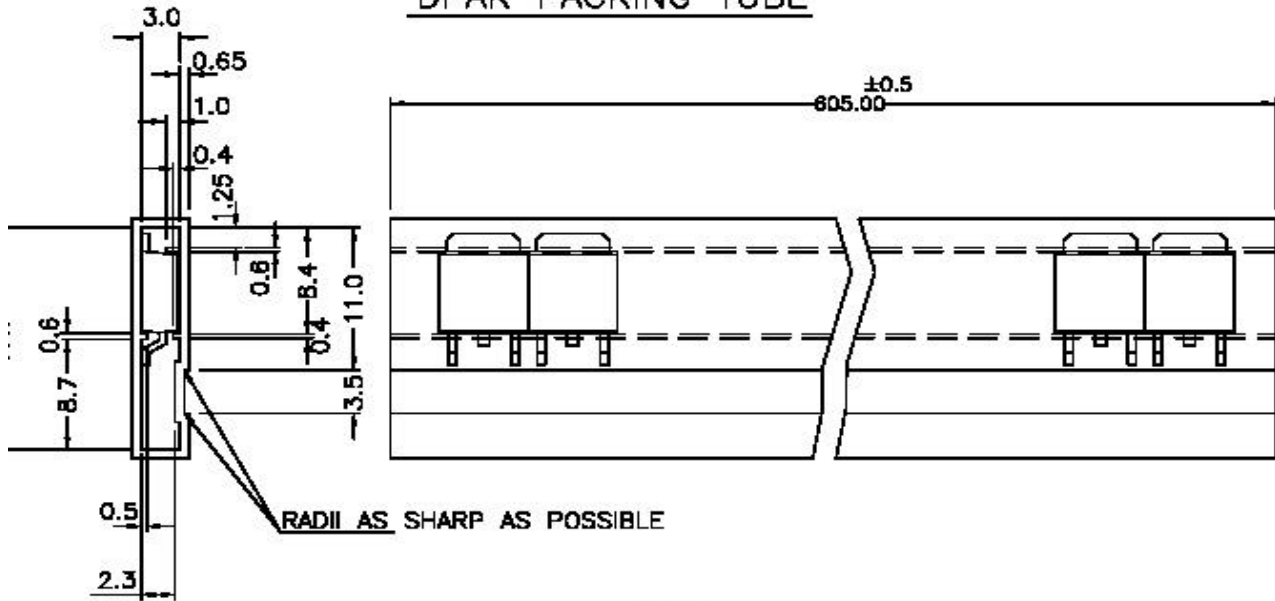
DIM	MIN.	MAX.
A	2.20	2.40
B	1.30	1.50
b	0.55	0.65
b1	0.75	0.85
b2	0.46	0.58
C	0.46	0.58
D	6.40	6.60
D1	5.20	5.40
E	5.40	5.60
e1	2.25	2.35
e2	4.50	4.70
L1	9.25	9.75
L2	0.5	–
L3	0.90	1.10



## PIN CONFIGURATION

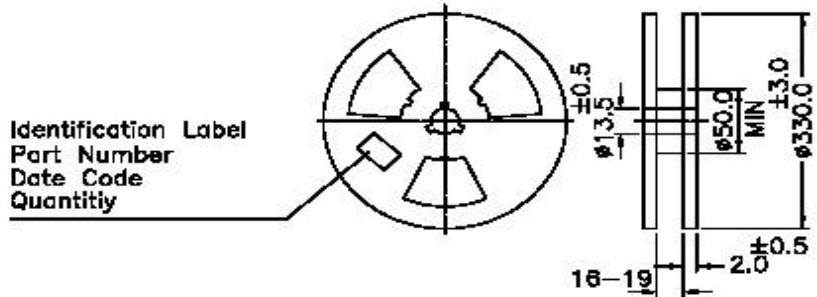
1. T1 MAIN TERMINAL 1
2. T2 MAIN TERMINAL 2
3. G GATE
4. FIN (T2)

DPAK PACKING TUBE



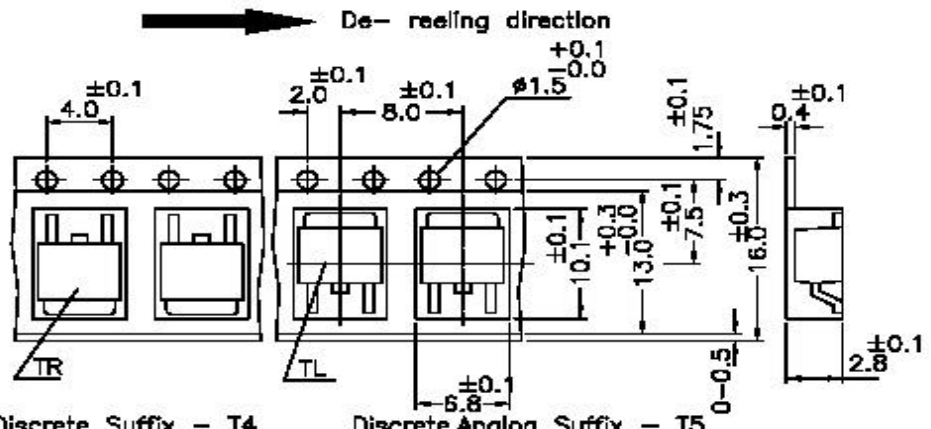
NOTE:-  
80 Pcs/TUBE  
ALL DIMENSIONS ARE IN mm

# DPAK TAPE & REEL SPECIFICATION



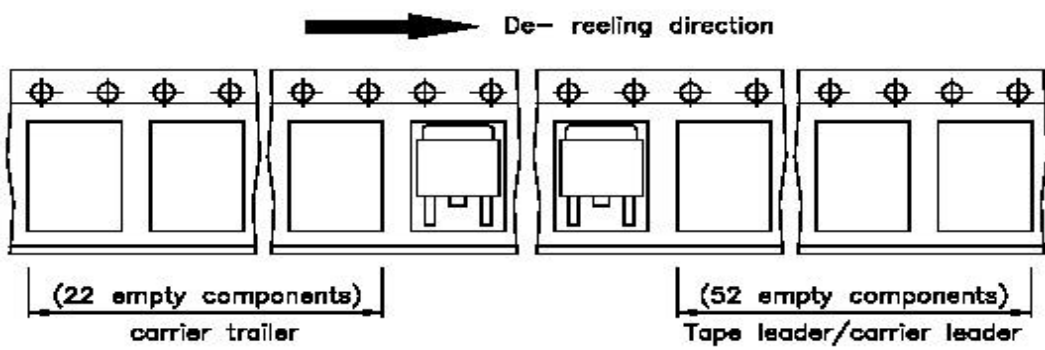
ALL DIMENSIONS ARE IN mm  
 REEL  $\phi$  330 mm (13")  
 No of Device 2500

## TAPE & REEL



Discrete Suffix - T4  
 Analog Suffix - RK  
 Discrete, Analog Suffix - T5

Notes:-  
 A maximum of three consecutive components may be missing. Provided this gap is followed by six consecutive components.



### **Disclaimer**

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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