



Solid State Devices, Inc.

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SFT5094 and SFT5096 Series

1 AMP, 500 Volts High Voltage PNP Transistor

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

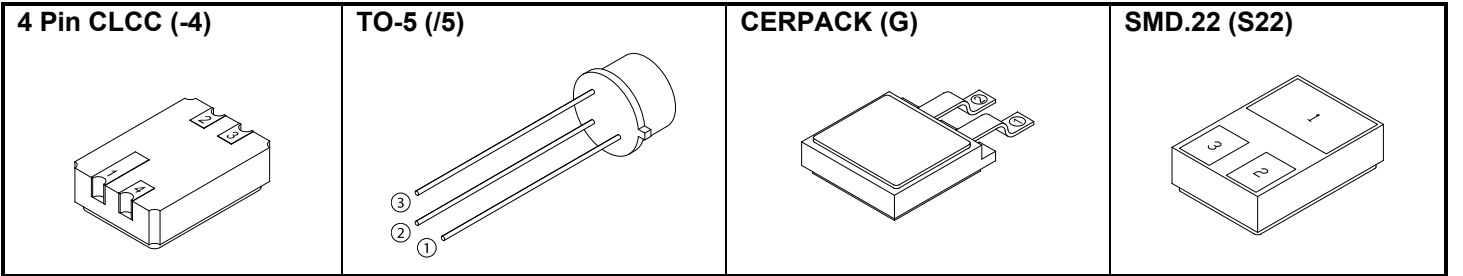
SFT5094
SFT5096

Screening ^{2/} = No Screening
TX = TX Level
TXV = TXV Level
S = S Level

Package ^{3/} -4 = 4 Pin CLCC
/5 = TO-5
G = CERPACK
S22 = SMD.22

- Features:**
- BV_{CER} to 500 Volts
 - Low Leakage at High Temperature
 - High Linear Gain, Low Saturation Voltage
 - 200°C Operating Temperature
 - Gold Eutectic Die Attach
 - TX, TXV, S-Level Screening Available
 - Designed for Complementary Use with SFT5015
 - Replacement for 2N5094 and 2N5096 with Lower Thermal Resistance
 - Available with TO-5, Cerpack, CLCC, and SMD.22 Cases

Maximum Ratings	Symbol	SFT5094	SFT5096	Units
Collector – Emitter Voltage (R _{BE} = 1kΩ)	V _{CEO} V _{CER}	400 450	450 500	Volts Volts
Collector – Base Voltage	V _{CBO}	450	500	Volts
Emitter – Base Voltage	V _{EBO}	6		Volts
Collector Current	I _C	1.0		Amps
Base Current	I _B	0.5		Amps
Total Power Dissipation (T _C = 25°C) Derate above T _C = 25°C (T _A = 25°C)	P _D	1.0 0.4		Watts Watts
Operating & Storage Temperature	T _J & T _{STG}	-65 to +200		°C
Maximum Thermal Resistance (Junction to Case)	R _{θJC}	4 Pin CLCC TO-5 CERPACK SMD.22	175 30 9 9	°C/W °C/W °C/W
Maximum Thermal Resistance (Junction to Ambient)	R _{θJA}	4 Pin CLCC TO-5 CERPACK SMD.22	440 --- 440 440	°C/W °C/W °C/W



NOTES: 1/ For Ordering Information, Price, Operating Curves, and Availability Contact Factory.
2/ Screened to MIL-PRF-19500.
3/ For Package Outlines, See Figure 1.
4/ Unless Otherwise Specified, Maximum Ratings/Electrical Characteristics at 25°C.

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: TR0081C **DOC**



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SFT5094 and SFT5096 Series

Electrical Characteristics ^{4/}	Symbol	Min	Max	Units	
Collector – Emitter Breakdown Voltage * (I _C = 50 mA) (I _C = 100 μA, R _{BE} = 1k Ω)	BV_{CEO}	SFT5094 400	SFT5096 450	—	Volts
	BV_{CER}	450	500	—	Volts
Collector – Base Breakdown Voltage * (I _C = 100 μA)	BV_{CBO}	450	500	—	Volts
Emitter – Base Breakdown Voltage (I _E = 50 μA)	BV_{EBO}	6	—	—	Volts
Collector Cutoff Current (V _{CB} = Rated, T _A = 25°C) (V _{CB} = Rated, T _A = 100°C)	I_{CBO1}	—	1.0	—	μA
	I_{CBO2}	—	50	—	μA
Emitter Cutoff Current (V _{EB} = 6 V)	I_{EBO}	—	1.0	—	μA
DC Current Gain * (I _C = 1 mA, V _{CE} = 10 V) (I _C = 25 mA, V _{CE} = 10 V) (I _C = 100 mA, V _{CE} = 10 V)	H_{FE}	20	250	—	—
		40	300	—	—
		20	250	—	—
Collector-Emitter Saturation Voltage * (I _C = 25 mA, I _B = 2.5 mA)	V_{CE(SAT)}	—	500	—	mV
Base-Emitter Saturation Voltage (I _C = 25 mA, I _B = 2.5 mA)	V_{BE(SAT)}	—	1.0	—	Volts
Current Gain Bandwidth Product * (I _C = 10 mA, V _{CE} = 10 V, f = 10 MHz)	f_T	25	—	—	MHz
Output Capacitance V _{CB} = 20 V, I _E = 0 A, f = 1.0MHz	C_{ob}	—	10	—	pF
Turn on Delay Time Rise Time Storage Time Fall Time V _{CC} = 100 V I _C = 100 mA I _{B1} = I _{B2} = 10 mA	T_d	—	500	—	ns
	T_r	—	1200	—	ns
	T_s	—	2.0	—	μs
	t_f	—	500	—	ns

Notes: * Pulse Test: Pulse Width = 300 μs. Duty Cycle = 2%.

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PIN ASSIGNMENT (Standard)

Package	Collector	Emitter	Base
4 Pin CLCC (-4)	Pin 1	Pin 2	Pin 3
TO-5 (/5)	Pin 3	Pin 1	Pin 2
CERPACK (G)	CASE	Pin 1	Pin 2
SMD.22	Pin 1	Pin 2	Pin 3

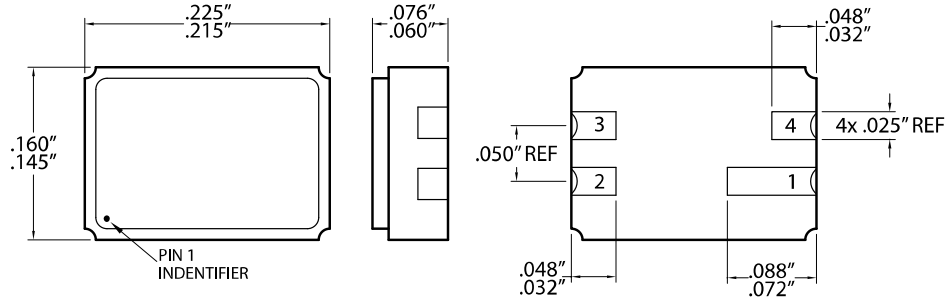
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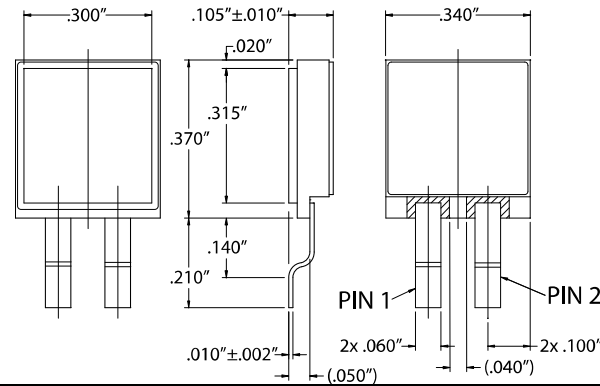
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FIGURE 1 – CASE OUTLINES

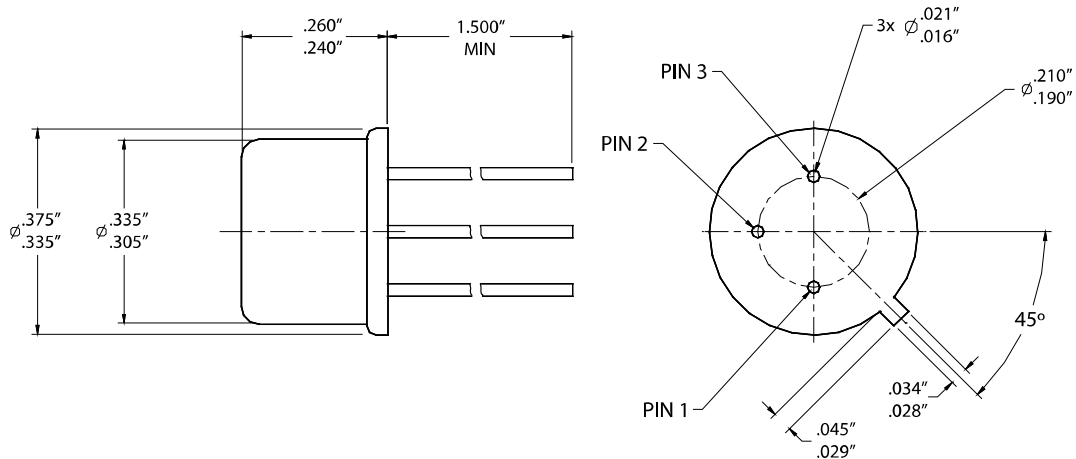
4 Pin CLCC (-4):



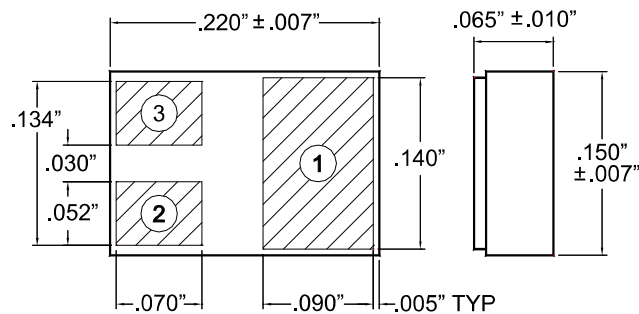
CERPACK (G):



TO-5 (I5):



SMD.22 (S22):



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