32-Channel Serial to Parallel Converter with P-Channel Open Drain Outputs

Features

- Processed with HVCMOS Technology
- Output voltages to -220V
- Source current minimum 60mA
- Shift register speed 8MHz
- Polarity and blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Can be used with the HV55 and HV56 to provide 220V push pull operation
- 44-lead PLCC surface mount package

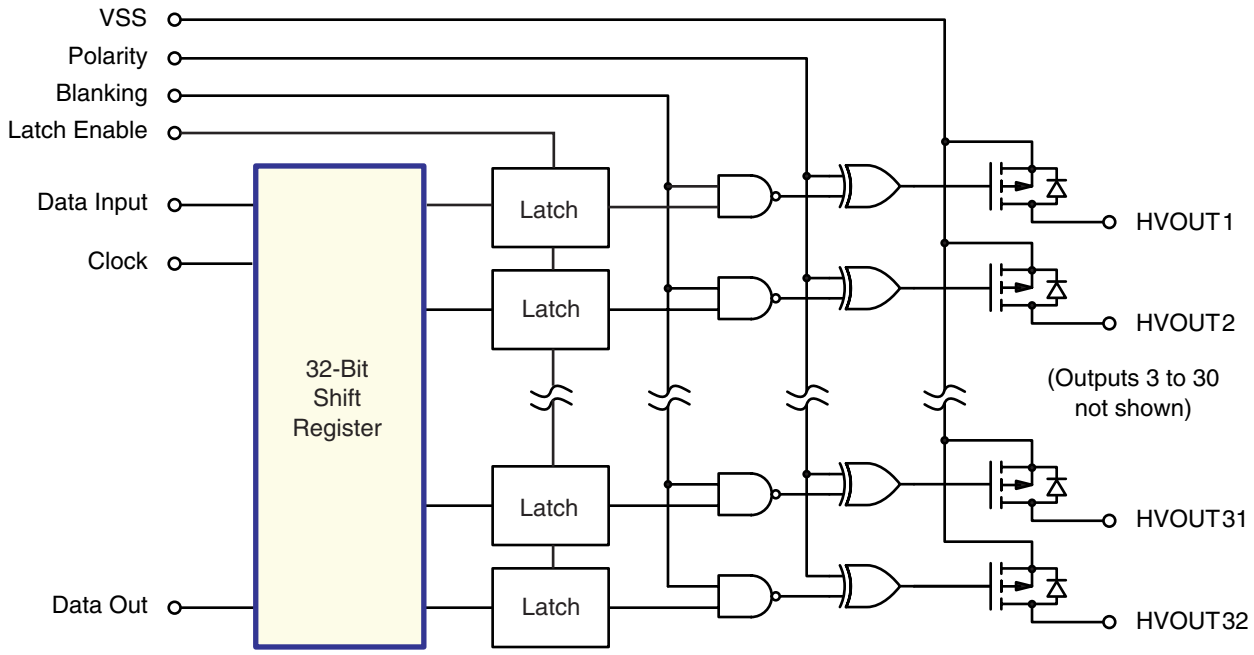
General Description

TThe HV4522 and HV4622 are low-voltage serial to high-voltage parallel converters with P-Channel open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current source capabilities, such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register, 32 data latches, and control logic to perform polarity and blanking functions. Data is shifted through the shift register on the logic high-to-low transition of the clock. The HV4522 shifts in the counter clockwise direction, while the HV4622 shifts in the clockwise direction (when viewed from the top of the package). A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. The data in the shift register is latched when the latch enable pin is brought to logic high, and then returned to ground. If the latch enable pin is held high, the latch becomes transparent and the shift register data is directly reflected in the outputs.

For applications requiring active pull down as well as pull up, the HV4522 and HV4622 can be paired with the HV55 and HV56 devices, respectively.

Functional Block Diagram

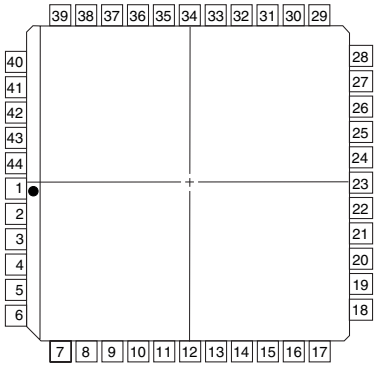


Ordering Information

Device	Package Options
	44-J Lead PLCC
HV4522	HV4522PJ-G
HV4622	HV4622PJ-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



44-J Lead PLCC (PJ)
(top view)

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	+0.5V to -16V
Output voltage , V_{PP}	+0.5V to -240V
Logic input levels	+0.5V to V_{DD} -0.3V
Ground current(1)	1.5A
Continuous total power dissipation(2)	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature *(1.6mm from case for 10 seconds)*	260°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to V_{SS}.

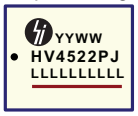
Notes:

(1) Duty cycle limited by the total power dissipated in the package.

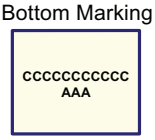
(2) For operation above 25°C ambiant derate linearly to maximum operating temperature at 20mW/°C.

Product Marking

Top Marking



Bottom Marking

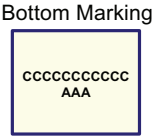


YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging
**May be part of top marking*

44-J Lead PLCC (PJ)

Top Marking

Bottom Marking



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44-J Lead PLCC (PJ)

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	-10.8	-13.2	V
V_{PP}	Output voltage	+0.3	-220	V
V_{IH}	High-level input voltage (Logic "1")	V_{DD} + 2V	V_{DD}	V
V_{IL}	Low-level input voltage (Logic "0")	0	-2.0	V
f_{CLK}	Clock frequency	-	8.0	MHz
T_A	Operating free-air temperature	-40	+85	°C

Note: *All voltages are referenced to V_{SS}*

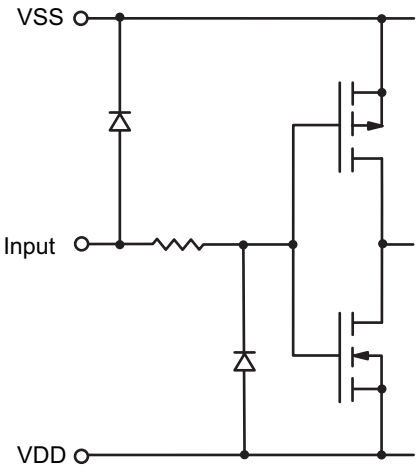
DC Electrical Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	-15	mA	f_{CLK} = 8.0MHz, F_{DATA} = 4.0MHz
I_{DDQ}	Quiescent V_{DD} supply current		-	-100	µA	V_{IN} = V_{SS} or V_{DD}
$I_{O(OFF)}$	Off state output current		-	-100	µA	All SWS parallel
I_{IH}	High-level logic input current		-	-1.0	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current		-	+1.0	µA	V_{IL} = V_{SS}
V_{OH}	High level output		V_{DD} + 1.0V	-	V	I_{DOUT} = -100µA
V_{OL}	Low level output	HV_{OUT}	-	-30	V	I_{HVOUT} = -60mA
		D_{OUT}	-	-1.0	V	I_{DOUT} = -100µA
V_{OC}	HV_{OUT} clamp voltage		-	+1.5	V	I_{OL} = +60mA

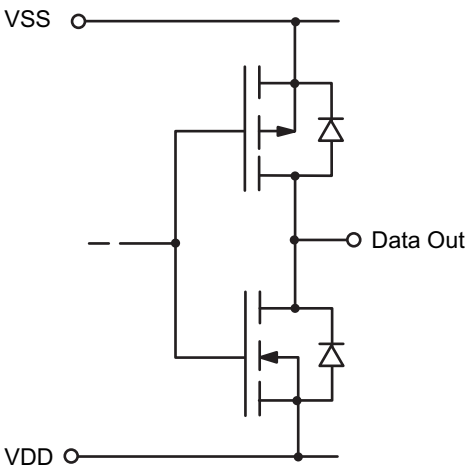
AC Electrical Characteristics *(V_{DD} = -12V, T_C = 25°C)*

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	---
t_{WH}, t_{WL}	Clock width high or low	62	-	ns	---
t_{SU}	Data set-up time before clock rises	50	-	ns	---
t_H	Data hold time after clock rises	20	-	ns	---
t_{ON}	Turn on time, HV_{OUT} from enable	-	400	ns	R_L = 10K to V_{OO} max
t_{DHL}	Delay time clock to data high to low	-	100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high	-	100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ high to low	37.5	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	50	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	37.5	-	ns	---

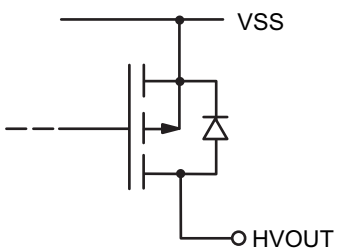
Input and Output Equivalent Circuits



Logic Inputs

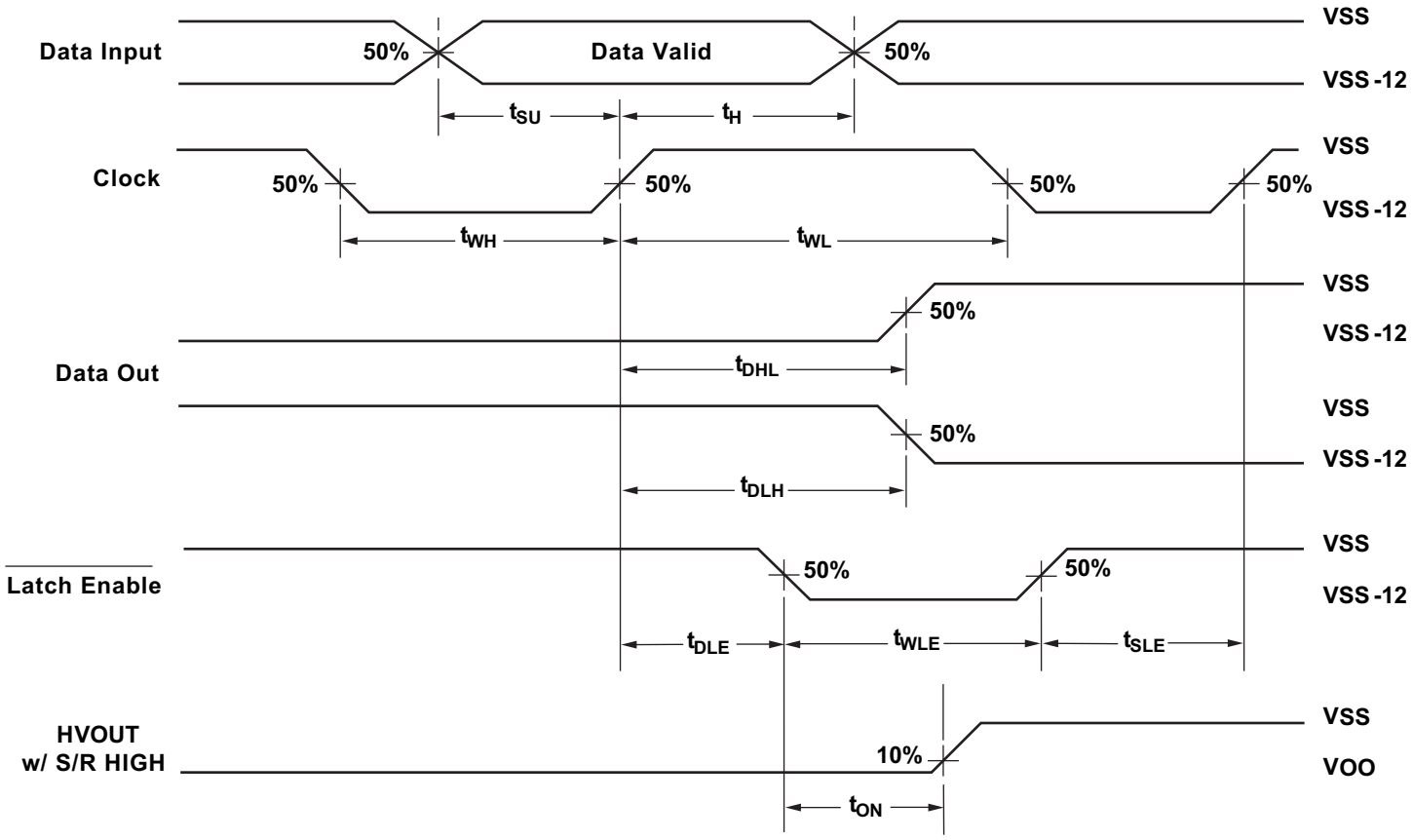


Logic Data Output



High Voltage Output

Switching Waveforms



Function Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*...*	*	*...*	*
Load latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↓	H	H	H	L	*...*	L	*...*	*
	H	↓	H	H	H	H	*...*	H	*...*	*

Notes:

H = high level = -12V, L = low level = 0V, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transition.

* = dependent on previous stage's state before the last CLK high-to-low transition or last $\overline{LE}$ high.

Pin Description (HV4522 - 44-J Lead PLCC)

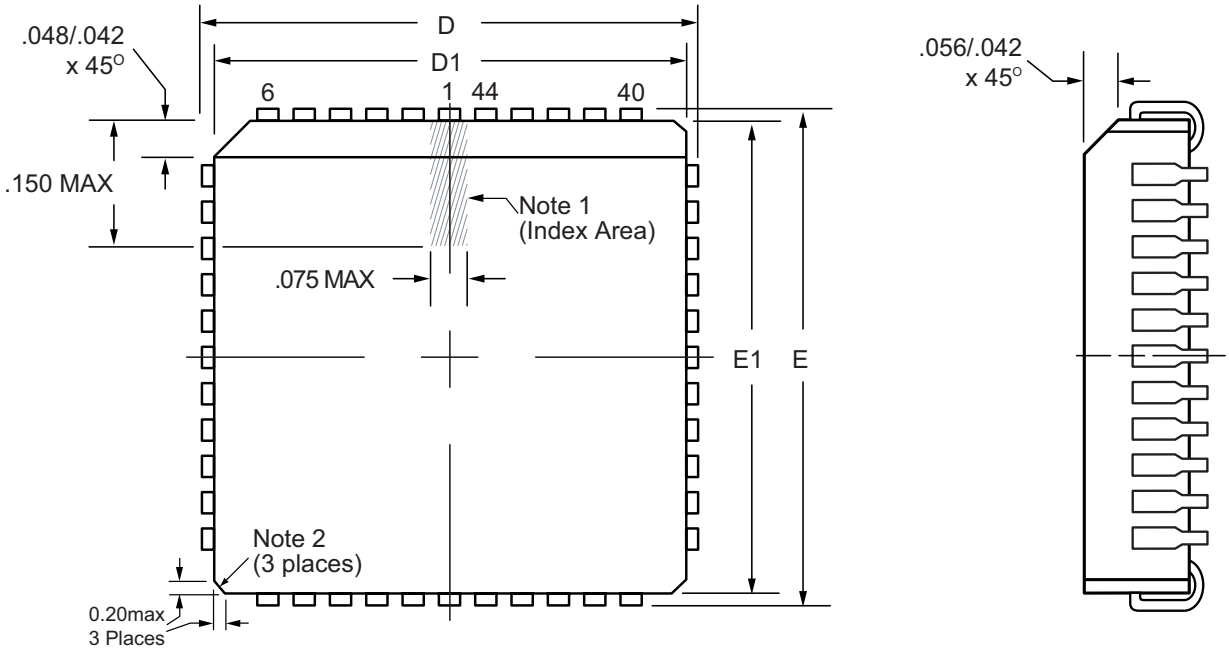
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HVOUT17	12	HVOUT28	23	Clock	34	HVOUT6
2	HVOUT18	13	HVOUT28	24	VSS	35	HVOUT7
3	HVOUT19	14	HVOUT30	25	VDD	36	HVOUT8
4	HVOUT20	15	HVOUT31	26	$\overline{LE}$	37	HVOUT9
5	HVOUT21	16	HVOUT32	27	Data In	37	HVOUT10
6	HVOUT22	17	N/C	28	$\overline{BL}$	39	HVOUT11
7	HVOUT23	18	Data Out	29	HVOUT1	40	HVOUT12
8	HVOUT24	19	N/C	30	HVOUT2	41	HVOUT13
9	HVOUT25	20	N/C	31	HVOUT3	42	HVOUT14
10	HVOUT26	21	N/C	32	HVOUT4	43	HVOUT15
11	HVOUT27	22	$\overline{POL}$	33	HVOUT5	44	HVOUT16

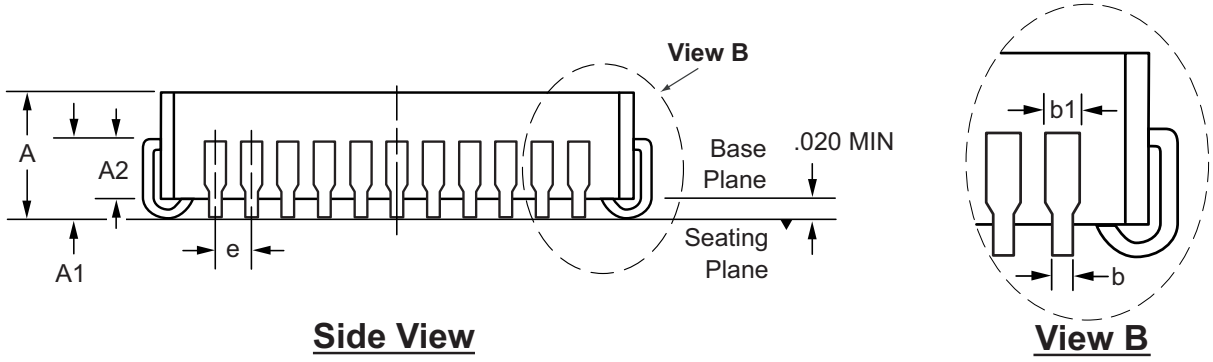
Pin Description (HV4622 - 44-J Lead PLCC)

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HVOUT16	12	HVOUT5	23	Clock	34	HVOUT27
2	HVOUT15	13	HVOUT4	24	VSS	35	HVOUT26
3	HVOUT14	14	HVOUT3	25	VDD	36	HVOUT25
4	HVOUT13	15	HVOUT2	26	$\overline{LE}$	37	HVOUT24
5	HVOUT12	16	HVOUT1	27	Data In	37	HVOUT23
6	HVOUT11	17	N/C	28	$\overline{BL}$	39	HVOUT22
7	HVOUT10	18	Data Out	29	HVOUT32	40	HVOUT21
8	HVOUT9	19	N/C	30	HVOUT31	41	HVOUT20
9	HVOUT8	20	N/C	31	HVOUT30	42	HVOUT19
10	HVOUT7	21	N/C	32	HVOUT29	43	HVOUT18
11	HVOUT6	22	$\overline{POL}$	33	HVOUT28	44	HVOUT17

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max.), .050in pitch





Note:

1. A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

2. Exact shape of this feature is optional.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC
	NOM	.172	.105	-	-	-	.690	.653	.690	.653	
	MAX	.180	.120	.083	.021	.036	.695	.656	.695	.656	

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

Drawings are not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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