High-Voltage Ring Generator

Ordering Information

Operating Voltage	Package Options
V_{PP1} - V_{NN1}	SOW-16
220V	HV440WG

Features

- ❏ 220V maximum operating voltage
- ❏ Integrated high voltage transistors
- ❏ Up to 70 V_{RMS} ring signal
- ❏ Pulse by pulse output over current protection
- ❏ 5 REN output capability
- ❏ External MOSFETs enhance output rating to 20 REN

Applications

- ❏ Microcontroller or microprocessor controlled high voltage ring generator
- ❏ Set-top/Street box ring generator
- ❏ Pair gain ring generator
- ❏ Wireless local loops
- ❏ Fibre in the loop/to the curb
- ❏ Coax cable loop

Absolute Maximum Ratings

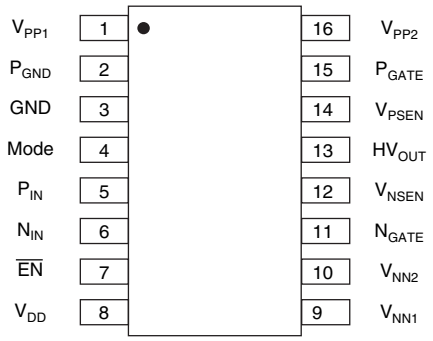
V_{PP1} - V_{NN1}, power supply voltage	+240V
V_{PP1}, positive high voltage supply	+120V
V_{PP2}, positive gate voltage supply	+120V
V_{NN1}, negative high voltage supply	-170V
V_{NN2}, negative gate voltage supply	-170V
V_{DD}, logic supply	+7.5V
Storage temperature	-65×C to +150×C
Power dissipation	800mW

General Description

The Supertex HV440 is a monolithic integrated circuit capable of generating up to 70V RMS sine wave output at frequencies of 15Hz to 60Hz with a load of 5 North American RENs. Its output rating can be enhanced to 20 North American RENs with the addition of two Supertex MOSFETs: one N-Channel MOSFET, the TN2524N8 and one P-Channel MOSFET, the TP2522N8.

The high voltage output P- and N-Channel transistors are controlled independently by the logic inputs P_{IN} and N_{IN}. Connecting the mode pin to ground will enable the device to be controlled with a single input, N_{IN}. This adds a 200ns deadband on the control logic to avoid cross conduction on the high voltage output. A logic high on N_{IN} will turn the high voltage P-Channel on and the N-Channel off. The high voltage outputs have pulse by pulse over current protection set by two external sense resistors. Nominal PWM logic input frequency is 100KHz.

Pin Configuration



Top View

SOW-16

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Electrical Characteristics

(Over operating supply voltage unless otherwise specified, T_A = 25°C.)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
V_{PP1}	High voltage positive supply	15		110	V	T_A = -40°C to +85°C
V_{PP2}	Positive linear regulator output voltage	V_{PP1} - 9.9		V_{PP1} -19.1	V	T_A = -40°C to +85°C
V_{NN1}	High voltage negative supply	V_{PP1} - 220		-110	V	T_A = -40°C to +85°C
V_{NN2}	Negative linear regulator output voltage	V_{NN1} + 5.6		V_{NN1} + 10.5	V	T_A = -40°C to +85°C
V_{DD}	Logic supply voltage	4.5		5.5	V	T_A = -40°C to +85°C
I_{PP1Q}	V_{PP1} quiescent current		250	400	µA	P_{IN} = N_{IN} = 0V, T_A = -40°C to +85°C
I_{NN1Q}	V_{NN1} quiescent current		250	550	µA	P_{IN} = N_{IN} = 0V, T_A = -40°C to +85°C
I_{DDQ}	V_{DD1} quiescent current			150	µA	P_{IN} = N_{IN} = 0V Mode = 0
I_{DDQ}	V_{DD1} quiescent current			60	µA	P_{IN} = N_{IN} = 0V Mode = 1
I_{PP1}	V_{PP1} operating current			1.7	mA	No load, V_{OUTP} and V_{OUTN} switching at 100KHz, T_A = -40°C to +85°C
I_{NN1}	V_{NN1} operating current			1.9	mA	No load, V_{OUTP} and V_{OUTN} switching at 100KHz, T_A = -40°C to +85°C
I_{DD}	V_{DD} operating current			1.0	mA	
I_{IL}	Mode logic input low current		25		µA	Mode = 0V
V_{IL}	Logic input low voltage	0		1.0	V	V_{DD} = 5.0V
V_{IH}	Logic input high voltage	4.0		5.0	V	V_{DD} = 5.0V

High Voltage Output

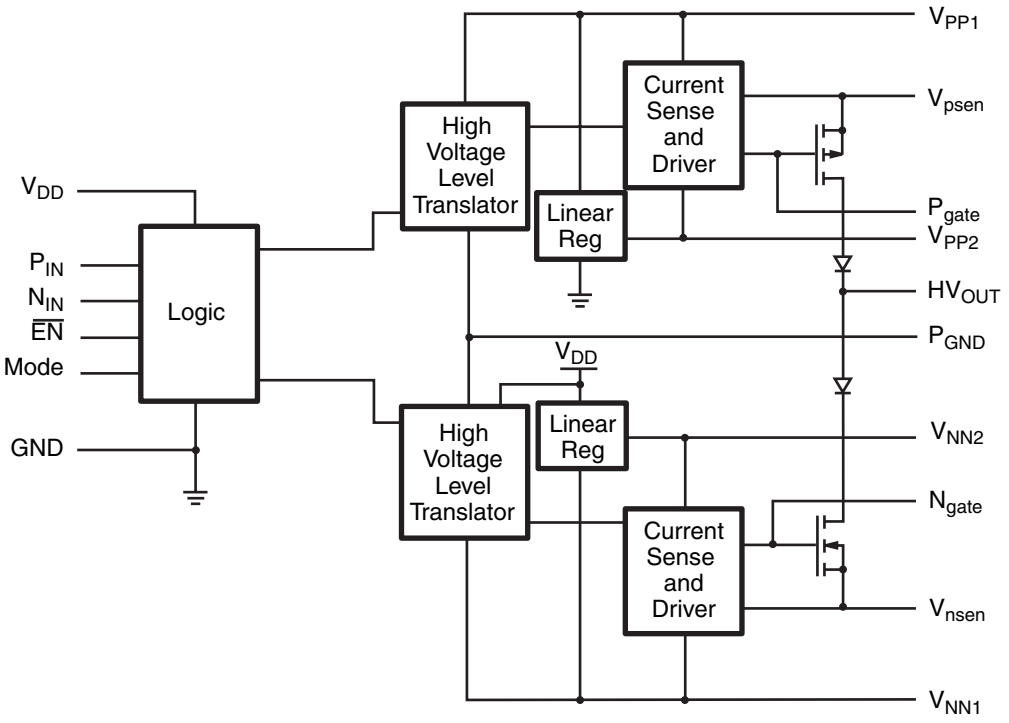
Symbol	Parameters	Min	Typ	Max	Unit	Conditions
R_{SOURCE}	V_{OUT}P source resistance		60	80	Ω	
	I_{OUT} = 100mA					
R_{SINK}	V_{OUT}P sink resistance		60	80	Ω	I_{OUT} = -100mA
ΔR/ΔT	Change in source/sink resistance over temperature		0.33		Ω/°C	T_A = -40°C to +85°C
$t_{d(ON)}$	HV_{OUT} delay time		150		ns	P_{IN} = high to low, Mode = high
t_{rise}	HV_{OUT} rise time			50	ns	P_{IN} = high to low
$t_{d(OFF)}$	HV_{OUT} delay time		200		ns	N_{IN} = low to high, Mode = high
t_{fall}	HV_{OUT} fall time			50	ns	N_{IN} = low to high
t_{db}	Logic deadband time			200	ns	Mode = low
V_{psen}	HV_{OUT} current source sense voltage	V_{PP1} -0.75	V_{PP1} -1.00	V_{PP1} - 1.25	V	
		V_{PP1} -0.67		V_{PP1} -1.31		T_A = -40°C to +85°C
V_{nsen}	HV_{OUT} current sink sense voltage	V_{NN1} + 0.75	V_{NN1} + 1.00	V_{NN1} + 1.25	V	
		V_{NN1} + 0.65		V_{NN1} + 1.33		T_A = -40°C to +85°C
t_{shortP}	HV_{OUT} off time when current source sense is activated			100	ns	
t_{shortN}	HV_{OUT} off time when current sink sense is activated			100	ns	
t_{WHOUT}	Minimum pulse width for HV_{OUT} at V_{PP1}			500	ns	T_A = -40°C to +85°C
t_{WLOUT}	Minimum pulse width for HV_{OUT} at V_{NN1}			500	ns	T_A = -40°C to +85°C

Truth Table

N_{IN}	P_{IN}	Mode	$\overline{EN}$	HV_{OUT}
L	L	H	L	V_{PP1}
L	H	H	L	High Z
H	L*	H	L	–
H	H	H	L	V_{NN1}
L	X	L	L	V_{NN1}
H	X	L	L	V_{PP1}
X	X	X	H	High Z

**This state will short V_{PP1} to V_{NN1} and should therefore be avoided.*

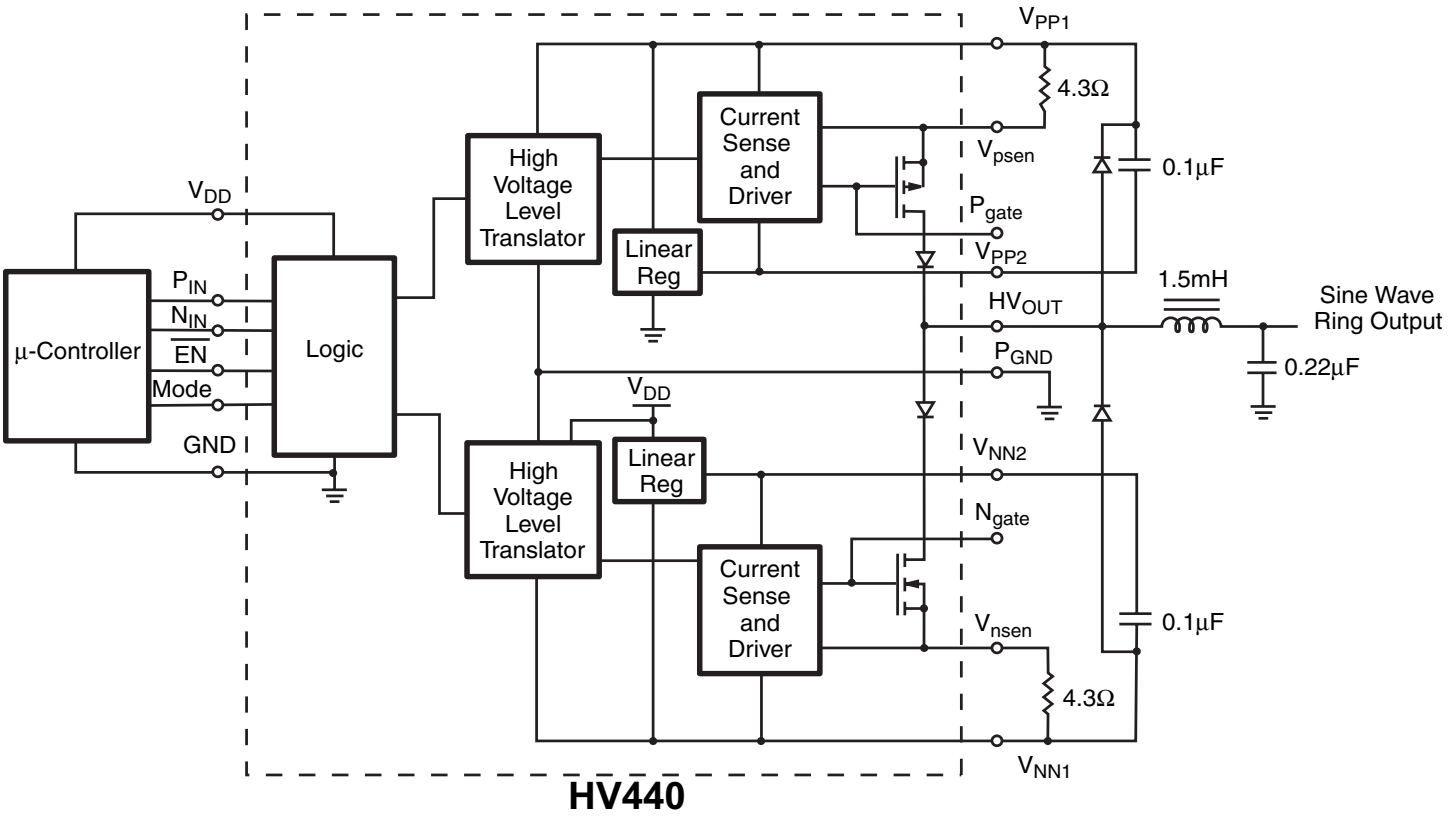
Block Diagram



Pin Description

V_{PP1}	Positive high voltage supply.
V_{PP2}	Positive gate voltage supply. Generated by an internal linear regulator. A 0.1µF capacitor should be connected between V_{PP2} and V_{PP1}.
V_{NN1}	Negative high voltage supply.
V_{NN2}	Negative gate voltage supply. Generated by an internal linear regulator. A 0.1µF capacitor should be connected between V_{NN2} and V_{NN1}.
V_{DD}	Logic supply voltage.
GND	Low voltage ground.
PGND	High voltage power ground.
P_{IN}	Logic control input. When mode is high, logic input high turns OFF output high voltage P-Channel.
N_{IN}	Logic control input. When mode is high, logic input high turns ON output high voltage N-Channel.
EN	Logic enable bar input. Logic low enables IC.
Mode	Logic mode input. Logic low activates 200nsec deadband. When mode is low, N_{IN} turns on and off the high voltage N- and P-Channels. Pin is not used and should be connected to V_{DD} or ground.
HV_{OUT}	High voltage output. Voltage swings from V_{PP1} to V_{NN1}.
V_{psen}	Pulse by pulse over current sensing for internal P-Channel MOSFET.
V_{nsen}	Pulse by pulse over current sensing for internal N-Channel MOSFET.
P_{gate}	Gate drive for external P-channel MOSFET.
N_{gate}	Gate drive for external N-channel MOSFET.

Typical Application Circuit



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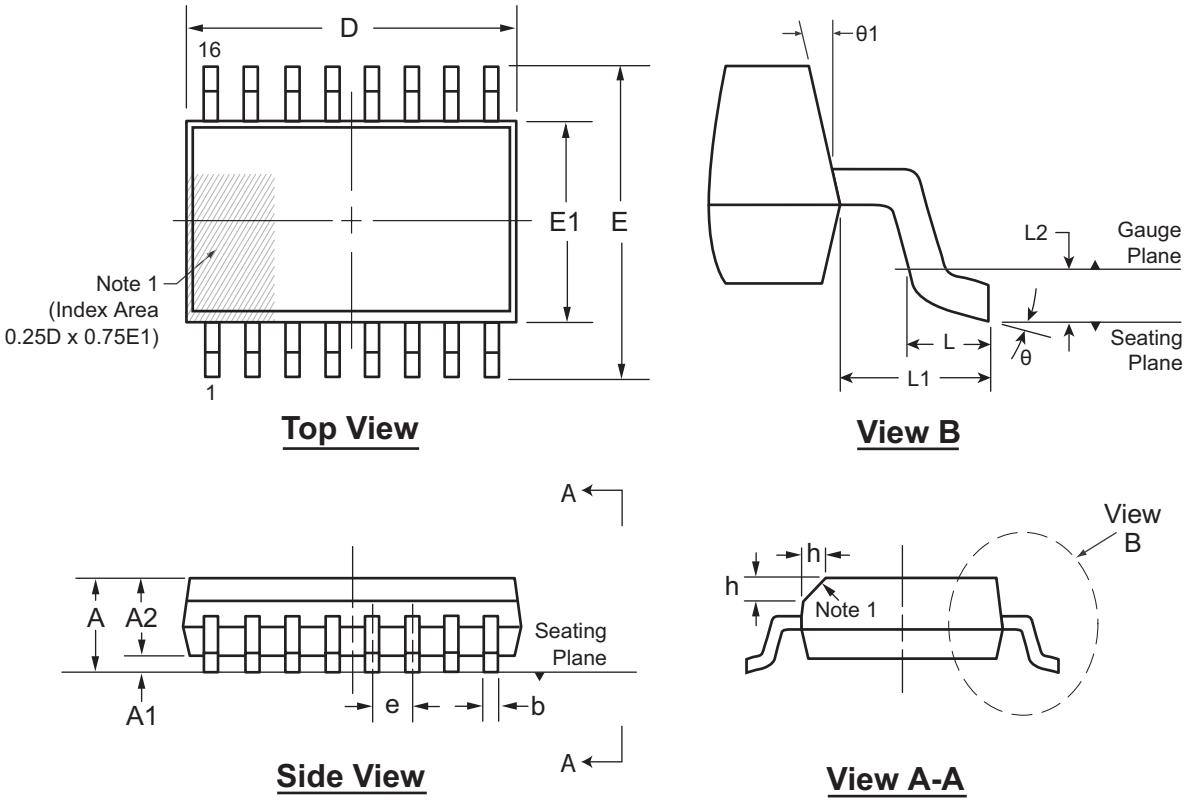
16-Lead SOW (Wide Body) Package Outline (WG)

10.30x7.50mm body, 2.65mm height (max), 1.27mm pitch



Note 1:

This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15	0.10	2.05	0.31	10.10	9.97	7.40	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	10.30	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55	0.51	10.50	10.63	7.60		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AA, Issue E, Sep. 2005.

Drawings are not to scale.

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Doc. #: DSPD-16SOWWG
B032607