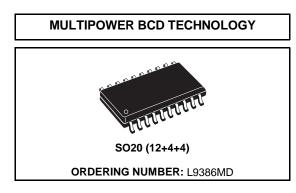


DUAL INTELLIGENT POWER LOW SIDE SWITCH

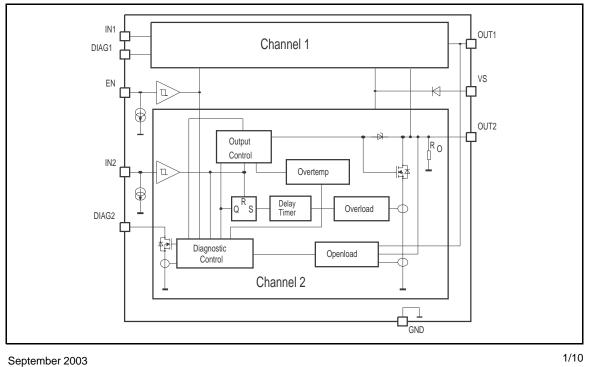
- DUAL POWER LOW SIDE DRIVER WITH 2 x 5A
- LOW R_{DSON} TYPICALLY 200m Ω @ T_J = 25°C
- INTERNAL OUTPUT CLAMPING DIODES VFB=50V FOR INDUCTIVE RECIRCULATION
- LIMITED OUTPUT VOLTAGE SLEW RATE FOR LOW EMI
- µP COMPATIBLE ENABLE AND INPUT
- WIDE OPERATING SUPPLY VOLTAGE RANGE 4.5V TO 45V
- REAL TIME DIAGNOSTIC FUNCTIONS
 OUTPUT SHORTED TO GND
 - OUTPUT SHORTED TO VSS
 - OPEN LOAD
 - LOAD BYPASS
 - OVERTEMPERATURE
- DEVICE PROTECTION FUNCTIONS
 - OVERLOAD DISABLE
 - REVERSE BATTERY UP TO -16V @ VS
 - THERMAL SHUTDOWN



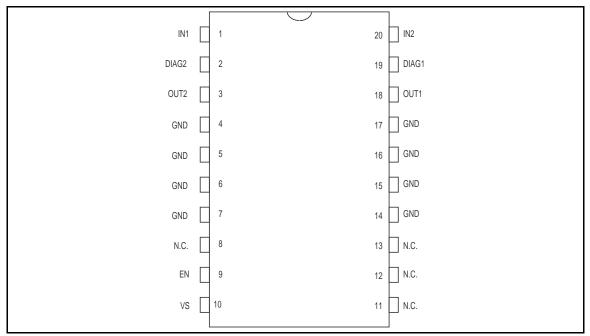
DESCRIPTION

The L9386MD is a monolithic integrated dual low side driver realized in an advanced Multipower-BCD mixed technology. It is especially intended to drive valves in automotive environment. Its inputs are μ P compatible for easy driving. Particular care has been taken to protect the device against failures, to avoid electro-magnetic interferences and to offer extensive real time diagnostic.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS (no damage or latch)

| Symbol | Parameter | Value | Unit |
|--------------------|---|------------------|------|
| VS _{DC} | DC supply voltage | -16 to 45 | V |
| VS _{TR} | Transient supply voltage ($t \le 500$ ms) | 60 | V |
| V _{IN,EN} | Input voltage ($ \leq 10mA $) | -1.5 to 6 | V |
| VD _{DC} | Diagnostic DC output voltage ($ \le $ 50mA) | -0.3 to 16 | V |
| VO _{DC} | DC output voltage | 45 | V |
| VO _{TR} | Transient output voltage ($R_L \ge 4\Omega$) | 60 | V |
| lo | Output load current | internal limited | |
| I _{OR} | Reverse output current limited by load | -4 | А |
| EO | Switch-off energy for inductive loads ($t_{EO} = 250 \mu s$, T = 5ms) | 50 | mJ |
| T _{jEO} | Junction temperature during switch-off $\sum t = 30$ min | 175 | °C |
| Tj | Junction temperature | -40 to +150 | °C |
| Ta | Storage temperature | -55 to +150 | °C |

THERMAL DATA

| Symbol | Parameter | Value | Unit |
|-------------------------|--|------------|------|
| T _{jDIS} | Thermal disable junction temperature threshold | 160 to 190 | °C |
| R _{th j} -pins | Thermal resistance junction to pins | 14 | °C/W |

ELECTRICAL CHARACTERISTICS (Operating Range) - The electrical characteristics are valid within the below defined operative range, unless otherwise specified.

| Symbol | Parameter | Test Condition | Min. | Тур. | Max. | Unit |
|--------|--------------------------------------|----------------|------|------|------|------|
| Vs | Board supply voltage | | 4.5 | 12 | 32 | V |
| VD | Stabilized diagnostic output voltage | | -0.3 | 5 | 16 | V |
| Tj | Junction Temperature | | -40 | | 150 | °C |

2/10

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Value T _{i1} | | | Unit |
|---------------------------|--|---|---------------------------|----------------------------|---------------------------|-----------------|
| | | | Min. | Тур. | Max. | |
| IS _{SB} | Static standby supply current | b) c) V_{EN} = L, $VO \le VO_{uv}$ | | 0.73 | 1.5 15 | mA mA |
| IS | DC supply current | b) c) V _{EN} = V _{IN} = H | | 1.3 | 5 15 | mA mA |
| VDL | Diagnostic ouput low voltage | b) I _D = 2mA c) I _D = 1mA | | 0.35 | 0.5 | V |
| ID _{LE} | Diagnostic output leakage current | $\begin{array}{l} VS = 0V \text{ or } VS = \text{open}; \\ VD = 5.5V \ T_i \leq 125^\circ C \end{array}$ | | 0.1 | 2 | μA |
| ID | Diagnostic output current capability | $VD \le 16V DIAG = L$ | 2 | 6 | 30 | mA |
| VO _{UV} | Open load voltage threshold | $V_{\text{EN}} = X, \ V_{\text{IN}} = L$ | 0.51 x VS | 0.55 x VS | 0.59 x VS | V |
| ΔVO _{UV1,2} | Open load difference voltage threshold | b) VEN = X, $V_{IN1,2}$ = L VS \geq VO _C \geq VO _{UV} VO _C = output voltage of other channel | VO _C - 0.9V | VO _C - 1.25V | VO _C - 1.6V | V ¹⁾ |
| | | c) | VO _C - 0.7V | VO _C - 1.25V | VO _C - 1.8V | V |
| IO _{UC} | Open load current threshold | a) V _{EN} = V _{IN} = H c) | 100 20 | 320 | 480 | mA mA |
| IO _{OC} | Over load current threshold | b) | 5 | 7 | | А |
| VO _{CL} | Output voltage during clamping | $IO_{CL} \ge 100 mA$ | 45 | 52 | 60 | V |
| Son, off | Output (fall, rise) slew rate | a) Fig. 2 | 200 | 1500 | 3200 | V/ms |
| R _{IO} | Internal output pull down resistor | V _{EN} = L 10 2 | | 20 | 40 | KΩ |
| R _{DSON} | Output on resistance | $\begin{array}{l} \text{VS} > 9.5 \text{V} \ \text{IO} = 2 \text{A} \\ \text{T}_{j} = 25^{\circ} \text{C} \\ \text{T}_{j} = 150^{\circ} \text{C} \end{array}$ | | 200 | 300 500 | mΩ mΩ |
| V _{(EN,IN)L} | Logic input low voltage | I _{EN, IN} ≤ 10mA b) c) | -1.5 -1.5 | | 1 0.5 | V V |
| V _(EN,IN) H | Logic input high voltage | | 2.2 | | 5.5 | V |
| V _{(EN,IN)hys} | Logic input hysteresis | | 0.2 | 0.4 | 1 | V |
| I _{EN} | Enable input sink current | $1V \leq V_{EN} \leq 5.5V$ | 10 | 30 | 60 | μA |
| I _{IN} | Logic input sink current | $1V \leq V_{IN} \leq 5.5V$ | 40 | 95 | 180 | μA |
| t _{D ON} | Output delay ON time | a) Fig. 2 | | 4 | 25 | μs |
| t _{D OFF} | Output delay OFF time | a) Fig. 2 | 5 | 15 | 30 | μs |
| t _{D H-L, Diag.} | Diag. delay output OFF time | a) Fig. 2 | 5 | 30 | 65 | μs |
| t _D iOu | Diagnostic open load delay time | a) Fig. 4 | | 8 | 50 | μs |
| t _{DOL} | Diagnostic overload delay switch-off time | a) Fig. 1 | 50 | 160 | 300 | μs |

a) $9V \le V_S \le 16V$ (Nominal operating range) $R_L \le 6\Omega$, $I_0 \le IO_{CC}$ b) $6.5V \le V_S \le 16V$ (Diagnostic operation range) c) $4.5V \le V_S < 6.5V$ and $16V < V_S \le 32V$ (Extended operation range) 1) Limit under evaluation.



| Conditions | | EN | IN | Out | Diag. |
|---|-----------------------------|--------|--------|------------|--------|
| Normal function | | L | Х | off | L |
| | | н | L | off | L |
| | | Н | Н | on (*) | Н |
| GND short | $VO_{typ} < 0.55V$ | L | Х | off | Н |
| Load bypass | $\Delta VO_{1,2} \ge 1.25V$ | Н | L | off | Н |
| Open load | IO _{typ} < 320mA | Н | Н | on (*) | L |
| T _{j typ} ≥ 175°C Oertemperature (**) | | X X | L H | off off | H L |
| Latched Over load IO _{min} > 5A | | Х | Н | off | L |
| Reset over load latch | | Х | | D.C. | D.C. |

DIAGNOSTIC TABLE (Operating range: $4.5V \le V_S \le 32V$)

(*) for 4.5V \leq VS < 6.5V, IO \leq 2A diag. table is valid.

(**) If one diag. status shows the overtemp. recognition, in parallel this output will be switched OFF internally. The corresponding channel should be switched OFF additional by its Input or ENABLE signal, otherwise the overload latch will be set after t_{DOL} is passed. This behaviour will be related to the overdrop sensing which will be used as over load recognition.

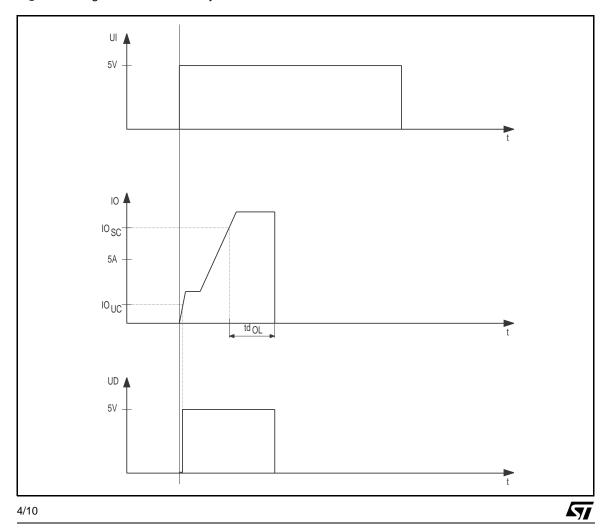
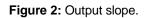


Figure 1: Diagnostic overload delay time



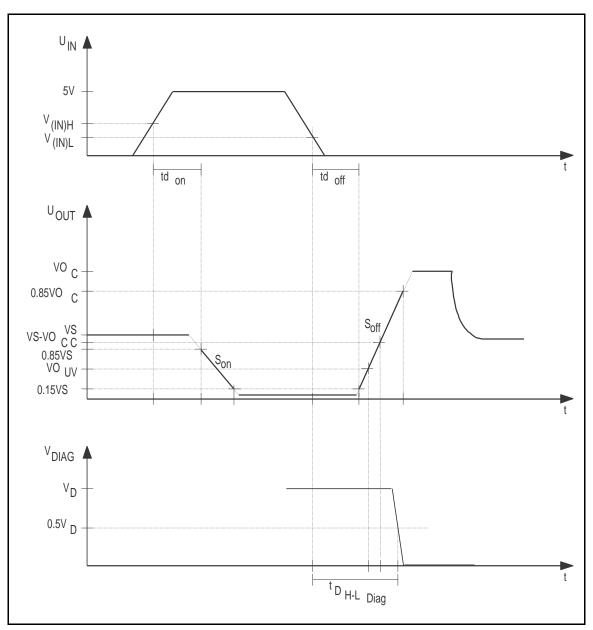


Figure 3: Block diagram - Open load voltage detection.

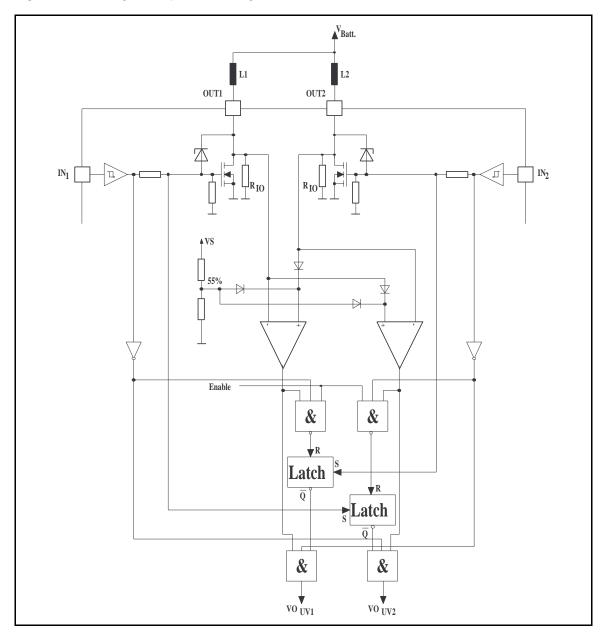
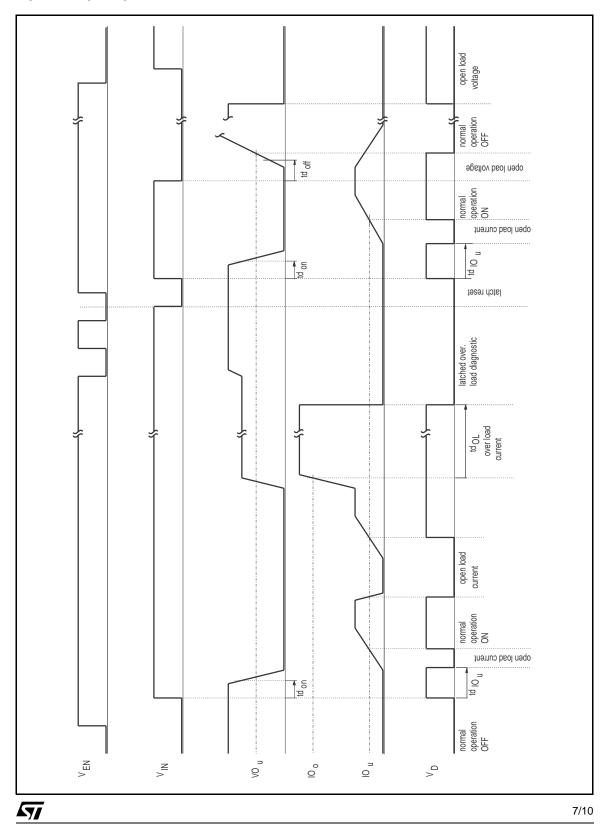


Figure 4: Logic diagram.



CIRCUIT DESCRIPTION

The L9386MD is a dual low side driver for inductive loads like valves in automotive environment. The device is enabled by a common CMOS compatible ENABLE high signal. The internal pull down current sources at the ENABLE and INPUT pins protect the device in open input conditions against malfunctions. An output slope limitation for du/dt is implemented to reduce the EMI. An integrated active flyback voltage limitation clamps the output voltage during the flyback phase to 50V.

Each driver is protected against short circuit and thermal overload. In short circuit condition the output will be disabled after a short delay time t_{DOL} to suppress spikes. This disable is latched until a negative slope occure at the correspondent input pin. The thermal disable for $T_J > 175^{\circ}C$ of the output will be reseted if the junction temperature decreases about 20°C below the disable threshold temperature.

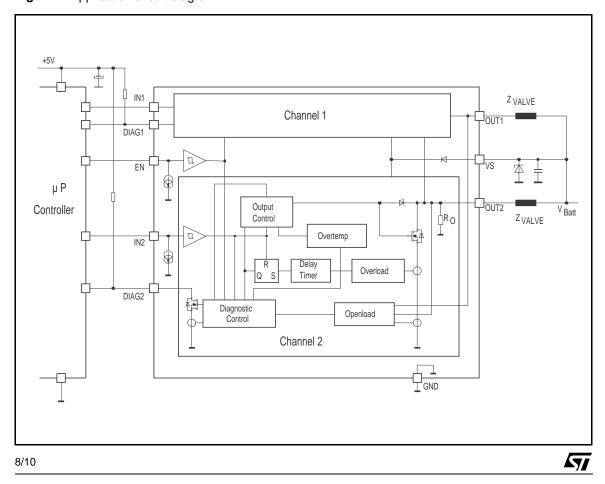
For the real time error diagnosis the voltage and the current of the outputs are compared with internal fixed values VO_{UV} for OFF and IO_{UC} for ON conditions to recognize open load ($R_L \ge 20K\Omega$, $R_L > 38\Omega$) in ON and OFF conditions. The diagnostic **Figure 5:** Application circuit diagram.

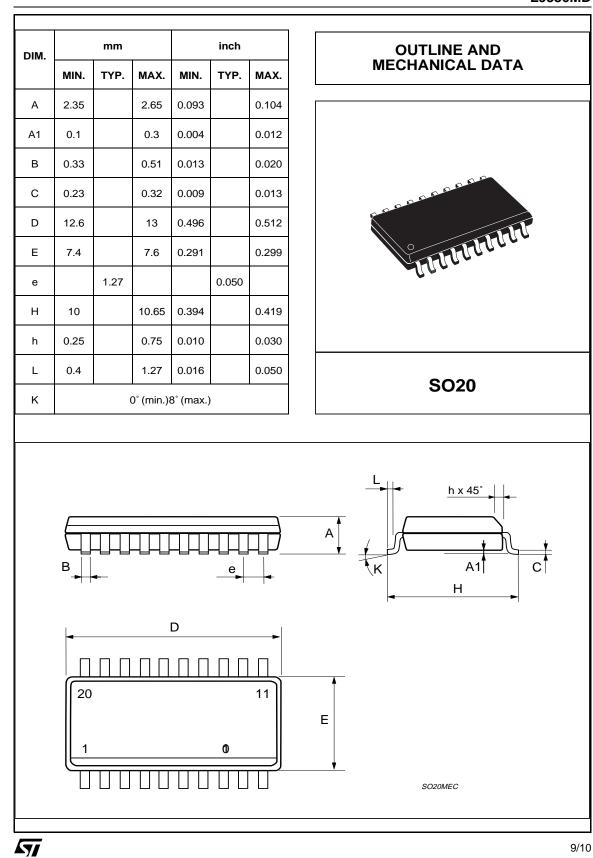
operates also in the extended supply voltage rang of $4.5V \le VS \le 32V$.

Also the output voltages VO_{1,2} are compared against each other in OFF condition with a fixed offset of Δ VOUV 1,2 to recognize GND bypasses. To suppress mail Δ VO diagnoses during the flyback phases of the compared output, the Δ VO diagnostic includes a latch function. Reaching the flyback clamping voltage VO_C the diagnostic signal is reseted by a latch. To activate again this kind of diagnostic a low signal at the correspondent INPUT or the ENABLE pin must occur (see also Fig.3).

The diagnostic output level in connection with different ENABLE and INPUT conditions allows to recognize different fail states, like overtemp, short to VSS, short to GND, bypass to GND and disconnected load (see also page 7 diagnostic table).

The diagnostic output is also protected against short to UD_{max} . Oversteping the over load current threshold IO_o, the output current will be limited internally during the diagnostic overload delay switch-off time t_{DOL}.





Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners © 2003 STMicroelectronics - All rights reserved

STMicroelectronics GROUP OF COMPANIES

Australia – Belgium - Brazil - Canada - China – Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States

www.st.com

10/10