

# DATA SHEET

## **UBA2024**

**Half-bridge power IC for CFL lamps**

Product specification  
Supersedes data of 2003 Aug 13

2004 Feb 03

# Half-bridge power IC for CFL lamps

# UBA2024

### FEATURES

- Integrated half-bridge power transistors
- Integrated bootstrap diode
- Integrated low-voltage supply
- Maximum voltage of 550 V
- Adjustable oscillator frequency
- Soft start
- Minimum glow time control.

### GENERAL DESCRIPTION

The UBA2024 is a high-voltage monolithic integrated circuit made in the EZ-HV SOI process. The IC is designed for driving CFL lamps in a half-bridge configuration.

The IC features a soft start function, an adjustable internal oscillator and an internal drive function with a high-voltage level shifter for driving the half-bridge.

To guarantee an accurate 50% duty cycle, the oscillator signal is passed through a divider before being fed to the output drivers.

### APPLICATIONS

- Driver for any kind of load in a half-bridge configuration
- Especially for electronically self-ballasted Compact Fluorescent Lamps (CFL) for lamp currents up to 220 mA (RMS) under the restriction that the maximum junction temperature is not exceeded.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA2024P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

### BLOCK DIAGRAM

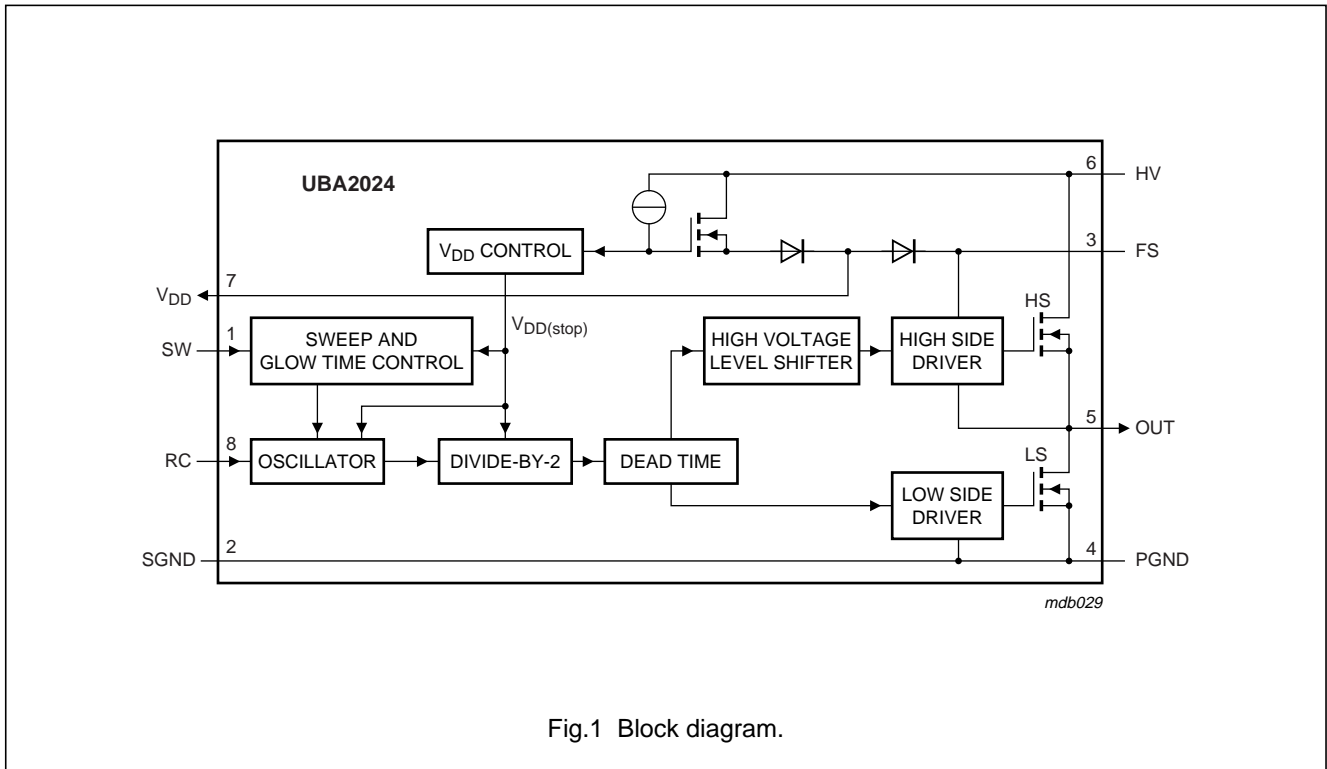


Fig.1 Block diagram.

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**PINNING**

SYMBOL	PIN	DESCRIPTION
SW	1	sweep timing input
SGND	2	signal ground
FS	3	high-side floating supply output
PGND	4	power ground
OUT	5	half-bridge output
HV	6	high-voltage supply
V <sub>DD</sub>	7	internal low-voltage supply output
RC	8	internal oscillator input

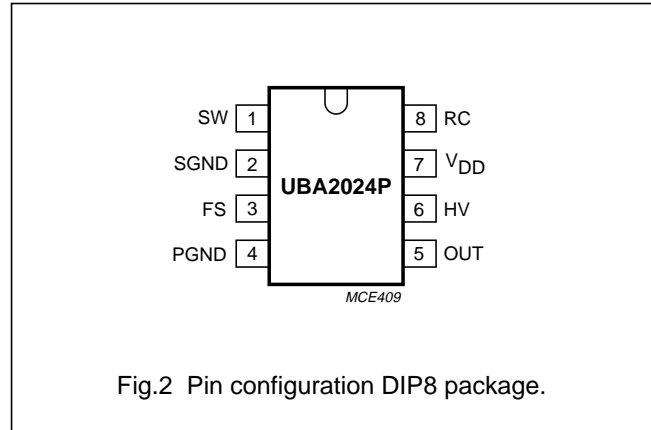


Fig.2 Pin configuration DIP8 package.

**FUNCTIONAL DESCRIPTION**

**Supply voltage**

The UBA2024 is powered by a supply voltage applied to pin HV. The IC generates its own low supply voltage for the internal circuitry and therefore, an additional external low-voltage supply is not required.

**Start-up state**

With an increase of the supply voltage on pin HV, the IC enters the start-up state. In the start-up state the high-side power transistor is not conducting and the low-side power transistor is switched on. The internal circuit is reset and the capacitors on the bootstrap pin FS and low-voltage supply pin V<sub>DD</sub> are charged. Pins RC and SW are switched to ground. The start-up state is defined until  $V_{DD} = V_{DD(start)}$ .

**Sweep mode**

The IC enters the sweep mode at the moment the voltage on pin V<sub>DD</sub> > V<sub>DD(start)</sub>. The capacitor on pin SW is charged by I<sub>sweep</sub> and the half-bridge circuit starts oscillating. The circuit enters the start-up state again when the voltage on pin V<sub>DD</sub> < V<sub>DD(stop)</sub>.

**Reset**

A DC reset circuit is incorporated in the high-side driver. The high-side transistor is switched off when the voltage on pin FS is below the high-side lockout voltage V<sub>FS(lock)</sub>.

**Oscillation**

The oscillation is based upon the 555-timer function. With the external resistor R<sub>OSC</sub> and capacitor C<sub>OSC</sub> (see Fig.5) a self oscillating circuit is made, where R<sub>OSC</sub> and C<sub>OSC</sub> determine the oscillating frequency.

To realize an accurate 50% duty cycle, an internal divider is used. Due to the presence of the divider, the bridge frequency is half the oscillator frequency.

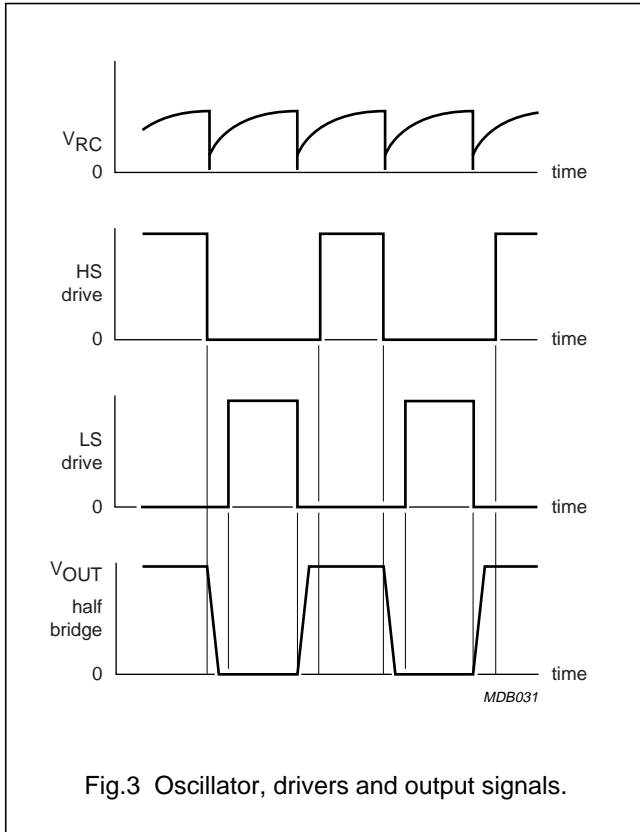
The output voltage of the bridge will change at the falling edge of the signal on pin RC. The design equation for the half-bridge frequency is:

$$f_{osc} = \frac{1}{k \times R_{OSC} \times C_{OSC}}$$

An overview of the oscillator signal, internal LS and HS drive signals and the output is given in Fig.3.

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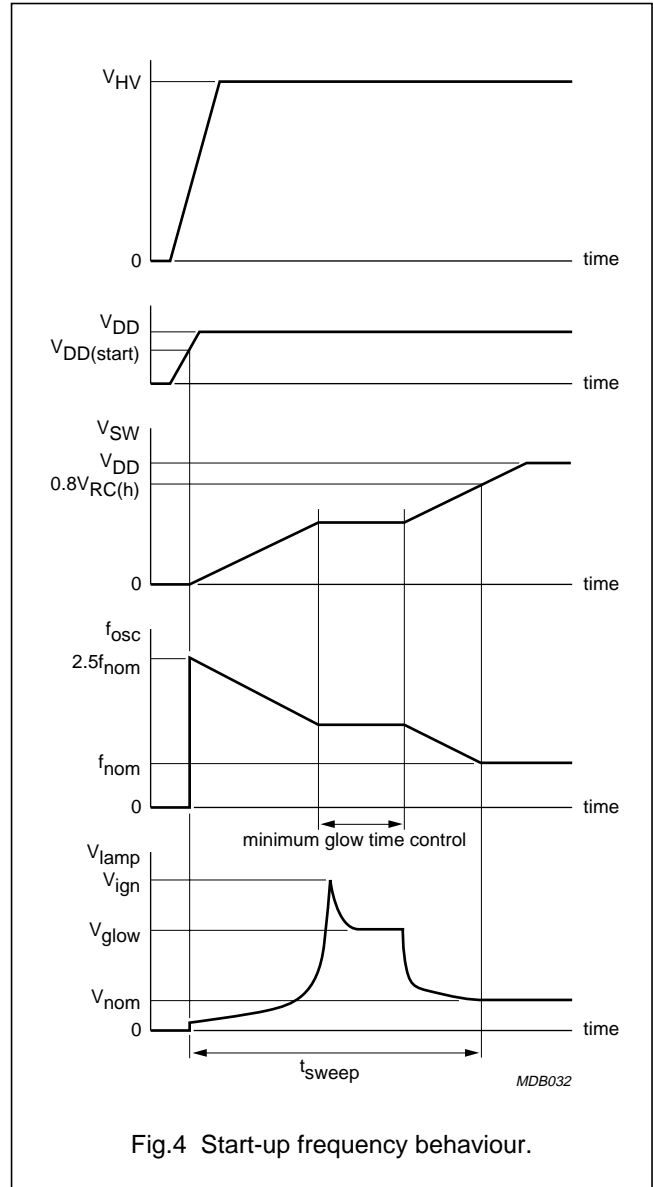


When entering the sweep mode, the oscillator starts at 2.5 times the nominal bridge frequency and sweeps down to the nominal bridge frequency  $f_{nom}$ ; see Fig.4. During this continuously decreasing of the frequency, the circuit approaches the resonance frequency of the load. This causes a high voltage across the load, which normally ignites the lamp.

The sweep time  $t_{sweep}$  is determined by the charge current  $I_{ch(sw)}$  and the external capacitor  $C_{SW}$ . The sweep to resonance time should be much larger than the settling time of the supply voltage on pin HV to guarantee that the full high-voltage is present at the moment of ignition.

The amplitude of the RC oscillator is equal to the minimum value of  $V_{RC(h)}$  and  $V_{SW} + 0.4 \times V_{RC(h)}$ .

During the sweep time a current is flowing through the lamp electrodes for pre-heating the filaments.



**Glow time control**

The drawback of cold-started CFL lamps is its inherent glow time which reduces the switching lifetime of the electrodes (lamp). To make this glow phase as short as possible, the maximum power is given to the lamp during the glow time via a special control; see Fig.4.

**Non-overlap time**

The non-overlap time is defined as the time that both MOSFETs are not conducting. The non-overlap time is internally fixed.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are measured with respect to SGND; positive currents flow into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>HV</sub>	high-voltage supply voltage	normal operation	–	373	V
		mains transients during 0.5 s	–	550	V
V <sub>FS</sub>	floating supply voltage		V <sub>HV</sub>	V <sub>HV</sub> + 14	V
V <sub>DD</sub>	low-voltage output supply voltage	DC supply	0	14	V
I <sub>DD</sub>	low-voltage output supply current	peak value is internally limited; T <sub>amb</sub> = 25 °C	0	5	mA
V <sub>PGND</sub>	power ground voltage	referenced to SGND	–1	+1	V
V <sub>i(RC)</sub>	internal oscillator input voltage on pin RC	I <sub>i(RC)</sub> < 1 mA	0	V <sub>DD</sub>	V
V <sub>i(SW)</sub>	sweep time input voltage on pin SW	I <sub>i(SW)</sub> < 1 mA	0	V <sub>DD</sub>	V
SR	slew rate output on pin OUT	repetitive	–4	+4	V/ns
T <sub>j</sub>	junction temperature		–40	+150	°C
T <sub>amb</sub>	ambient temperature		–40	+150	°C
T <sub>stg</sub>	storage temperature		–55	+150	°C
V <sub>esd(HBM)</sub>	HBM electrostatic discharge voltage on pins HV and V <sub>DD</sub> , SW, RC, FS and OUT	note 1	–	1000	V
			–	2500	V
V <sub>esd(MM)</sub>	MM electrostatic discharge voltage on pins FS, HV, V <sub>DD</sub> , SW, RC and OUT	note 2	–	200	V
			–	250	V

**Notes**

- In accordance with the Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
- In accordance with the Machine Model (MM): equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor and a 0.75 μH inductor.

**QUALITY SPECIFICATION**

Quality in accordance with *SNW-FQ-611*.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air; note 1	95	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case	note 1	16	K/W

**Note**

- In accordance with IEC 60747-1.

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**CHARACTERISTICS**T<sub>j</sub> = 25 °C; all voltages are measured with respect to SGND; positive currents flow into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>High-voltage supply</b>						
V <sub>HV</sub>	high-voltage supply voltage	t < 0.5 s and I <sub>HV</sub> < 30 μA	0	–	550	V
V <sub>FS</sub>	floating supply voltage	t < 0.5 s and I <sub>FS</sub> < 30 μA	0	–	564	V
<b>Low-voltage supply</b>						
V <sub>DD</sub>	low-voltage output supply voltage	V <sub>HV</sub> = 100 V; R <sub>OSC</sub> = ∞; V <sub>SW</sub> = V <sub>DD</sub> ; V <sub>RC</sub> = 0 V	11.7	12.5	13.3	V
<b>Start-up state</b>						
I <sub>HV</sub>	high-voltage supply current	V <sub>HV</sub> = 100 V; R <sub>OSC</sub> = ∞; V <sub>SW</sub> = V <sub>DD</sub> ; V <sub>RC</sub> = 0 V	–	–	0.39	mA
V <sub>DD(start)</sub>	start of oscillation voltage		10	11	12	V
V <sub>DD(stop)</sub>	stop of oscillation voltage		8	8.5	9	V
V <sub>DD(hys)</sub>	start-stop hysteresis voltage		2	2.5	3	V
<b>Output stage</b>						
R <sub>HS(on)</sub>	HS transistor on-resistance	V <sub>HV</sub> = 310 V; I <sub>d</sub> = 100 mA	–	9.7	11	Ω
R <sub>LS(on)</sub>	LS transistor on-resistance	I <sub>d</sub> = 100 mA	–	8.5	9.4	Ω
V <sub>HS(d)</sub>	HS body diode forward voltage	I <sub>f</sub> = 200 mA	1.4	1.8	2.2	V
V <sub>LS(d)</sub>	LS body diode forward voltage	I <sub>f</sub> = 200 mA	1.2	1.6	2.0	V
I <sub>HS(sat)</sub>	HS transistor saturation current	V <sub>ds</sub> = 30 V; T <sub>j</sub> ≤ 125 °C; V <sub>HV</sub> = 310 V	900	–	–	mA
I <sub>LS(sat)</sub>	LS transistor saturation current	V <sub>ds</sub> = 30 V; T <sub>j</sub> ≤ 125 °C	900	–	–	mA
V <sub>boot</sub>	bootstrap diode drop voltage	I <sub>f</sub> = 1 mA	0.7	1.0	1.3	V
t <sub>no</sub>	non overlap time		1	1.35	1.7	μs
V <sub>FS(lock)</sub>	floating supply lock-out voltage		3.6	4.2	4.8	V
I <sub>FS</sub>	floating supply current	V <sub>HV</sub> = 310 V; V <sub>FS</sub> = 12.2 V	10	14	18	μA
<b>Internal oscillator</b>						
f <sub>osc</sub>	frequency range bridge oscillator	V <sub>SW</sub> = V <sub>DD</sub>	–	–	60	kHz
f <sub>osc(nom)</sub>	nominal frequency bridge oscillator	R <sub>OSC</sub> = 100 kΩ; C <sub>OSC</sub> = 220 pF; V <sub>SW</sub> = V <sub>DD</sub>	40.05	41.32	42.68	kHz
Δf <sub>osc(nom)</sub>	bridge oscillator frequency variation with temperature	R <sub>OSC</sub> = 100 kΩ; C <sub>OSC</sub> = 220 pF; ΔT = –20 to +150 °C	–	2	–	%
k <sub>h</sub>	high-level trip point factor		0.382	0.395	0.408	
V <sub>RC(h)</sub>	high-level trip point voltage on pin RC	V <sub>RC(h)</sub> = k <sub>h</sub> × V <sub>DD</sub>	4.58	4.94	5.29	V
k <sub>l</sub>	low-level trip point factor		0.030	0.033	0.036	
V <sub>RC(low)</sub>	low-level trip point voltage on pin RC	V <sub>RC(l)</sub> = k <sub>l</sub> × V <sub>DD</sub>	0.367	0.413	0.458	V
k <sub>osc</sub>	oscillator constant	R <sub>OSC</sub> = 100 kΩ; C <sub>OSC</sub> = 220 pF	1.065	1.1	1.135	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Sweep function</b>						
$I_{ch(sw)}$	charge current for sweep	$V_{SW} = 0 V$	215	280	345	nA
$t_{sweep}$	sweep time	$C_{SW} = 33 nF; V_{DD} = 12.2 V$	0.28	0.35	0.45	s

## APPLICATION INFORMATION

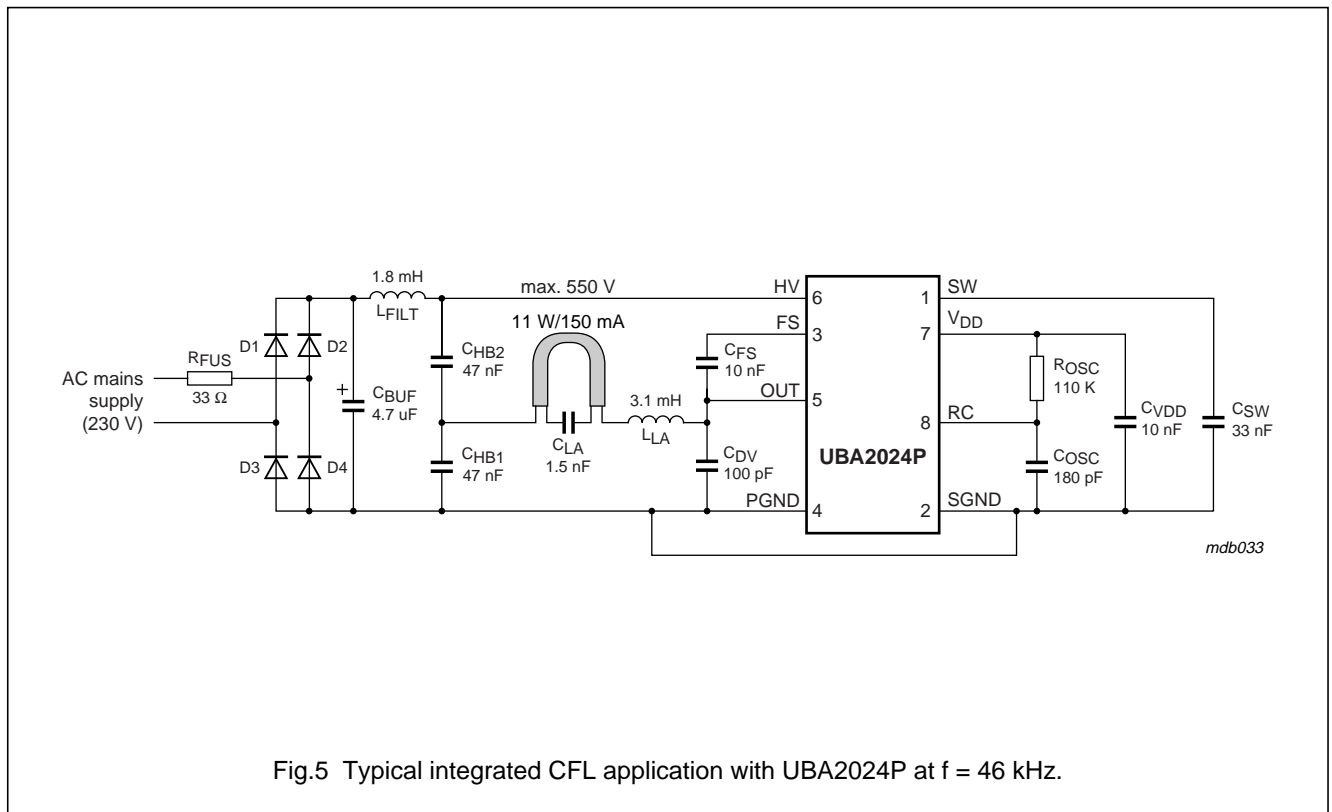


Fig.5 Typical integrated CFL application with UBA2024P at  $f = 46 \text{ kHz}$ .

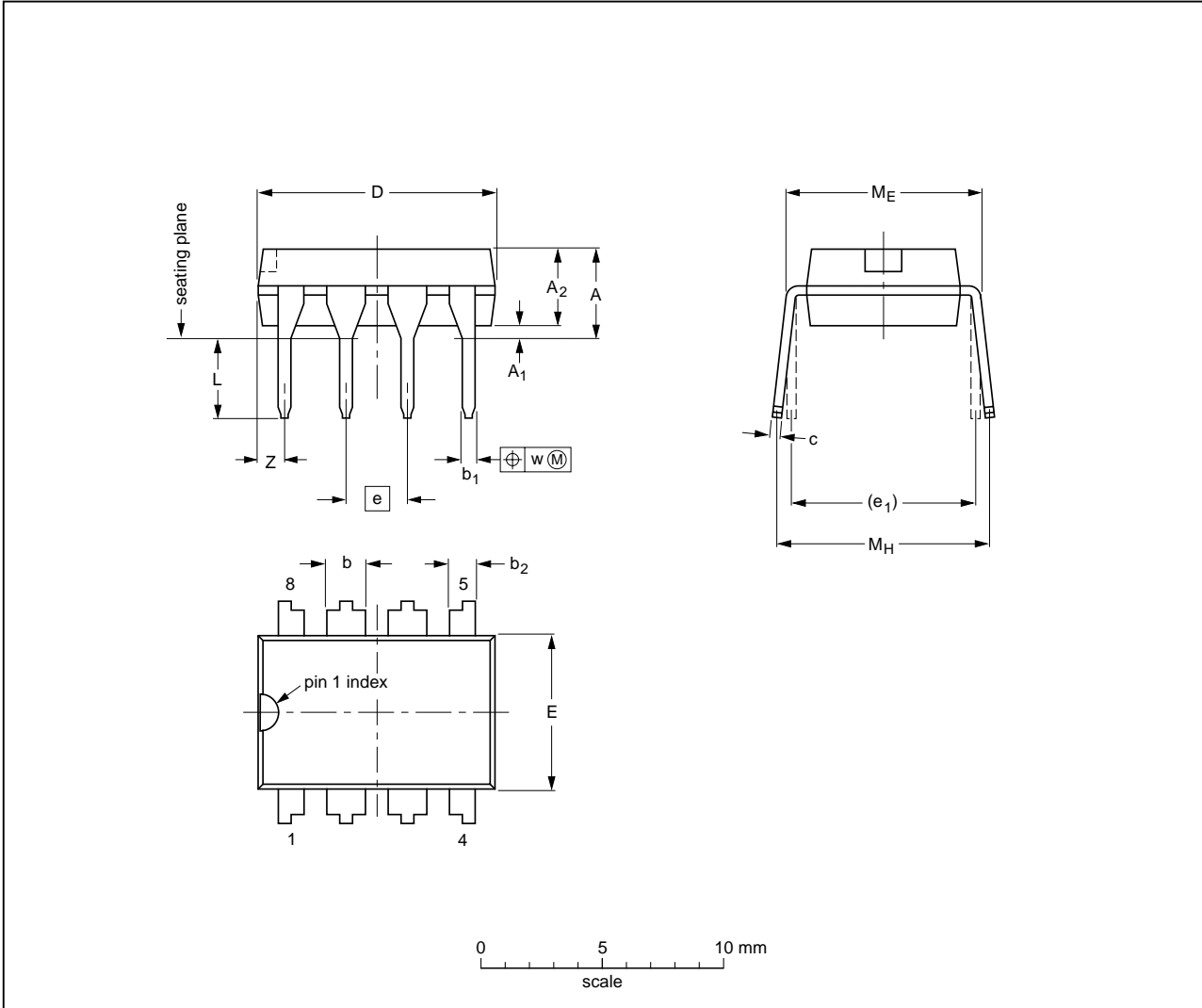
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## PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			99-12-27 03-02-13



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### SOLDERING

#### Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

#### Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
CPGA, HCPGA	–	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable <sup>(1)</sup>
PMFP <sup>(2)</sup>	–	not suitable

#### Notes

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- For PMFP packages hot bar soldering or manual soldering is suitable.

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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