NCP5080

Xenon Photoflash Capacitor Charge with Photo Sense Interface

The NCP5080 product is a high voltage boost driver dedicated to the Xenon power flashes.

The built-in DC/DC converter is based on a flyback structure with an external transformer to adapt any range of high voltage demand. The external feedback network makes it possible to dynamically adjust of the output voltage.

Features

- 2.7 V to 5.5 V Input Voltage Range
- Xenon Function Fully Supported
- Built-in Short Circuit Protection
- Dedicated Photo Flash Trigger Pin
- Provides IGBT drive
- Embedded Photodiode Sense
- Adjustable Primary I_{peak} Current
- This is a Pb-Free Device

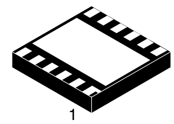
Typical Applications

- Digital Camera Photo Flash
- Digital Cellular Phone Camera Photo Flash
- Low Power Beacon

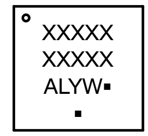
ON Semiconductor®

http://onsemi.com

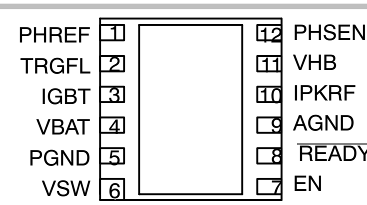
MARKING DIAGRAM



LLGA12
CASE 513AD



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)



ORDERING INFORMATION

Device	Package	Shipping†
NCP5080MUTXG	LLGA12 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

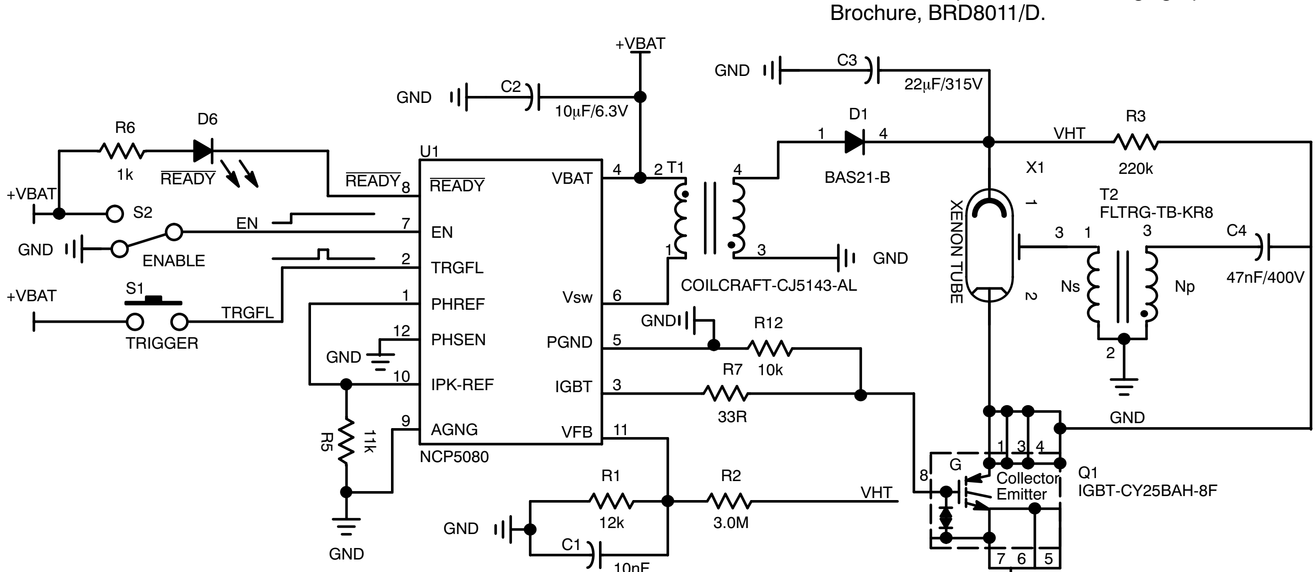


Figure 1. Typical NCP5080 Photo Flash Application

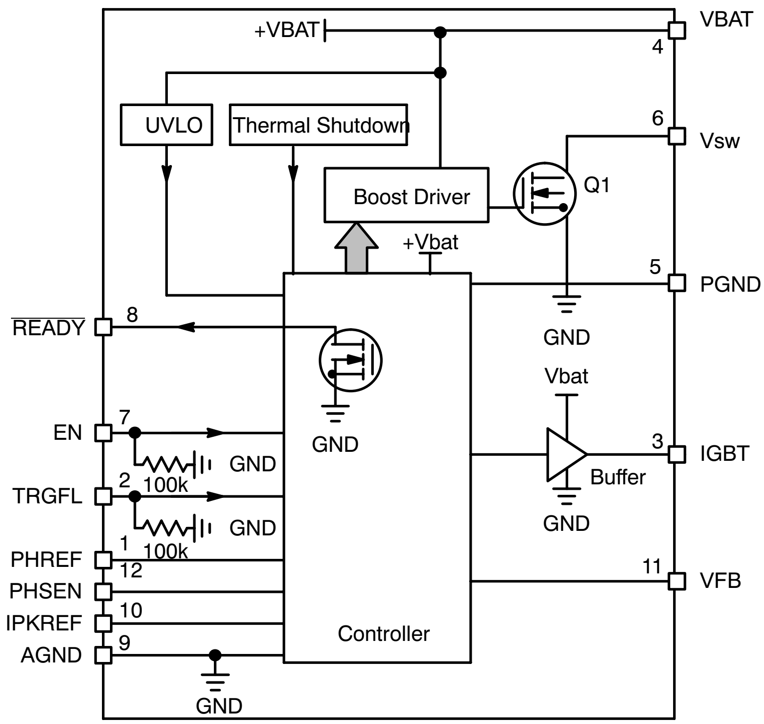


Figure 2. NCP5080 Simplified Block Diagram

PIN DESCRIPTIONS

PIN	Name	Type	Description
1	PHREF	INPUT, ANALOG	The external controller biases this pin with the reference voltage used, together with the PHSEN pin, to control the illumination of the photo scene. The V_{PH} voltage shall be in the 0.5 V to 1.5 V range, capable to support the internal resistor network (R load minimum is 500 kΩ). The photo sense function is deactivated when 0.5 V ≤ PHREF ≤ 1.5 V and PHSEN = GND (see Table 4).
2	TRGFL	INPUT, DIGITAL	A positive going pulse applied to this pin triggers the external IGBT and the flash sequence takes place. This command is active when EN = High, but is not synchronized with the output voltage value (see Table 4).
3	IGBT	OUTPUT, POWER	This pin provides the signal to drive the external IGBT and can be forced High or Low independently of the output voltage value, (assuming EN = High) according to the TRGFL pin status (see Table 4). Depending upon the type of IGBT used in the application, specific external gate network might be necessary to satisfy the IGBT gate drive conditions.
4	VBAT	INPUT, POWER	This pin carries the power supply to the analog, digital and DC/DC converter blocks and must be decoupled to ground by a 10 μF ceramic capacitor connected as close as possible to the package.
5	PGND	POWER	This pin is the GROUND return for the DC/DC converter and must be connected to the system ground, a ground plane is strongly recommended.
6	VSW	OUTPUT, POWER	This pin is the drain of the internal NMOS device and shall be connected to the primary of the external transformer. Care must be observed, at PCB layout level, to minimize the noise due to the large current and voltage transients present on that pin during normal operation.
7	EN	INPUT, DIGITAL	This pin controls the operation of the boost converter: EN = Low → The DC/DC converter is OFF, no flash can take place, the voltage across the external reservoir capacitor depends solely upon the leakage current present in the environment. EN = High → The DC/DC converter is activated, the voltage across the external reservoir capacitor is regulated at the predetermined value according to the V_{FB} reference. Similarly, a flash can take place, assuming the Xenon tube is properly biased.
8	$\overline{\text{READY}}$	OUTPUT, DIGITAL	This Open Drain Output goes LOW when the output voltage has reached the predetermined value across the external reservoir capacitor. The signal is HIGH when V_{out} is below the expected value, or if a fault has been detected at chip level.
9	AGND	POWER	This pin returns the Analog and Digital blocks ground and must be connected to the external ground plane.
10	IPKREF	INPUT, ANALOG	This pin provides the setup of the peak current flowing into the primary of the external transformer. The main purpose of this reference is to adjust the size of the transformer as a function of the flash power.
11	VFB	INPUT, ANALOG	This pin is the voltage feedback used to regulate the high voltage across the external reservoir capacitor. The impedance across V_{FB} and GND shall be kept to the lowest possible value to minimize the noise pickup.
12	PHSEN	INPUT, ANALOG	This pin provides a feedback from the illumination during the photo flash and, associated to the PHREF signal, controls the duration of the photo flash. The photodiode, connected across PHSEN and VBAT, shall be adjusted according to the Xenon flash in use. On the other hand, an external pulldown resistor shall be connected between the PHSEN pin and the ground reference. Such a resistor shall be calculated to cope with the type of photodiode used in the illumination sense loop. The photo sense function is deactivated when PHSEN = GND and 0.5 V ≤ PHREF ≤ 1.5 V (see Table 4).

1. Using low ESR ceramic capacitor, X5R type, is mandatory to optimize the DC/DC operation and to reduce the EMI.

MAXIMUM RATINGS (Note 2)

Symbol	Rating	Value	Unit
V_{BAT}, V_{CC}	Power Supply	$-0.3 < V_{BAT} < 7.0$	V
V_{SW}	Output Power Supply	40.0	V
EN, PFLASH	Digital Input Voltage Digital Input Current	$-0.3 < V < V_{BAT}$ 1	V mA
ESD	Human Body Model: R=1500 Ω, C=100 pF (Note 3) Machine Model	2 200	kV V
P_D R_{THja} R_{THJC}	LLGA12 package Power Dissipation @ T_A = +85°C (Note 4) Thermal Resistance Junction-to-Air Thermal Resistance Junction-to-Case	400 100 12	mW °C/W °C/W
T_A	Operating Ambient Temperature Range	-40 to +85	°C
T_J	Operating Junction Temperature Range	-40 to +125	°C
T_{Jmax}	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature Range	-65 to + 150	°C
	Latchup Current Maximum Rating per JEDEC Standard: JESD78	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum electrical ratings define the values beyond which permanent damage(s) may occur internally to the chip whatever be the operating temperature
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115
4. The maximum package power dissipation limit must not be exceeded.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

POWER SUPPLY SECTION (Typical values are referenced to T_A =+25°C, minimum and maximum values are referenced -40°C to +85°C ambient temperature, unless otherwise noted, and operating conditions are 2.85 V < V_{BAT} < 5.5 V, unless otherwise noted)

Pin	Symbol	Rating	Min	Typ	Max	Unit
4	V_{BAT}	DC/DC Converter Power Supply	2.7		5.5	V
4	U_{VLO}	Input Voltage Undervoltage Monitoring	2.1		2.6	V
6	I_{pk}	Primary Transformer Peak Current (750 mA Final Test Correlation) R_{ipk} = 11 kΩ			1.5	A
6	I_{dss}	Internal Power Switch NMOS Leakage Current @ V_{dss} = 40 V			0.5	μA
	t_{start}	DC/DC Start Time (C_{out} = 100 μF, No Load) V_{BAT} = 4 V, from EN Positive Pulse to V_{out} = 300 V (Note 6)		2	3	s
4	I_{stdb}	Standby Current, V_{BAT} = 5.5 V, I_{out} = 0 mA, EN = Low V_{BAT} = 3.6 V, I_{out} = 0 mA, EN = Low			1 0.75	μA
4	I_{op}	Operating Current, @V_{out} = Nominal, V_{BAT} = 3.6 V, EN = High		0.5		mA
3	R_{drv}	External IGBT Drive @ V_{BAT} = 3.6V V_{gs} = High (Note 8) V_{gs} = Low		23 33	37 52	Ω
	T_{onmx}	Maximum Inductor Charge Current ON Time		60		μs
	T_{offmx}	Maximum Inductor Discharge Current OFF Time		60		μs
	T_{LEB}	Leading Blanking (Note 7)		260		ns
6	$R_{DS(on)}$	Internal Power Switch NMOS $R_{DS(on)}$ @ V_{BAT} = 4.2 V		250	600	mΩ

6. Since this parameter is highly depending upon the application, it is not tested, guaranteed by design.
7. The blanking parameter is internal and cannot be tested in production, guaranteed by design.
8. Since the IGBT gate drive is derived from the V_{BAT} supply, special care must be taken to ensure that the IGBT triggers when V_{gs} is high and V_{BAT} is below 3.0 V.

ANALOG SECTION (Typical values are referenced to T_A = +25°C, minimum and maximum values are referenced -40°C to +85°C ambient temperature, unless otherwise noted, operating conditions 2.85 V < V_{BAT} < 5.5 V, unless otherwise noted)

Pin	Symbol	Rating	Min	Typ	Max	Unit
10	I_{REF}	Reference current @ V_{REF} = 1.14 V (Notes 9 and 10)	10		100	μA
10	V_{REF}	Reference Voltage (Note 10)	-3%	1.14	+3%	V
10	I_{PKR}	Reference Current (I_{REF}) Current Ratio	12000	13700	15400	
6	F_{PWM}	Internal DC/DC Flyback Frequency @ V_{BAT} = 4.2 V, I_p = 1 A, Lp = 6 μH, L_f = 200 nH, Transformer = TDK (Note 11)	15		600	kHz
11	V_{FB}	Output Voltage Feed Back reference	1.10	1.15	1.20	V
1	V_{PH}	Photo Sense Voltage Reference	0.5		1.5	V
1	V_{PHR}	Photo Reference Internal Resistance (Pin 1 to GND)		625		kΩ
	P_{FB}	Photo Feedback Tolerance		±3		%

9. I_{REF} current specifies the reference current range one can absorb from the I_{REF} pin
10. The external circuit must not force the I_{REF} pin voltage either higher or lower than the 1.14 V specified.
11. This parameter depends solely upon the output transformer and load characteristic and cannot be tested.
12. The overall photo sense tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.

DIGITAL PARAMETERS SECTION (Typical values are referenced to T_A = +25°C, minimum and maximum values are referenced -40 °C to +85°C ambient temperature, unless otherwise noted, operating conditions 2.85 V < V_{BAT} < 5.5 V, unless otherwise noted)

Pin	Symbol	Rating	Min	Typ	Max	Unit
2, 7	V_{IH}	EN, TRGFL Input Digital Signal	1.2		V_{BAT}	V
2, 7	V_{IL}	EN, TRGFL Input Digital Signal	0		0.4	V
8	V_{OL}	Ready Output Digital @ I_{rdy} = 1 mA			0.3	V
2	T_{pwfl}	TRGFL Input Flash Signal Pulse Width	10			μs
2, 7	R_p	EN, TRGFL Input Pulldown Resistor	50	100	200	kΩ

NOTE: Digital inputs undershoot ≤ 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{BAT}.

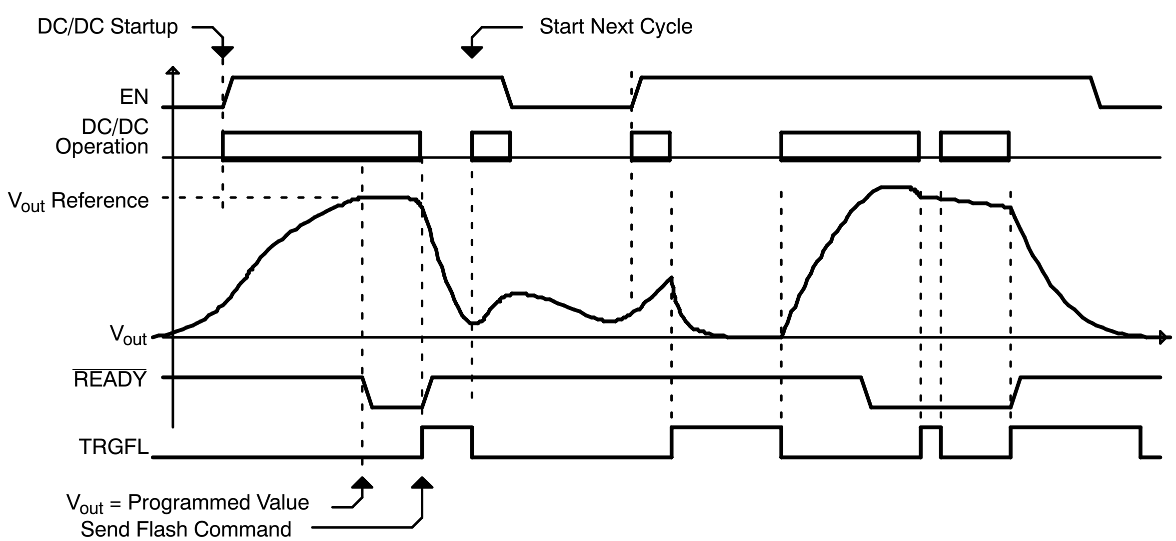


Figure 3. Basic Operation Timings

DC/DC Operation

The converter is based on a flyback topology, associated to an external transformer dedicated to the high voltage application. The Primary/Secondary turns ratio is defined to limit the peak voltage, at the NCP5080 pin V_{SW} level, to the operating voltage sustained by the internal NMOS device. With a 1:10 ratio, the peak voltage is limited to 30 V to supply a regulated 300 V across the external reservoir capacitor.

Note that although an OVP circuit is built-in the NCP5080 chip, it is strongly recommended to avoid operation without an external reservoir capacitor, a 1 μF / 315 V being the minimum value.

When the NMOS is ON, the current increases into the primary of the transformer until either the I_{peak} limit has been reached, or the time out is finished: at this point, the NMOS is switched OFF and the energy stored into the primary is dumped to the secondary, providing the current to recharge the reservoir capacitor. The OFF period is monitored by sensing the primary voltage and the system will re-start a new cycle when either $V_p = 0$ V or the time out is finished. The external resistor divider, connected across V_{out} and Ground, senses the output voltage to close the feedback loop at FBD pin. The output voltage is based on the 1.2 V reference and the R1/R2 ratio: $V_{out} = V_{REF} * ((R1 + R2) / R2)$.

The output voltage is regulated when the EN = H, but drops to zero when EN = L. In this case, the discharge time of the external reservoir depends solely upon the value of the passive component and the leakage currents that might exist at system level.

The DC/DC converter is switched OFF when either EN = Low, or TRGFL = High, or when the output voltage has reached the programmed value (see Figure 3).

Inductor Peak Current

In order to provide more flexibility to the NCP5080 driver, an extra pin, IPKREF, is provided to set up the peak current flowing into the primary inductor of the transformer. The I_{REF} is given by the 1.14 V voltage reference and the value of the external resistor:

$$I_{REF} = 1.14\,V / \,RIPK \qquad \text{(eq. 1)}$$

The primary peak current is given by Equation 1:

$$I_{peak} = I_{REF} * 14000 \qquad \text{(eq. 2)}$$

The maximum I_{peak} current shall be limited to 1.5 A maximum, assuming the transformer is sized to sustain such amount of electromagnetic energy. The efficiency of the DC/DC converter, and the recharge cycle time as well, depends upon the ESR and leakage inductance of the power transformer: a poor transformer will generate large oscillations during the operation which will be difficult to filter out at PCB level.

Table 1. PREFERRED POWER TRANSFORMER MANUFACTURERS

Manufacturer	Model	Comments
TDK	LDT565620ST-20 3	I_{peak} = 750 mA Max
Coilcraft	CJ5143-AL	I_{peak} = 1200 mA Max

Table 2. PREFERRED HIGH VOLTAGE TRIGGER FUNCTION

Component	Manufacturer	Model	Comments
High Voltage Trigger	PCA	EPC3215G-X	V_{out} = 4000 V
High Voltage Ceramic Capacitor	TDK	C3225X7R2J473M	Reference design+
22 μF/330 V to 120 μF/330 V	RUBYCON	FW series	Preferred

Table 3. PREFERRED XENON LAMP

Component	Manufacturer	Model	Comments
Flash Lamp-Reflector Assembly	Perkin-Elmer	RF-ASYRF160709 PKI08 (H)	E_j = 1.5 Joule C_{out} = 33 μF
Flash Lamp-Reflector Assembly	Perkin-Elmer	RF-ASY RF160709 PKI07 (H)	E_j = 2.1 Joule C_{out} = 47 μF
Flash Lamp-Reflector Assembly	Nam Kwong Co. LTD.	FET-O-D03150220E-02	9.8 Joule, C_{out} = 180 μF
Flash Lamp-Reflector Assembly	Nam Kwong Co. LTD.	FET-O-D02230202A-07	8.0 Joule, C_{out} = 150 μF

Perkin Elmer
coordinates: kimguan.lim@perkinelmer.com

Flash Strobe

The flash is activated by the digital status present at the TRGFL Pin and the logic condition of the EN and PHSEN Pins as defined in Table 4.

Table 4. FLASH OPERATING TRUE TABLE

EN	TRGFL	PHREF	PHSEN	Status
0	X	X	X	System Disabled: The boost and the flash are de-activated. Any on going flash is immediately switched OFF.
1	0	0.5 V to 1.5 V	GND	System Active: The output reservoir is being charged and the output voltage regulated. The photo sense is deactivated. The IGBT gate drive is LOW.
1	1	0.5 V to 1.5 V	GND	System Active: The output reservoir is being charged and the output voltage regulated. The photo sense is deactivated. The IGBT gate drive is HIGH whatever be the V_{out} voltage value . The xenon tube is fired if $V_{out} = V_{xen}$ minimum and the flash light keeps going until either TRGFL = 0, or the reservoir capacitor is fully discharged.
1	0	VREF	PHOTODIODE	System Active: The output reservoir is being charged and the output voltage regulated. The photo sense is activated . The IGBT gate drive is LOW.
1	1	VREF	PHOTODIODE	System Active: The output reservoir is being charged and the output voltage regulated. The photo sense is deactivated and the flash is switched OFF if the voltage present at the PHSEN Pin is higher the reference voltage applied to the PHREF Pin. The IGBT gate drive is HIGH whatever be the V_{out} voltage value . The Xenon tube is fired if $V_{out} = V_{xen}$ minimum and the IGBT keeps going until either TRGFL = 0, or the PHSEN > PHREF, or the reservoir capacitor is fully discharged.

The TRGFL signal provides a simple way to generate multiple consecutive flashes (similar to the stroboscope effect) to minimize the red eye effect, or to freeze multiple pictures of moving objects. The IGBT must be capable to turn ON with limited Gate voltage.

Photodiode Sensor

The photodiode sensor provides a feedback from the illumination generated by the xenon flash to avoid the overexposed picture. The PHREF pin shall be biased according to the model of xenon tube (in particular, the energy level) and optical lens aperture.

The function can be deactivated when not used in the application shown in Table 5. More over, connecting the PHREF Pin to the IPKREF Pin provides an easy way to fully disconnect the photo sense function.

The external photo sense element shall be connected across PHSEN and V_{BAT} to source the current as the illumination increases, with a pull-down resistor connected to the ground reference as depicted in Figure 4. The sense resistor is calculated to get the collector current when the photo diode is saturated. With a typical 10 µA to 30 µA of photodiode current, the resistor will be 100 kΩ to cope with the low input battery supply voltage situation.

Table 5. NCP5080 PHOTO SENSE TRUE TABLE

Pin	Operation	Operation
0.5 V ≤ PHREF ≥ 1.5 V PHSEN = GND	Photodiode Sense Deactivated	The IGBT is solely controlled by the TRGFL Pin
PHREF = VPH PHSEN = Photodiode	Photodiode Sense Activated	The IGBT is controlled by the [TRGFL AND PHSEN] status.

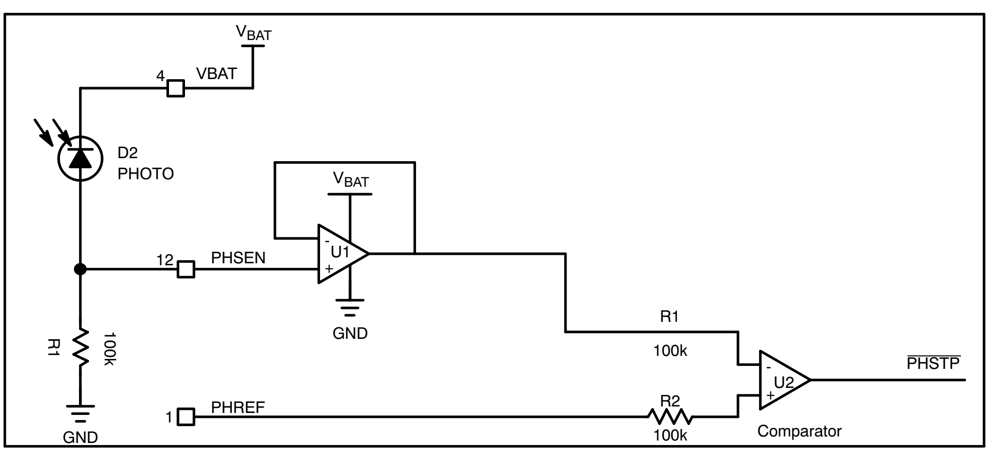


Figure 4. Basic Photo Sense Input Circuit

Although it is possible to increase the photo feedback sensitivity by increasing the value of the pulldown resistor, care must be observed since such a resistor is in parallel with the internal network as depicted in Figure 4 and the input node might be too sensitive to the ambient noise. It is recommended to avoid sense resistor value above 100 kΩ, although that 1 MΩ is possible, the operation being rapidly downgraded when the resistance increases beyond this value.

The PHREF voltage is setup by the external controller, in the 0.5 V to 1.5 V range, depending upon the need of the application. The internal structure includes a 500 kΩ (typical) resistor network, connected between PHREF pin and GND : the external reference source must support such a load and a 10 kΩ output impedance, or lower, is recommended to avoid uncontrolled operation. Finally, the IGBT signal will be switched OFF when the PHSEN signal reaches the PHREF reference.

The function is deactivated by forcing a voltage in the 0.5 V to 1.5 V range at the PHREF pin, associated with a GND connection to the PHSEN pin.

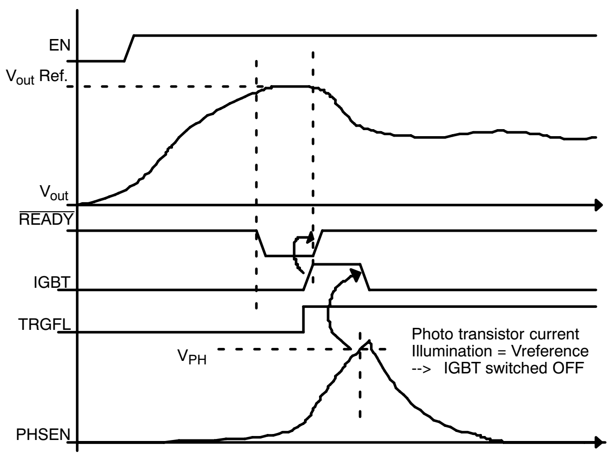


Figure 5. Typical Photo Sense Timings

When the photo sense is active and the photo sense threshold has been crossed, the photo sense feedback is internally latched and recycling the TRGFL signal (H to L) is necessary to reset the latch and start a new sequence .

Simplified Flash

The circuitry can be simplified when the application does not need the multiple flashes during the same photo sequence. In this case, the IGBT can be removed as there is no more need to dynamically switch off the xenon tube . Similarly, the photo sense becomes useless since there will be no way to control the illumination once the xenon flash has been triggered. Such a feature must be properly deactivated to avoid uncontrolled operation during a photo sequence: a simple resistor network fulfill such a requirement as depicted in Figure 6.

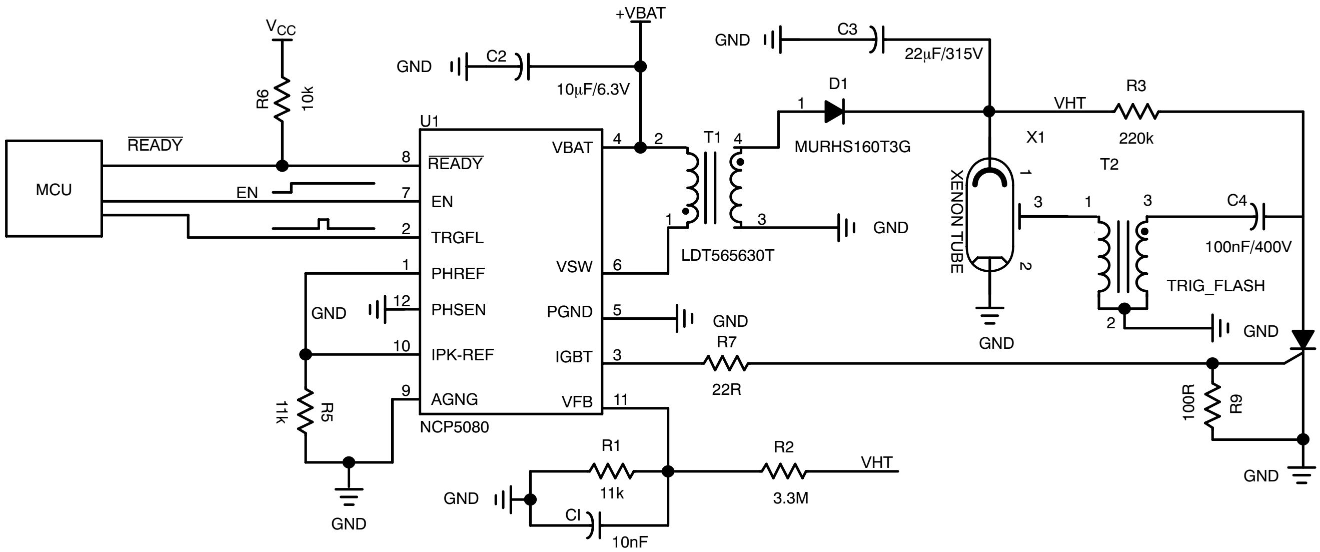


Figure 6. Simplified Xenon Flash Controller

On the other hand, since it is not possible to connect the high voltage trigger pin to the controller (MCU or other digital device), the IGBT pin will be used to trig the SCR device necessary to fire the high voltage pulse as depicted in Figure 6.

DEMO BOARD

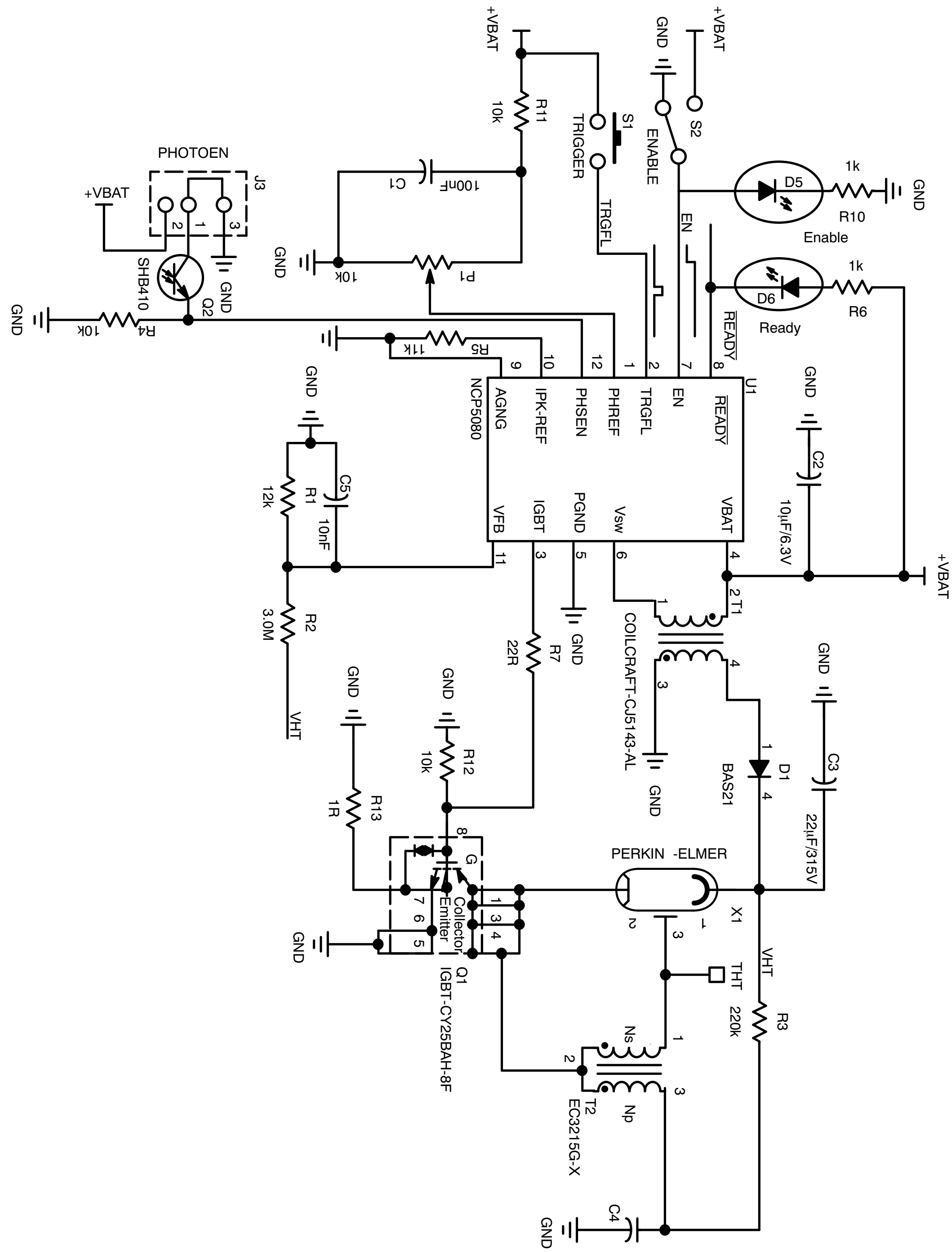


Figure 7. Demo Board Schematic Diagram

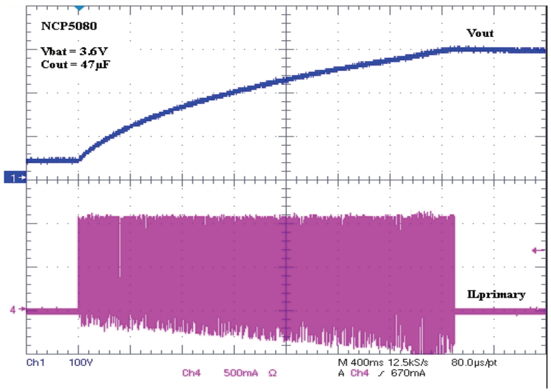


Figure 8. Output Capacitor Recharge Cycle

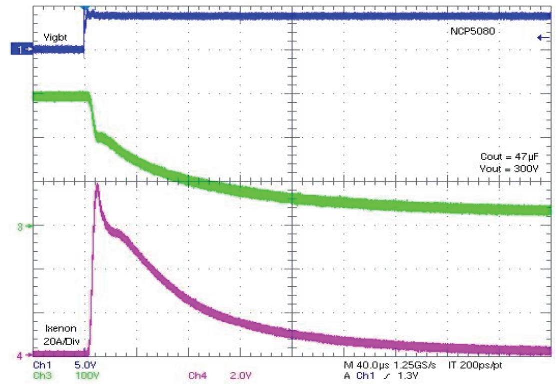


Figure 9. Xenon Tube Discharge Current

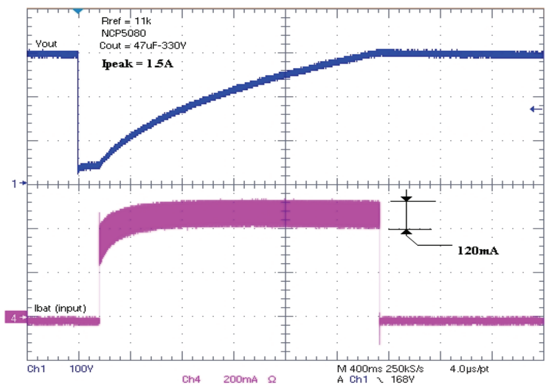


Figure 10. Recycling V_{OUT} Slope and Battery Input Current with I_{peak} = 1.5 A

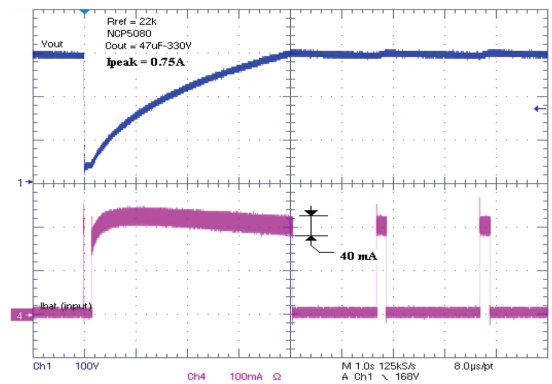
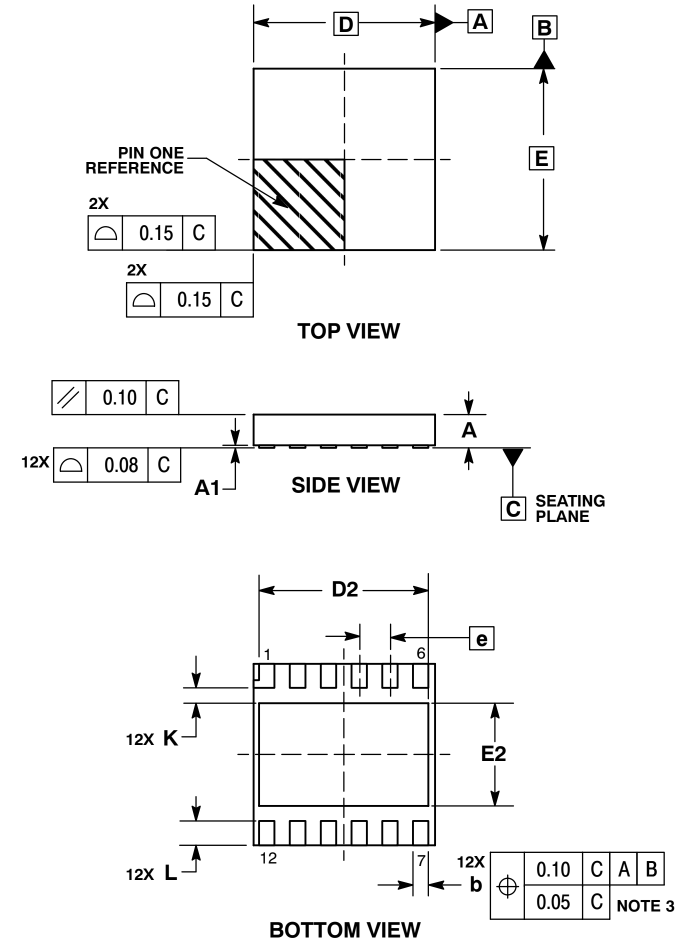


Figure 11. Recycling V_{OUT} Slope and Battery Input Current with I_{peak} = 750 mA

TRGFL: Trigger Flash pulse
PHREF: photo sense reference voltage (provided by the external circuit)
PHSEN: photo sense input voltage (provided by the photo transistor sensor)

PACKAGE DIMENSIONS

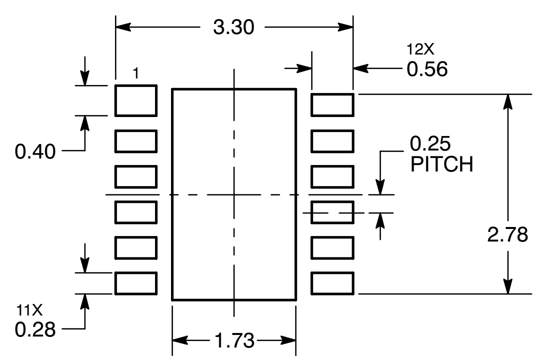
LLGA12
CASE 513AD-01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	2.75	2.85
E	3.00 BSC	
E2	1.65	1.75
e	0.50 BSC	
K	0.20	---
L	0.35	0.45

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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