

- Structure Silicon Monolithic Integrated Circuit
- Product Switched Capacitor Voltage Converter for Cellular
- Type **BH6040FVM**
- Function • Switched Capacitor Voltage Converter (Output Voltage: 5.0V)
 • A countermeasure on the VIN side (input side) noise is easy.
 • Internal SW for SHUTDOWN (This Converter ON/OFF Control)
 • Super-miniature MSOP-8 Package

○Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Range	Unit	Condition
Maximum Supply Voltage	VMAX	6.5	V	
Power Dissipation(*1)	Pd	350 (* 1)	mW	
Operating Temperature range	Topr	-30 ~ +75	°C	
Storage Temperature Range	Tstg	-55 ~ +125	°C	

(*1) This is the allowable loss of a single package.
 Reduce to 3.5 mW/°C when Ta = 25°C or above.

○Recommend Movement Range (Ta = -30~+75°C)

Parameter	Symbol	Range	Unit	Condition
Power Supply Voltage	VIN	3.0~4.5	V	

This product is not especially designed to be protected from radioactivity.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Use-related Cautions

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toy).

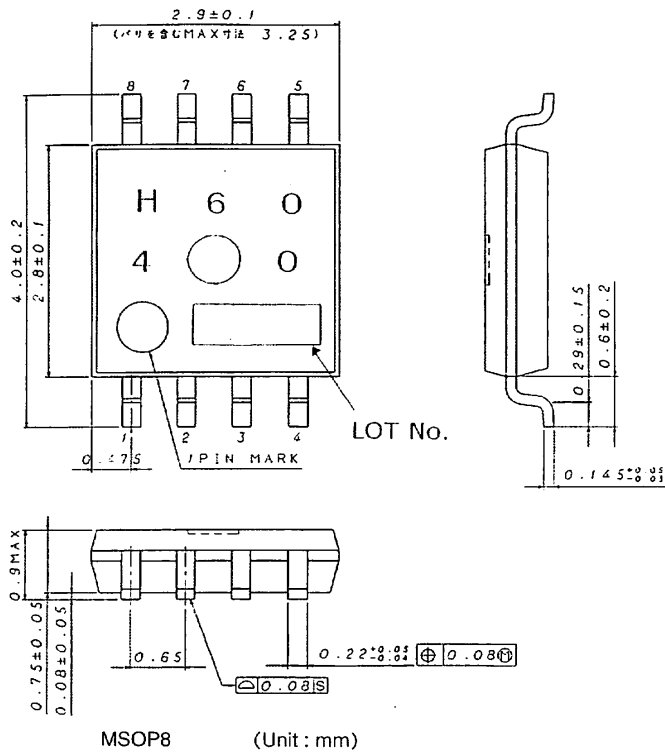
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○Electrical Characteristics

Unless otherwise specified, Ta=+25°C, VIN=3.6V

Parameter	Symbol	Spec			Unit	Condition
		MIN	TYP	MAX		
Circuit Current						
Circuit Current 1	IQ1	-	0	1	uA	Stand-by Mode
Circuit Current 2	IQ2	-	3.0	4.5	mA	Voltage Converter : Active no load (SHUTDOWN:H)
Voltage Converter						
Output Voltage	VOUT	4.85	5.00	5.15	V	3.2 ≤ VIN ≤ 4.5V, IO=60mA
Input Stability	VOVI	-	-	0.45	V	VIN=3.0~3.6V, IO=60mA VOVI=VO(VIN=3.6V)-VO(VIN=3.0V)
Load Regulation	ΔVO	-	50	100	mV	IO=1~60mA
Output Ripple level	VOAC	-	100	-	mVp-p	IO=1~60mA
Oscillation Frequency	fOSC	470	650	850	kHz	
Maximum Output Current	IOMAX	80	-	-	mA	3.2 ≤ VIN, VO ≥ 4.5V
Output Voltage Temperature coefficient	TCVO	-	100	-	ppm/°C	IO=60mA
SHUTDOWN SW						
Input 'H' level	VIH	1.3	-	VIN+0.3	V	Voltage Converter : Active
Input 'L' level	VIL	-0.3	-	0.5	V	Voltage Converter : Stationary
'H' level Inflow Current	IINH	0.5	1.8	5	uA	VSW=1.8V
'L' level Inflow Current	IINL	-	0	3	uA	

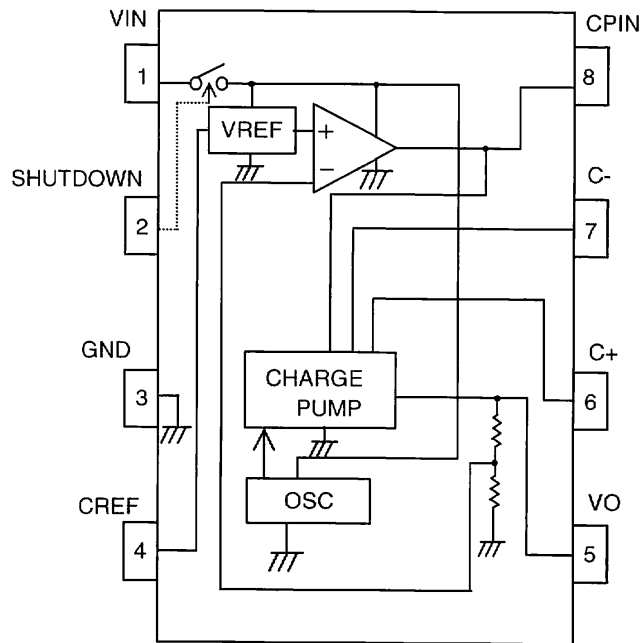
○Package Diagram



○Terminal table

PIN	BALL Name
1	LEDSEL
2	CC1
3	CC2
4	TEST
5	LED1
6	LED2
7	LED3
8	LED4
9	LED5
10	LED6
11	AGND
12	IREF
13	VBAT
14	CGND
15	C1M
16	CPIN
17	C2P
18	C2M
19	C1P
20	CPOUT

○Block Diagram



○Use-related Cautions

(1) Absolute maximum ratings

If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range

This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector

There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines

In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(4) GND voltage

Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation

When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields

Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board

When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins

Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern

When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors

When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

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U.S.A / San Diego	TEL : +1(858)625-3630	FAX : +1(858)625-3670
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Dallas	TEL : +1(972)312-8818	FAX : +1(972)312-0330
Germany / Dusseldorf	TEL : +49(2154)9210	FAX : +49(2154)921400
United Kingdom / London	TEL : +44(1)908-282-666	FAX : +44(1)908-282-528
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Shanghai	TEL : +86(21)6279-2727	FAX : +86(21)6247-2066
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Beijing	TEL : +86(10)8525-2483	FAX : +86(10)8525-2489
Taiwan / Taipei	TEL : +866(2)2500-6956	FAX : +866(2)2503-2869
Korea / Seoul	TEL : +82(2)8182-700	FAX : +82(2)8182-715
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Japan /
(Internal Sales)

Tokyo	2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082	TEL : +81(3)5203-0321	FAX : +81(3)5203-0300
Yokohama	2-4-8, Shin Yokohama, Kohoku-ku, Yokohama, Kanagawa 222-8575	TEL : +81(45)476-2131	FAX : +81(45)476-2128
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Yokohama		TEL : +81(45)476-9270	FAX : +81(045)476-9271