High Voltage PIN Diode Driver

Features

- Processed with HVCMOS® technology
- 5.0V CMOS logic - low power dissipation
- DMOS output voltage up to 220V
- Low power level shifting -2.5V to 220V
- Source current 1.7mA
- Output fault detection
- Latched data output

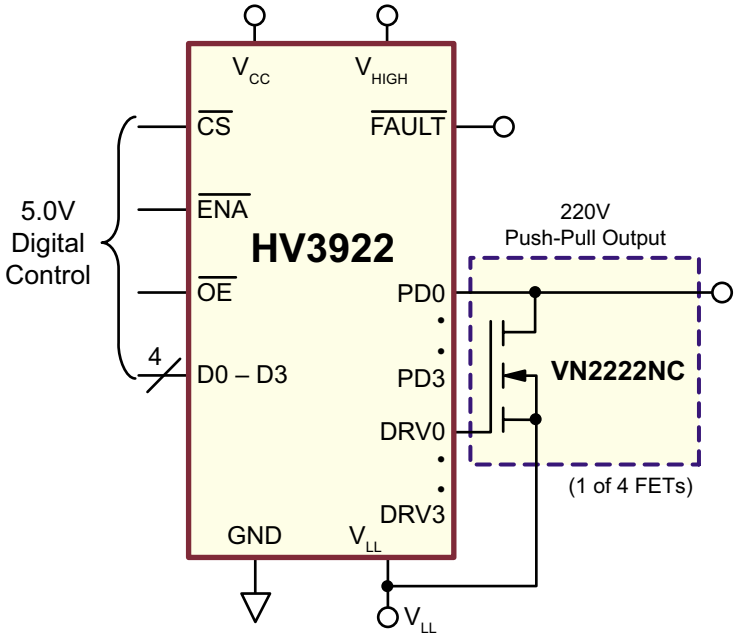
General Description

The HV3922 is a monolithic, high voltage quad-output driver that is designed to be used in conjunction with the Supertex VN2222NC, a separate N-channel DMOS FET quad array, whose device characterics are briefly described below. Together, these devices per-form a 220V push-pull function that is especially suited for driving PIN diodes in applications such as frequency-hopping radios, microwave communication systems and phased array radar.

Used as a microwave or RF switch, the HV3922 has 4 high voltage P-channel outputs: PD0, PD1, PD2 and PD3. Additional controls are Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) functions. The HV3922 also has an output fault detection function that protects the outputs from damage by putting them into a high impedance state when a short is detected. The HV3922 provides 4 low voltage outputs - DRV0, DRV1, DRV2 and DRV3 - that drive the gates of the 4 N-channel FETs.

The VN2222NC is an N-channel DMOS FET quad array recommended for use in conjunction with HV3922 outputs to form four 220V push-pull outputs. Each of the four devices has a max $R_{DS(ON)}$ of 1.25Ω, min $I_{D(ON)}$ of 5.0 amps, and BV_{DSS} of 220V.

Typical Application Circuit



Ordering Information

Device	Package Options		
	20-Lead Ceramic Side-Brazed *.950x.288in body,* *.200in height (max), .100in pitch*	28-JLead Quad Cerpac *.490x.490in body,* *.190in height (max.), .050in pitch*	28-JLead PLCC *.453x.453in body,* *.180in height (max.), .050in pitch*
HV3922	HV3922C	HV3922DJ	HV3922PJ-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{CC}	-0.5V to +7.0V
Logic input voltage	-0.3V to V_{CC} +0.3V
Supply voltage, V_{LL}	-5.0V
Supply voltage, V_{PP}	+230V
Maximum power dissipation	0.8W
Junction temperature	+150°C
Storage temperature range	-65°C to +150°C
Operating temperature range	-55°C to +125°C
Lead temperature*	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

** 1.6mm from case for 10 seconds.*

Recommended Operating Conditions

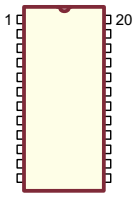
Sym	Parameter	Min	Max	Units
V_{CC}	Logic supply voltage	4.5	5.5	V
V_{IN}	DC logic input voltage	0	V_{CC}	V
V_{LL}	V_{LL} supply voltage	-3.5	-2.5	V
V_{PP}	V_{PP} supply voltage	200	220	V
$IP_{D(N)}H$	High-state continuous $P_{D(N)}$ source current	-	1.7	mA
T_A	Ambient operating temp	-55	+125	°C
CL	$D_{RV(N)}$ load capacitance	0	0.006	µF

Notes:

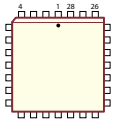
1. *V_{PP} rise time (dv/dt) should be less than 50V/µS.*
2. *Power-up sequence should be the following:*
   A) Connect ground;
   B) Apply V_{CC};
   C) Apply V_{LL};
   D) Apply V_{PP};
   E) Set all inputs to a known state.

Power-down sequence should be the reverse of the above.

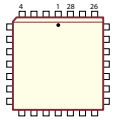
Pin Configurations



20-Lead Ceramic Side-Brazed (C)
(top view)



28-JLead Quad Cerpac (DJ)
(top view)



28-JLead PLCC (PJ)
(top view)

Product Markings

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

20-Lead Ceramic Side-Brazed (C)

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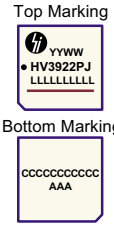
28-JLead Quad Cerpac (DJ)



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28-JLead PLCC (PJ)

Electrical Characteristics

DC Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter	Min	Max	Units	Conditions
I_{CCQ}	Maximum quiescent V_{CC} supply current	-	1.0	mA	V_{CC} = 5.5V all outputs open.
I_{LLQ}	Maximum quiescent V_{LL} supply current	-	4.0	mA	V_{LL} = -3.5V $D_{RV(N)}$ high or low.
I_{PPQ}	Maximum quiescent V_{PP} supply current	-	100	µA	V_{PP} = 220V $P_{D(N)}$ high or low.
I_{IH}	High-level logic current	-	10	µA	H = V_{CC}
I_{IL}	Low-level logic current	-	10	µA	L = 0V
V_{FH}	Minimum high-level logic output voltage (fault detect)	4.4	-	V	V_{CC} = 4.5V, I_{OH} = 20µA
V_{FL}	Maximum low-level logic output voltage (fault detect)	-	0.1	V	V_{CC} = 5.5V, I_{OH} = -20µA
V_{DH}	Minimum $P_{D(N)}$ high-level output voltage	198	-	V	V_{PP} = 203V, I_{OH} = 1.7mA
	Minimum $D_{RV(N)}$ high-level output voltage	4.0	-	V	V_{CC} = 4.5V, I_{OH} = 100µA
V_{DL}	Maximum $D_{RV(N)}$ low-output voltage	-	-2.3	V	V_{LL} = -2.5V, I_{DL} = -500µA
$V_{TH(min)}$	Minimum fault threshold for $P_{D(N)}$ output high	0.5 x V_{PP} fault	-	V	$P_{D(N)}$ = HIGH, $\overline{OE}$ = V_{CC}
$V_{TH(max)}$	Maximum fault threshold for $P_{D(N)}$ output high	0.85 x V_{PP} fault	-	V	$P_{D(N)}$ = HIGH, $\overline{OE}$ = V_{CC}
$V_{TL(min)}$	Minimum fault threshold for $P_{D(N)}$ output Hi-Z	$V_{(PDN)}$ = 0	-	V	$P_{D(N)}$ = Hi-Z, $\overline{OE}$ = V_{CC}
$V_{TL(mAX)}$	Maximum fault threshold for $P_{D(N)}$ output Hi-Z	-	$V_{(PDN)}$ = 25	V	$P_{D(N)}$ = Hi-Z, $\overline{OE}$ = V_{CC}

AC Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter	Min	Max	Units	Conditions
t_{WCS}	Minimum $\overline{CS}$ pulse to latch data	100	-	ns	V_{CC} = 4.5V, $\overline{ENA}$ = 0V
t_{WENA}	Minimum $\overline{ENA}$ pulse width to latch data	100	-	ns	V_{CC} = 4.5V, $\overline{CS}$ = 0V
t_{WOE}	$\overline{OE}$ pulse width	10	50	µs	V_{CC} = 4.5V, $\overline{OE}$ = 0V, V_{PP} = 220V, $P_{D(N)}$ LOAD = 20KΩ to GND
		16	50	µs	V_{PP} = 220V, $P_{D(N)}$ LOAD = 20KΩ and 3000pF to GND
TT	Input transition rise and fall time	0	200	ns	V_{CC} = 4.5V
T_{SU1}	Minimum set-up time D_N and $\overline{CS}$ to $\overline{ENA}$	150	-	ns	V_{CC} = 4.5V
T_{SU2}	Minimum set-up time $\overline{ENA}$ to $\overline{OE}$ falling edge	150	-	ns	V_{CC} = 4.5V
TH	Minimum hold time	5.0	-	ns	V_{CC} = 4.5V
CIN	Maximum input capacitance	-	10	pF	Not tested, reference only
TO	$P_{D(N)}$ transition time from $\overline{OE}$ low to $P_{D(N)}$ high/low	1.0	50	µs	V_{PP} = 220V, $P_{D(N)}$ output loaded by 20KΩ and 3000pF to GND

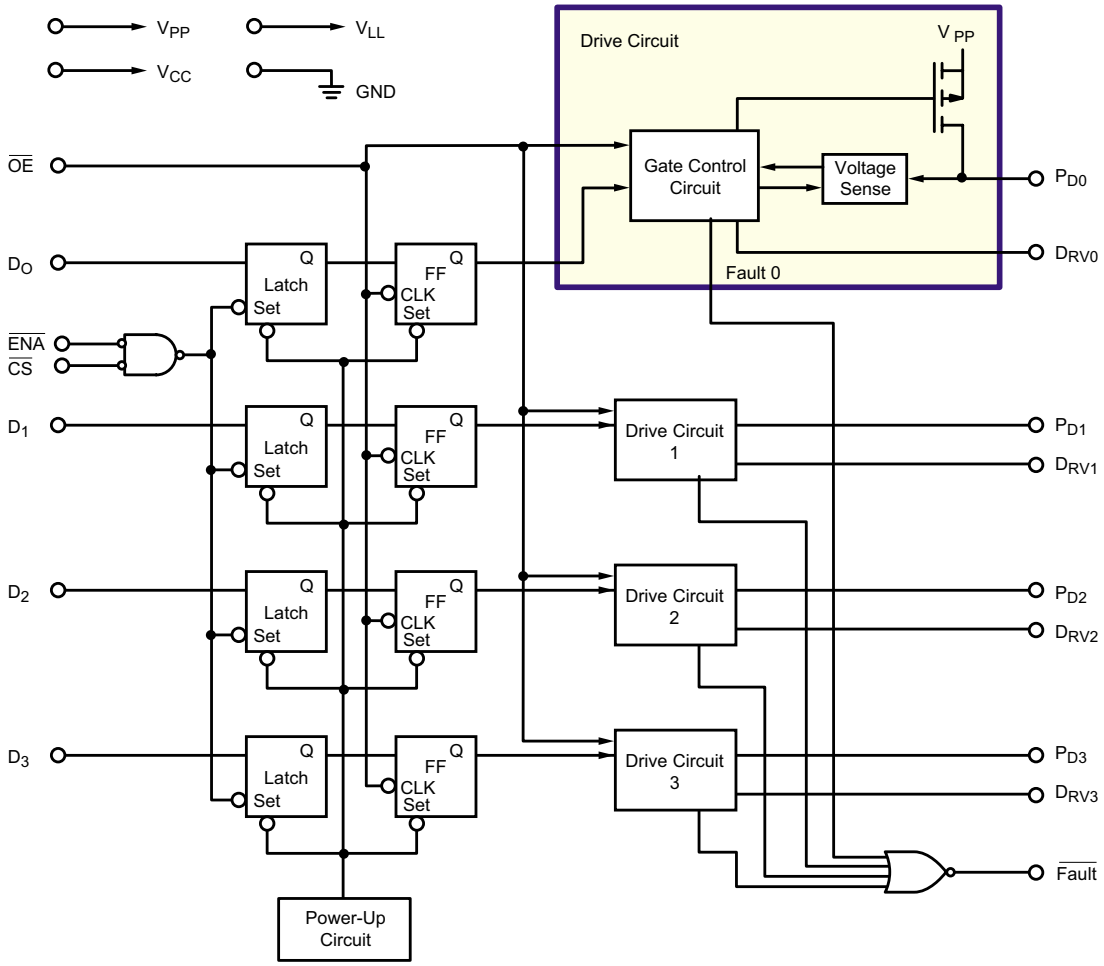
Function Table

Input					Output			
$\overline{CS}$	$\overline{ENA}$	$\overline{OE}$	Data $D_{(N)}$	V_{TH} Level[2]	Internal Latch Q(N)	$P_{D(N)}$	$D_{RV(N)}$	$\overline{Fault}$
H	X	H	X	Pass	Previous State	Previous State	Previous State	VFH
X	H	H	X	Pass	Previous State	Previous State	Previous State	VFH
L	L	H	H	Pass	Set	Previous State	Previous State	VFH
L	L	H	L	Pass	Reset	Previous State	Previous State	VFH
L	L	H > L	H	P/F	Set	VDH	VDL	VFH
L	L	H > L	L	P/F	Reset	Hi-Z	VDH	VFH
H	X	H > L	X	-	Previous State	-	-	-
-	-	-	-	P/F	Set	VDH	VDL	VFH
-	-	-	-	P/F	Reset	Hi-Z	VDH	VFH
X	H	H > L	X	-	Previous State	-	-	-
-	-	-	-	Pass	Set	VDH	VDL	VFH
-	-	-	-	Pass	Reset	Hi-Z	VDH	VFH
X	X	H	X	Fail	-	Hi-Z	VDL	VFL
(At Power Up)								
X	X	V_{IH}	X	P/F	Set	VDH	VDL	VFH

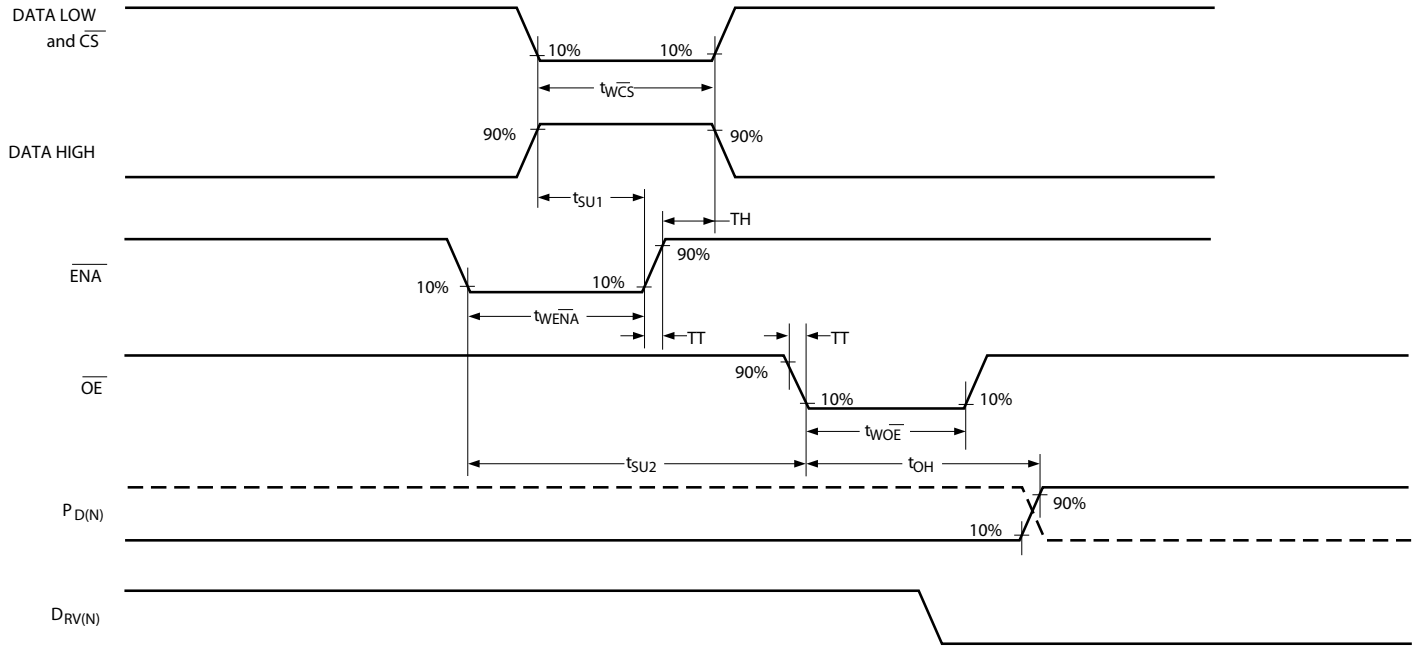
Notes:

1. *X indicates "Don't Care" input state (L or H).*
2. *The output threshold is internally tested for each $P_{D(N)}$ output; the pass condition occurs when $\overline{OE}$ = H and:*
   - *A) $P_{D(N)}$ driving high with output > $V_{TH(MAX)}$, or may occurs if $P_{D(N)}$ driving high and output > $V_{TH(MIN)}$ and < $V_{TL(MAX)}$.*
     OR
   - *B) $P_{D(N)}$ driving Low with output < $V_{TH(MIN)}$, or may occur if $P_{D(N)}$ driving low and output < $V_{TH(MAX)}$ and < $V_{TL(MIN)}$.*
3. *$\overline{FAULT}$ output = V_{FL} indicates a fault has been detected in at least one of the $P_{D(N)}$ output loads when $\overline{OE}$ = H. All other outputs shall function normally when a fault condition has been detected for one of the outputs. The $\overline{FAULT}$ output shall remain in the low state, regardless of the state of the output which initiated the fault status, until the next falling edge of $\overline{OE}$. Whenever $\overline{OE}$ = L, the $\overline{FAULT}$ output is forced to V_{FH}, and the fault latch is reset. If the fault condition persists, the fault response repeats each time the $\overline{OE}$ input is set to H.*
4. *H>L indicates falling edge (H to L).*
5. *HI-Z indicates no current is sourced to output $P_{D(N)}$.*
6. *P/F indicates "Pass" or "Fail" fault threshold conditions.*

Functional Block Diagram



Timing Diagram



Pin Description - 20-Lead Ceramic Side-Brazed (C)

Pin #	Function	Pin #	Function
1	D1	11	PD0
2	D2	12	DRV1
3	D3	13	DRV0
4	VLL	14	VPP
5	GND	15	VCC
6	DRV3	16	$\overline{\text{ENA}}$
7	DRV2	17	$\overline{\text{OE}}$
8	PD3	18	$\overline{\text{CS}}$
9	PD2	19	$\overline{\text{FAULT}}$
10	PD1	20	D0

Pin Description - 28-JLead Quad Cerpac (DJ)

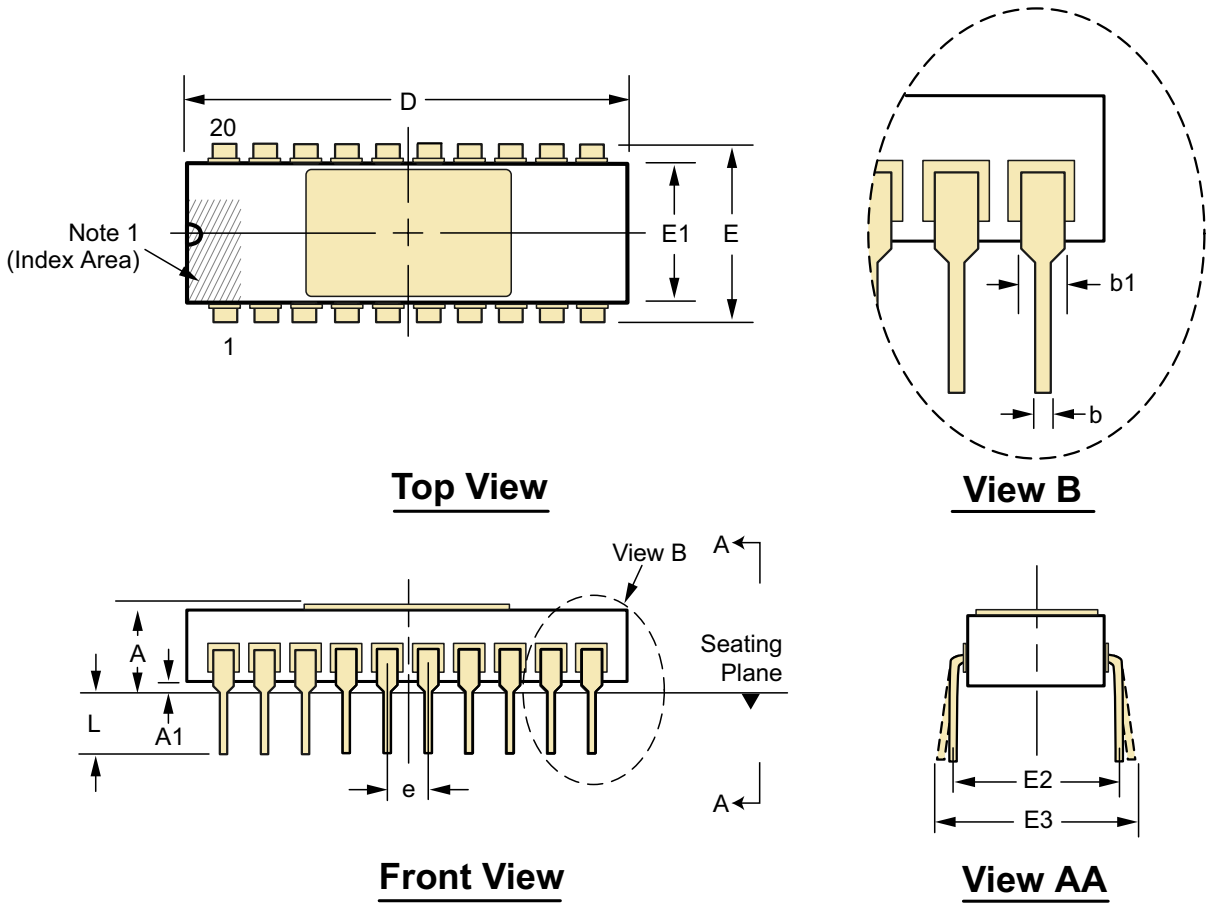
Pin #	Function	Pin #	Function
1	D1	15	PD1
2	D2	16	PD0
3	D3	17	NC
4	NC	18	DRV1
5	VLL	19	DRV0
6	GND	20	NC
7	NC	21	VPP
8	DRV3	22	NC
9	DRV2	23	VCC
10	NC	24	$\overline{\text{ENA}}$
11	PD3	25	$\overline{\text{OE}}$
12	NC	26	$\overline{\text{CS}}$
13	PD2	27	$\overline{\text{FAULT}}$
14	NC	28	D0

Pin Description - 28-JLead PLCC (PJ)

Pin #	Function	Pin #	Function
1	D1	15	PD1
2	D2	16	PD0
3	D3	17	NC
4	NC	18	DRV1
5	VLL	19	DRV0
6	GND	20	NC
7	NC	21	VPP
8	DRV3	22	NC
9	DRV2	23	VCC
10	NC	24	$\overline{\text{ENA}}$
11	PD3	25	$\overline{\text{OE}}$
12	NC	26	$\overline{\text{CS}}$
13	PD2	27	$\overline{\text{FAULT}}$
14	NC	28	D0

20-Lead Ceramic Side-Brazed Package Outline (C)

.980x.300in. body, .200in. height (max), .100in. pitch



Note 1:

A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	b	b1	D	E	E1	E2	E3	e	L
Dimension (inches)	MIN	.085	.025	.015	.045	.980	.300	.280	.300 REF	-	.100 BSC	.125
	NOM	-	-	-	-	-	-	-		-		-
	MAX	.200	.070	.022	.065	1.020	.325	.310		.400		.200

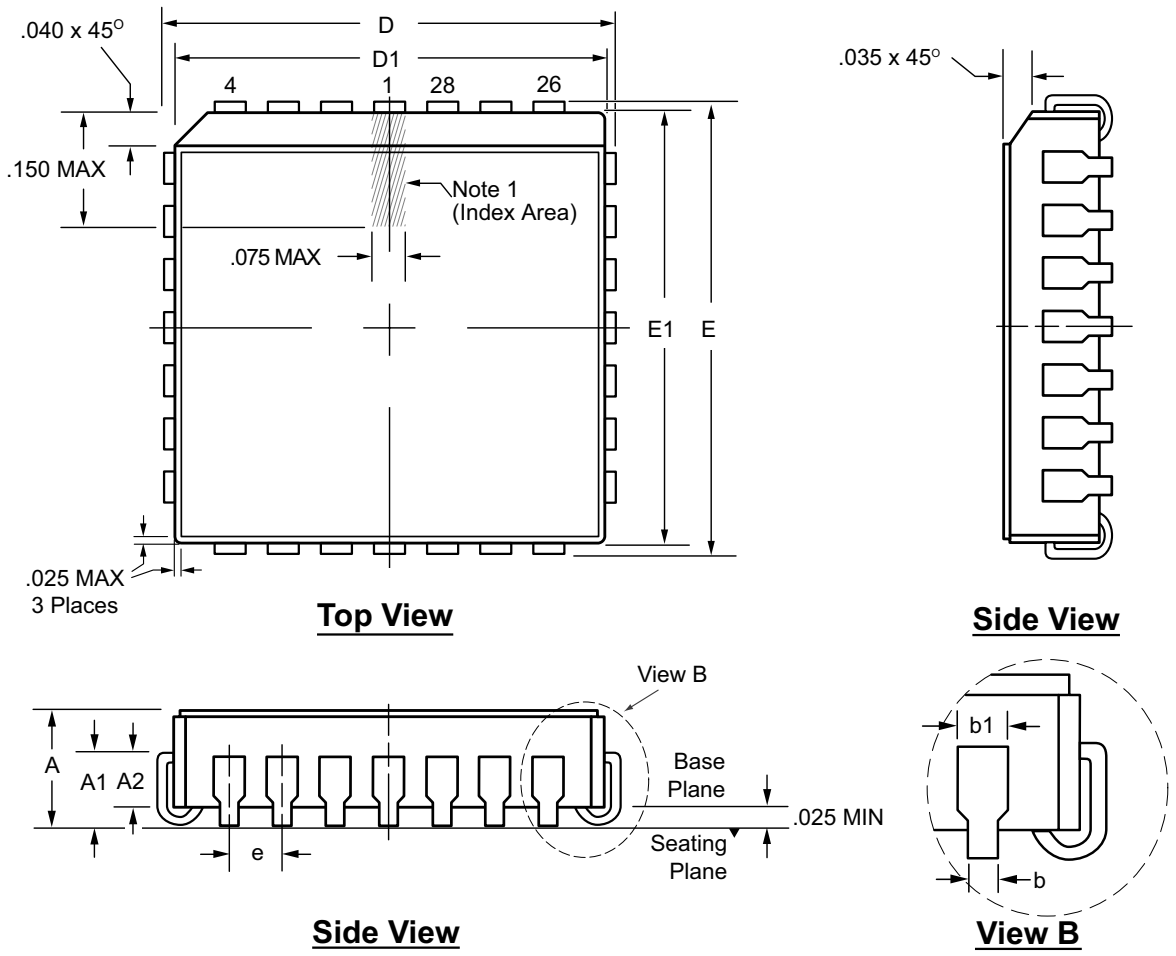
JEDEC Registration MS-015, Variation AE, Issue A, July, 1990.

Drawings not to scale.

Supertex Doc.#: *DSPD-20CDIPCNC, Version B070108.*

28-JLead Quad Cerpac Package Outline (DJ)

.490x.490in. body, .190in. height (max.), .050in. pitch



Note 1:

A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.155	.090	.060 REF	.017	.026	.485	.430	.485	.430	.050 BSC
	NOM	.172	.100		.019	.029	.490	.450	.490	.450	
	MAX	.190	.120		.021	.032	.495	.465	.495	.465	

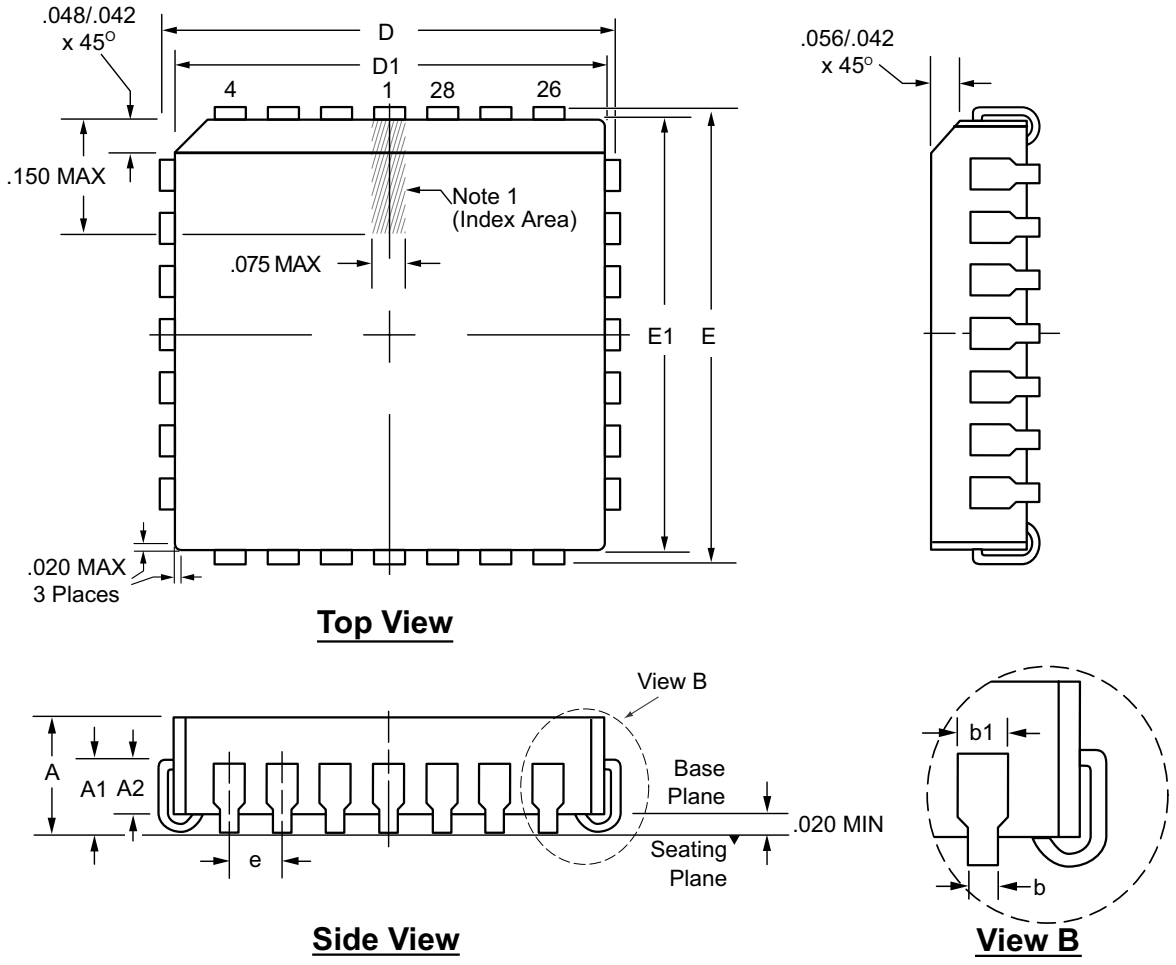
JEDEC Registration MO-087, Variation AA, Issue B, August, 1991.

Drawings not to scale.

Supertex Doc.#: *DSPD-28CERPACDJ, Version A063008.*

28-JLead PLCC Package Outline (PJ)

.453x.453in. body, .180in. height (max.), .050in. pitch



Note 1:

A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC
	NOM	.172	.105	-	-	-	.490	.453	.490	.453	
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456	

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.
Drawings not to scale.
Supertex Doc. #: *DSPD-28PLCCPJ, Version A063008.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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