64-Channel Gray-Shade Display Column Driver

Ordering Information

Device	Package Options*	
	Die in wafer form	Die in waffle pack
HV62106	HV62106XW	HV62106X

*Consult factory for availability of bumped die.

Features

- 5V CMOS inputs
- 64 outputs per device
- Up to 60V output voltage
- Capable of 4 output pulse widths
- PWM gray shade conversion
- Two 2-bit data buses
- 28 MHz data throughput rate
- Pin-programmable shift direction (DIR)
- Integrated high-voltage CMOS technology
- Optimized layout for COG use

General Description

Not recommended for new designs.

The HV62106 is a 64-channel column driver IC designed for gray shade flat panel displays. Using Supertex's unique HVCMOS® technology, it is capable of providing gray shading by pulse width modulation (PWM) conversion.

A high level on the chip select input enables the IC to load data into a set of input data latches. This input data, in two groups of two, are latched into the input data latches on both edges of the Shift Clock. The data stored in these input data latches is transferred to a set of output data latches on the rising edge of Load Count. After the input data registers are full, a chip select output signal is provided for enabling the next IC in the chain.

A master binary counter is reset with a high level on Load Count and is incremented on the rising edge of Count Clock. The data stored in the output data latches is compared to the contents of the master counter. The output of the comparator drives the high voltage output devices. The higher the binary number in the output data latches, the longer the pulse width will be on the corresponding output.

DIR is a shift-direction-select input which is provided to inter-change the direction of the latched data inputs. When the DIR input is high, CS2 becomes chip select input and data is latched into the data latches in the sequence of $HV_{OUT}1$ to $HV_{OUT}64$. When the DIR input is low, CS1 becomes chip select input and data is latched into the data latches in the sequence of $HV_{OUT}64$ to $HV_{OUT}1$. $D_{IN}1$ and $D_{IN}2$ load in data for odd number of outputs. $D_{IN}3$ and $D_{IN}4$ load in data for even number of outputs.

Absolute Maximum Ratings

Supply voltage, V_{DD}	-0.5V to +7.5V
Supply voltage, V_{PP}	-0.5V to +70V
Logic input levels	-0.5V to V_{DD} + 0.5V
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Note:
All voltages are referenced to GND.

Electrical Characteristics

(Over recommended conditions of V_{DD} = 5V, V_{PP} = 60V, T_A = 25°C unless otherwise noted)

Low Voltage DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		10	mA	f_{SC} = 7MHz, f_{CC} = 3MHz
I_{DDQ}	Quiescent V_{DD} supply current		1	mA	All V_{IN} = GND
I_{IH}	High-level input current		10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level input current		-10	µA	V_{IL} = GND
I_{OH}	High-level output current	-1		mA	
I_{OL}	Low-level output current	1		mA	

High Voltage DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{PPQ}	Quiescent V_{PP} supply current		100	µA	All HV_{OUT} low or high
V_{OH}	High-level output	50		V	I_{OUT} = -12mA
V_{OL}	Low-level output		8	V	I_{OUT} = 15mA

AC Characteristics (Logic Timing)

Symbol	Parameter	Min	Max	Units	Conditions
f_{SC}	Shift clock frequency		7	MHz	
f_{DIN}	Data In frequency		7	MHz	
f_{CC}	Count clock frequency		3	MHz	
t_{WA}	Chip select pulse width	80		ns	
t_{SS}	Chip select set-up time	20		ns	
t_{HS}	Chip select hold time	40		ns	
t_{DS}	Data to shift clock set-up time	-10	30	ns	
t_{DH}	Data to shift clock hold time	30		ns	
t_{WLC}	Load count pulse width	160		ns	
t_{DLCC}	Load count to count clock delay	70		ns	
t_{DSL}	Shift clock to load count delay	200		ns	
t_{CSC}	Shift clock cycle time	143		ns	
t_{DLC}	Load count to HV_{OUT} delay		1.5	µs	C_L = 15pF // R_L = 10MΩ
t_{WCC}	Count clock pulse width	160		ns	
t_{CCC}	Count clock cycle time	333		ns	
t_{DCC}	Count clock to HV_{OUT} delay		1.5	µs	C_L = 15pF // R_L = 10MΩ
t_{WSC}	Shift clock pulse width	70		ns	
t_{WD}	Data in pulse width	60		ns	

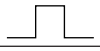
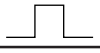
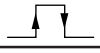
Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	Conditions
V_{PP}	High voltage supply	0	60	V	
V_{DD}	Logic supply voltage	4.5	5.5	V	
V_{IL}	Low-level input voltage	0	1	V	
V_{IH}	High-level input voltage	V_{DD}-1	V_{DD}	V	
f_{SC}	Shift clock frequency		7	MHz	
f_{CC}	Count clock frequency		3	MHz	
T_A	Operating temperature	-40	+85	°C	

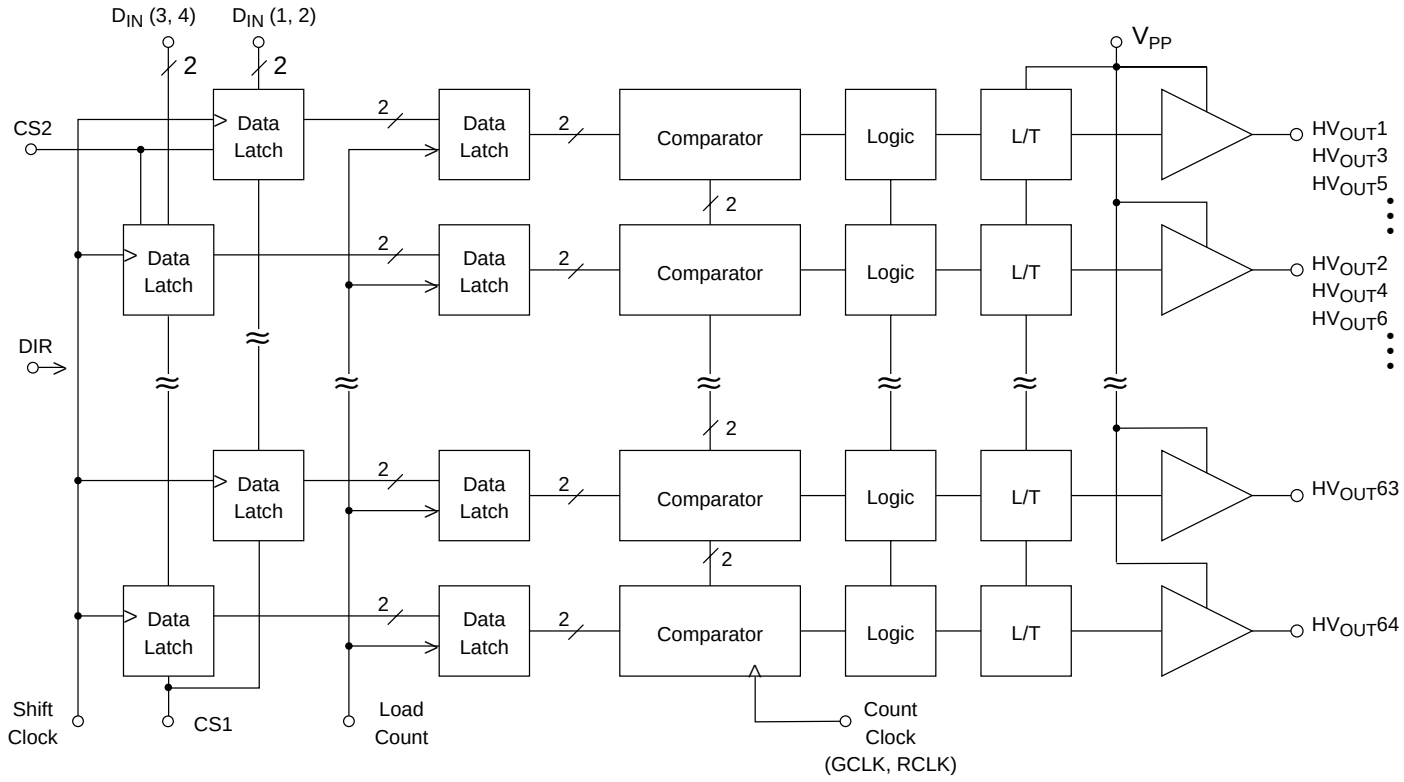
Pad Definitions

Pad #	Name	I/O	Function
2 - 5 18 -21	$D_{IN}1$ - $D_{IN}4$	I	Inputs for binary-format parallel data (D_{IN}^2 and D_{IN}^4 are the most significant bits)
23, 33	Shift Clock	I	Latching data on both edges
24, 32	CS1	I/O	Input when DIR = 0; Output when DIR = 1
10, 22	CS2	I/O	Output when DIR = 0; Input when DIR = 1
8, 15	Load Count	I	Initiates the conversion
26, 30	DIR	I	Controls the data shift directions
27, 29	GND	—	Logic ground
14, 28	HVGND	—	High voltage ground
1, 41	V_{PP}	—	High voltage supply
42-105	$HV_{OUT}1$ – 64	O	High voltage outputs
25, 31	V_{DD}	—	Logic supply voltage
6, 17	Count Clock (GCLK)	I	Input for incrementing the master counter for the green pixel
7, 16	Count Clock (RCLK)	I	Input for incrementing the master counter for the red pixel

Function Table

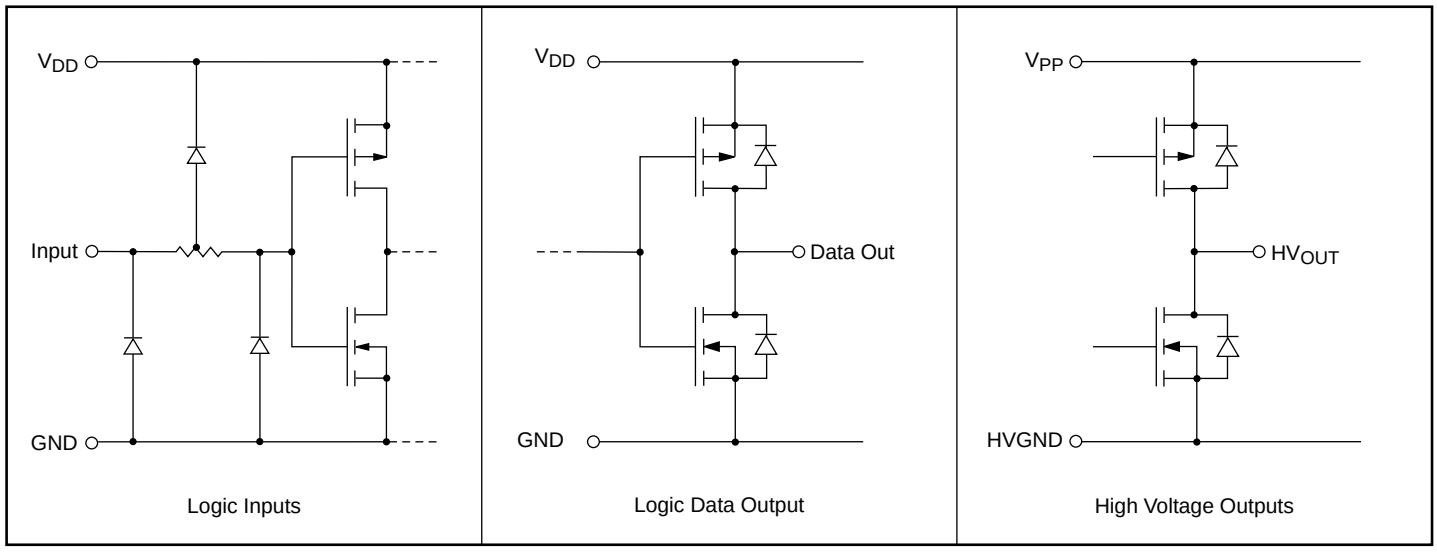
Sequence	Function	Data-In (D1 - D4)	CS1/ CS2	CS2/ CS1	Shift Clock	Load Count	Count Clock (RCLK, GCLK)	HV_{OUT}
1	Load data from data bus	H/L		X		L	H	L
2	Load counter	X	L	X	X		H	
3	Counting/conversion	X	L	X	X	L		H/L
4	Next cycle	H/L		X		L	H	L

Functional Block Diagram



L/T = Level Translator

Input and Output Equivalent Circuits



Timing Diagrams