

OKI Semiconductor**FEDD51V65405E-03**
Issue Date: Jul. 19, 2005**MD51V65405E****16,777,216-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO****DESCRIPTION**

The MD51V65405E is a 16,777,216-word × 4-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MD51V65405E achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MD51V65405E is available in a 32-pin plastic SOJ or 32-pin plastic TSOP.

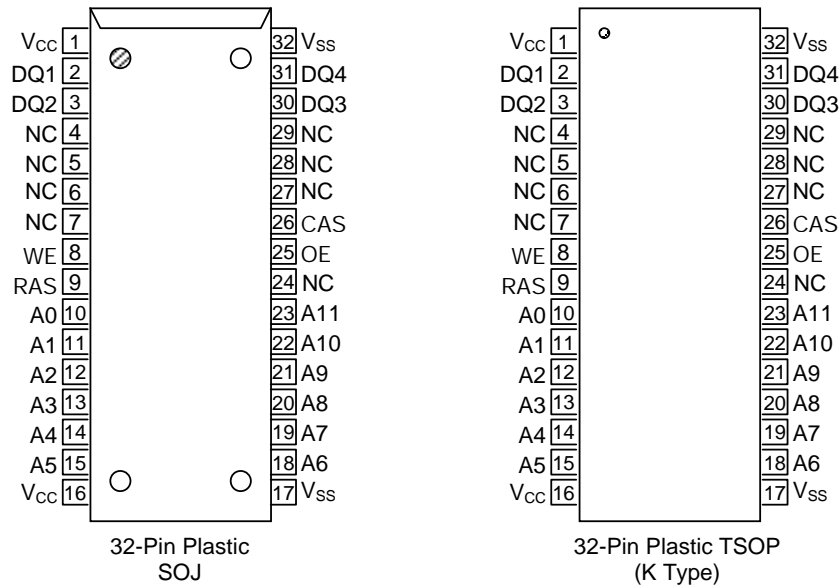
FEATURES

- 16,777,216-word × 4-bit configuration
 - Single 3.3V power supply, ±0.3V tolerance
 - Input : LVTTL compatible, low input capacitance
 - Output : LVTTL compatible, 3-state
 - Refresh :
 - RAS only refresh : 4096 cycles/64ms
 - CAS before RAS refresh, hidden refresh : 4096 cycles/64ms
 - Fast page mode with EDO, read modify write capability
 - CAS before RAS refresh, hidden refresh, RAS-only refresh capability
 - Packages
 - 32-pin 400mil plastic SOJ (SOJ32-P-400-1.27) (Product : MD51V65405E-xxJA)
 - 32-pin 400mil plastic TSOP (TSOPII32-P-400-1.27-K) (Product : MD51V65405E-xxTA)
- xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MD51V65405E	50ns	25ns	13ns	13ns	84ns	504mW	1.8mW
	60ns	30ns	15ns	15ns	104ns	432mW	

PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0–A11	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
DQ1–DQ4	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V _{CC}	Power Supply (3.3V)
V _{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

ELECTRICAL CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to $V_{CC}+0.5$	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D^*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$ **RECOMMENDED OPERATING CONDITIONS** $(T_a = 0 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC} + 0.3^{*1}$	V
Input Low Voltage	V_{IL}	-0.3^{*2}	—	0.8	V

Notes: *1. The input voltage is $V_{CC} + 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

PIN CAPACITANCE $(V_{CC} = 3.3\text{V} \pm 0.3\text{V}, T_a = 25^{\circ}\text{C}, f = 1 \text{ MHz})$

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 – A11)	C_{IN1}	—	5	pF
Input Capacitance (RAS, CAS, WE, OE)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 – DQ4)	$C_{I/O}$	—	7	pF

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MD51V65405 E-50		MD51V65405 E-60		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -2.0mA	2.4	V _{CC}	2.4	V _{CC}	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0V ≤ V _I ≤ V _{CC} +0.3V; All other pins not under test = 0V	- 10	10	- 10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0V ≤ V _O ≤ V _{CC}	- 10	10	- 10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	RAS, CAS cycling, t _{RC} = Min.	—	140	—	120	mA	1,2
Power Supply Current (Standby)	I _{CC2}	RAS, CAS = V _{IH}	—	1	—	1	mA	1
		RAS, CAS ≥ V _{CC} - 0.2V	—	0.5	—	0.5		
Average Power Supply Current (RAS-only Refresh)	I _{CC3}	RAS cycling, CAS = V _{IH} , t _{RC} = Min.	—	140	—	120	mA	1,2
Power Supply Current (Standby)	I _{CC5}	RAS = V _{IH} , CAS = V _{IL} , DQ = enable	—	5	—	5	mA	1
Average Power Supply Current (CAS before RAS Refresh)	I _{CC6}	RAS = cycling, CAS before RAS	—	140	—	120	mA	1,2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	RAS = V _{IL} , CAS cycling, t _{HPC} = Min.	—	140	—	120	mA	1,3

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while RAS = V_{IL}.
3. The address can be changed once or less while CAS = V_{IH}.

AC CHARACTERISTICS (1/2)

 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0 \text{ to } 70^\circ\text{C})$ Note1,2,3

Parameter	Symbol	MD51V65405 E-50		MD51V65405 E-60		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	84	—	104	—	ns	
Read Modify Write Cycle Time	t _{RWC}	110	—	135	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	20	—	25	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{HPRWC}	58	—	68	—	ns	
Access Time from RAS	t _{RAC}	—	50	—	60	ns	4, 5, 6
Access Time from CAS	t _{CAC}	—	13	—	15	ns	4,5
Access Time from Column Address	t _{AA}	—	25	—	30	ns	4,6
Access Time from CAS Precharge	t _{CPA}	—	30	—	35	ns	4
Access Time from OE	t _{OEa}	—	13	—	15	ns	4
Output Low Impedance Time from CAS	t _{CLZ}	0	—	0	—	ns	4
Data Output Hold After CAS Low	t _{DOH}	5	—	5	—	ns	
CAS to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	13	0	15	ns	7,8
RAS to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	13	0	15	ns	7,8
OE to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	ns	7
WE to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	13	0	15	ns	7
Transition Time	t _T	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	64	—	64	ms	
RAS Precharge Time	t _{RP}	30	—	40	—	ns	
RAS Pulse Width	t _{RAS}	50	10,000	60	10,000	ns	
RAS Pulse Width (Fast Page Mode with EDO)	t _{RASP}	50	100,000	60	100,000	ns	
RAS Hold Time	t _{RSH}	7	—	10	—	ns	
RAS Hold Time referenced to OE	t _{ROH}	7	—	10	—	ns	
CAS Precharge Time (Fast Page Mode with EDO)	t _{CP}	7	—	10	—	ns	
CAS Pulse Width	t _{CAS}	7	10,000	10	10,000	ns	
CAS Hold Time	t _{CSH}	35	—	40	—	ns	
CAS to RAS Precharge Time	t _{CRP}	5	—	5	—	ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	30	—	35	—	ns	
OE Hold Time from CAS (DQ Disable)	t _{CHO}	5	—	5	—	ns	

AC CHARACTERISTICS (2/2)

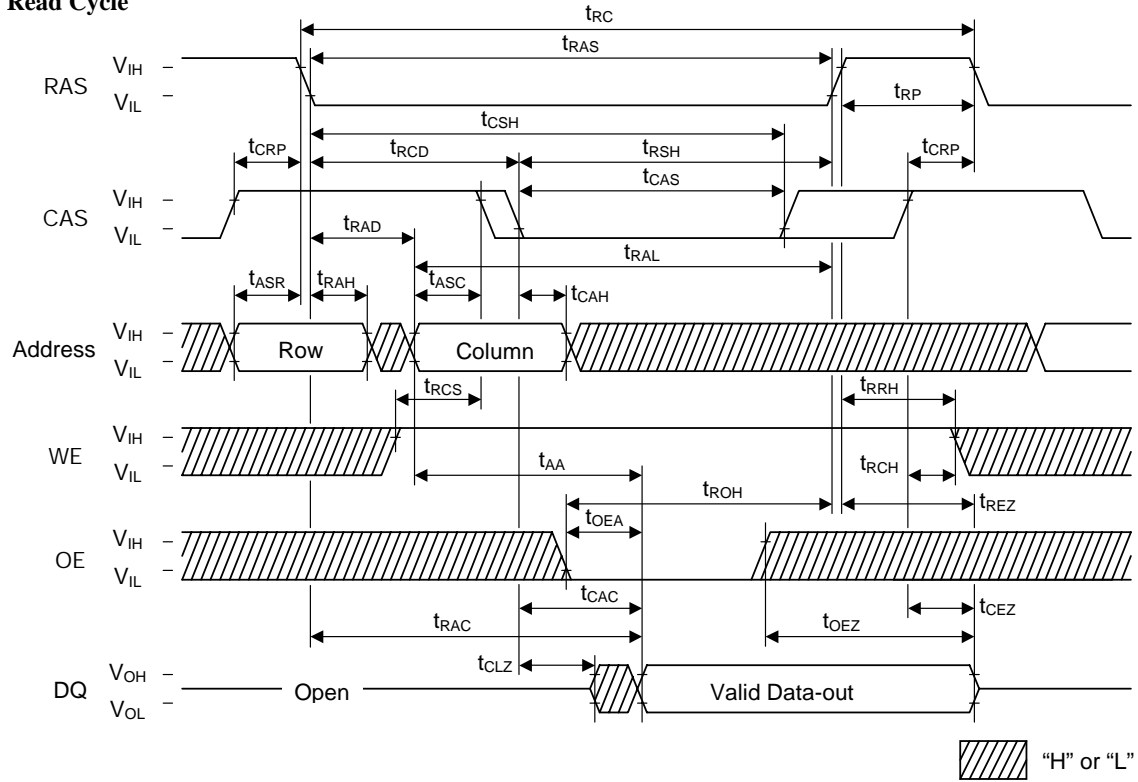
 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0 \text{ to } 70^\circ\text{C})$ Note1,2,3

Parameter	Symbol	MD51V65405 E-50		MD51V65405 E-60		Unit	Note
		Min.	Max.	Min.	Max.		
RAS to CAS Delay Time	t_{RCD}	11	37	14	45	ns	5
RAS to Column Address Delay Time	t_{RAD}	9	25	12	30	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	7	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	7	—	10	—	ns	
Column Address to RAS Lead Time	t_{RAL}	25	—	30	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	9
Read Command Hold Time referenced to RAS	t_{RRH}	0	—	0	—	ns	9
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	7	—	10	—	ns	
Write Command Pulse Width	t_{WP}	7	—	10	—	ns	
WE Pulse Width (DQ Disable)	t_{WPE}	7	—	10	—	ns	
OE Command Hold Time	t_{OEH}	7	—	10	—	ns	
OE Precharge Time	t_{OEP}	7	—	10	—	ns	
OE Command Hold Time	t_{OCH}	7	—	10	—	ns	
Write Command to RAS Lead Time	t_{RWL}	7	—	10	—	ns	
Write Command to CAS Lead Time	t_{CWL}	7	—	10	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	7	—	10	—	ns	11
OE to Data-in Delay Time	t_{OED}	13	—	15	—	ns	
CAS to WE Delay Time	t_{CWD}	30	—	34	—	ns	10
Column Address to WE Delay Time	t_{AWD}	42	—	49	—	ns	10
RAS to WE Delay Time	t_{RWD}	67	—	79	—	ns	10
CAS Precharge WE Delay Time	t_{CPWD}	47	—	54	—	ns	10
CAS Active Delay Time from RAS Precharge	t_{RPC}	5	—	5	—	ns	
RAS to CAS Set-up Time (CAS before RAS)	t_{CSR}	5	—	5	—	ns	
RAS to CAS Hold Time(CAS before RAS)	t_{CHR}	10	—	10	—	ns	
WE to RAS Hold Time(CAS before RAS)	t_{WRP}	10	—	10	—	ns	
WE Hold Time(CAS before RAS)	t_{WRH}	10	—	10	—	ns	

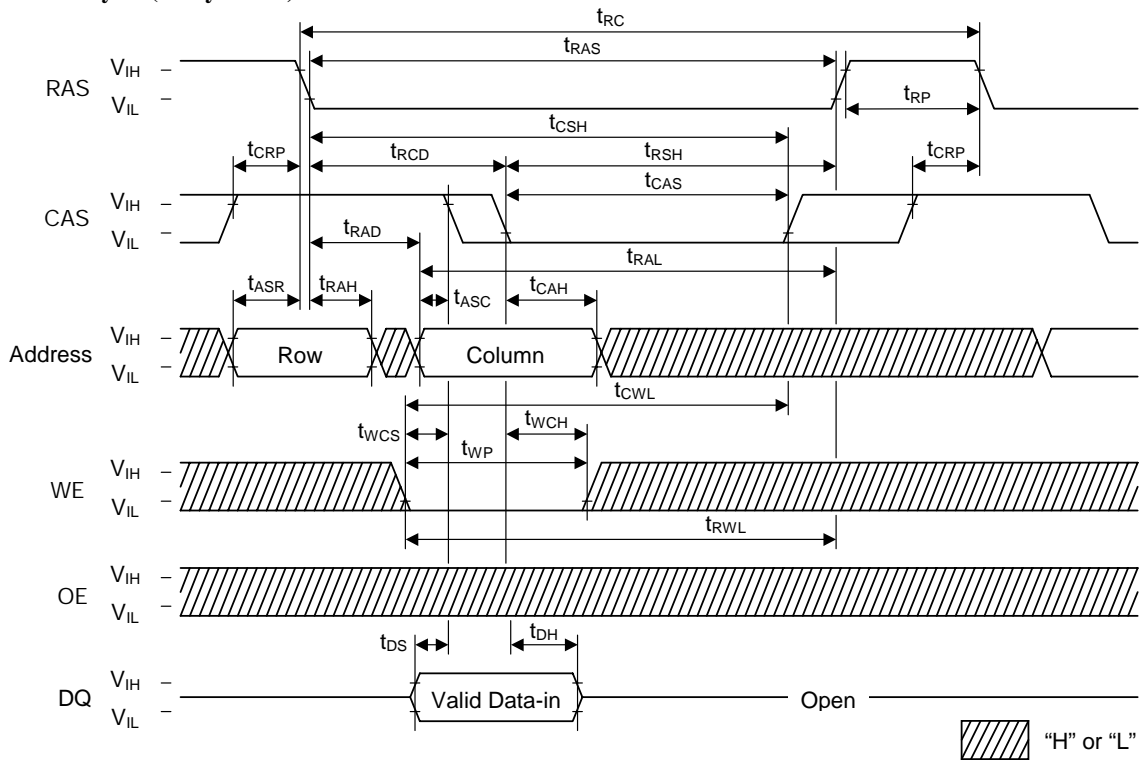
- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles (RAS-only refresh or CAS before RAS refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF. The output timing reference levels are $V_{OH}=2.0$ and $V_{OL}=0.8$ V.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.), and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} , and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the CAS, leading edges in an early write cycle, and to the WE leading edge in an OE control write cycle, or a read modify write cycle.

TIMING CHART

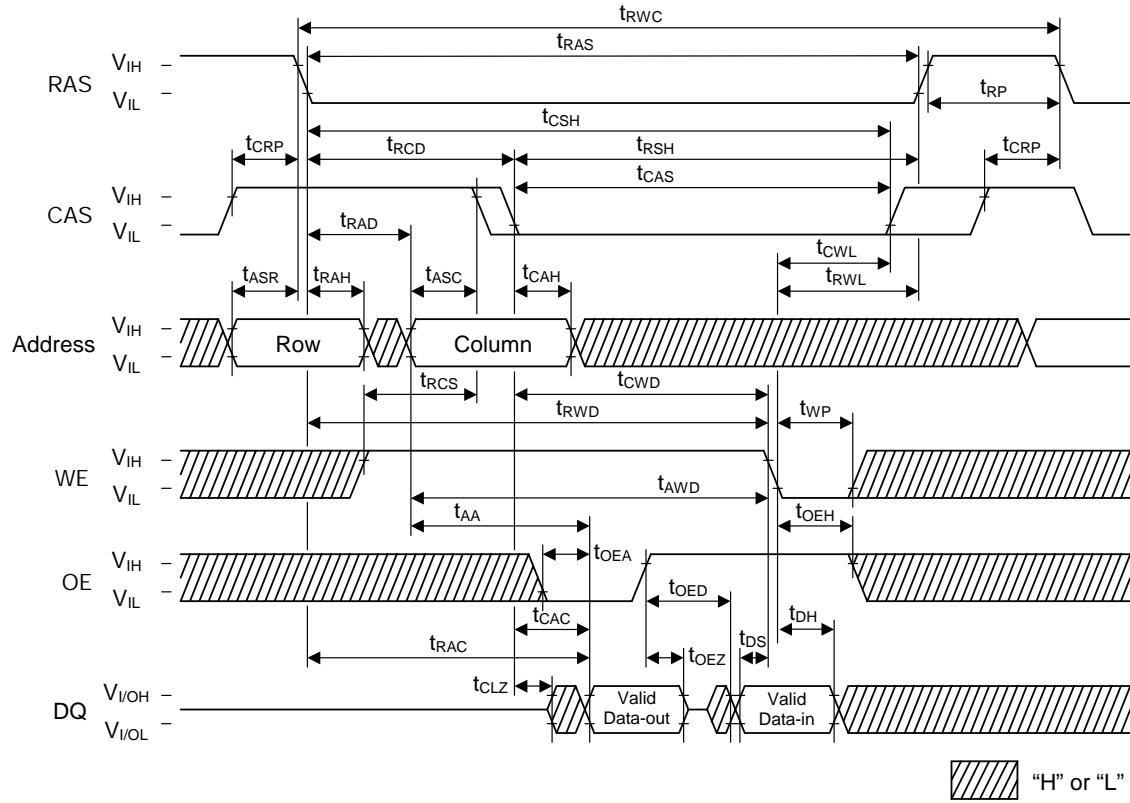
Read Cycle



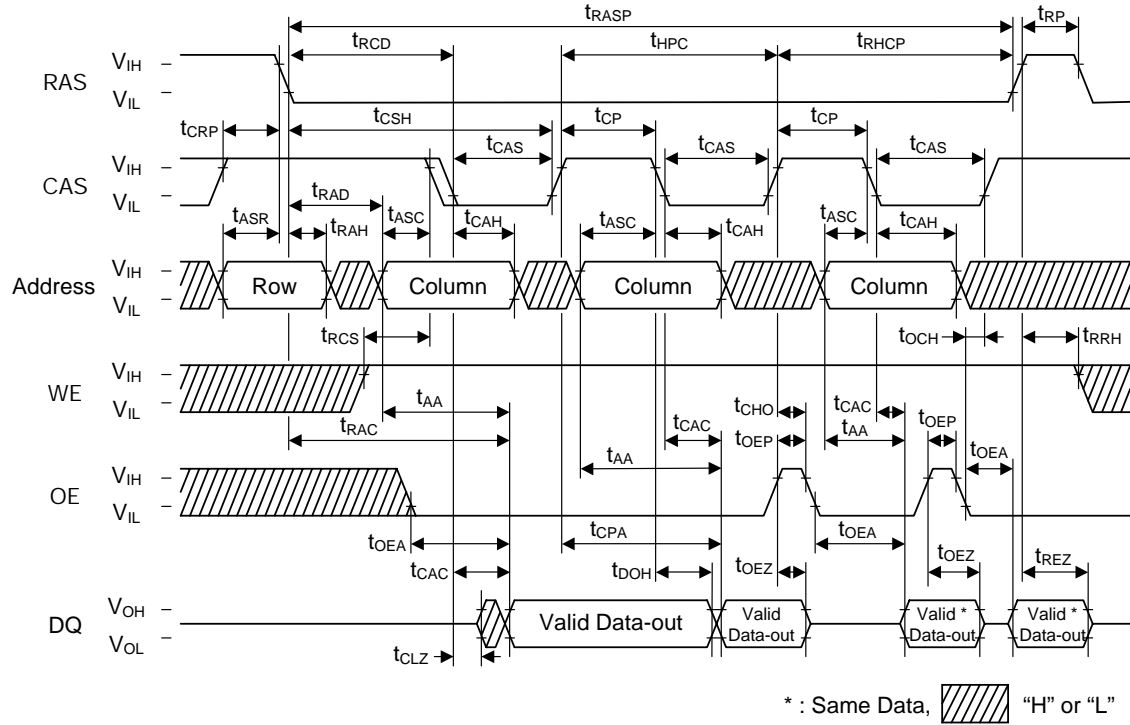
Write Cycle (Early Write)



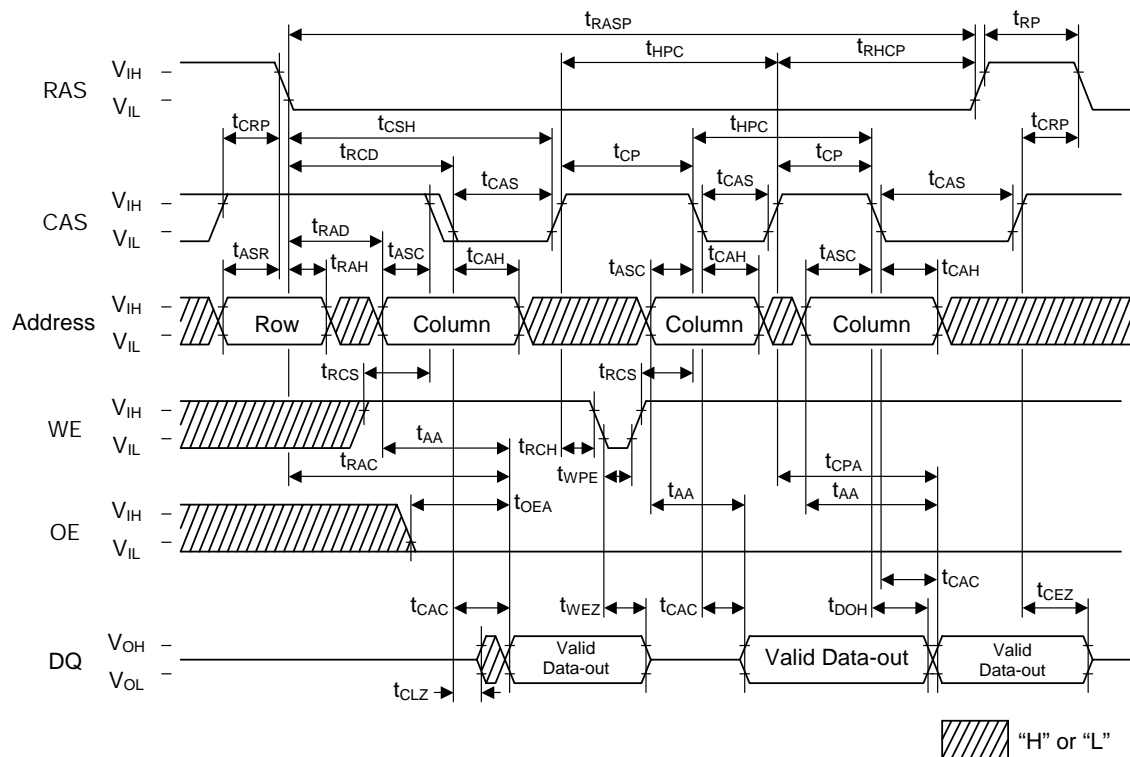
Read Modify Write Cycle



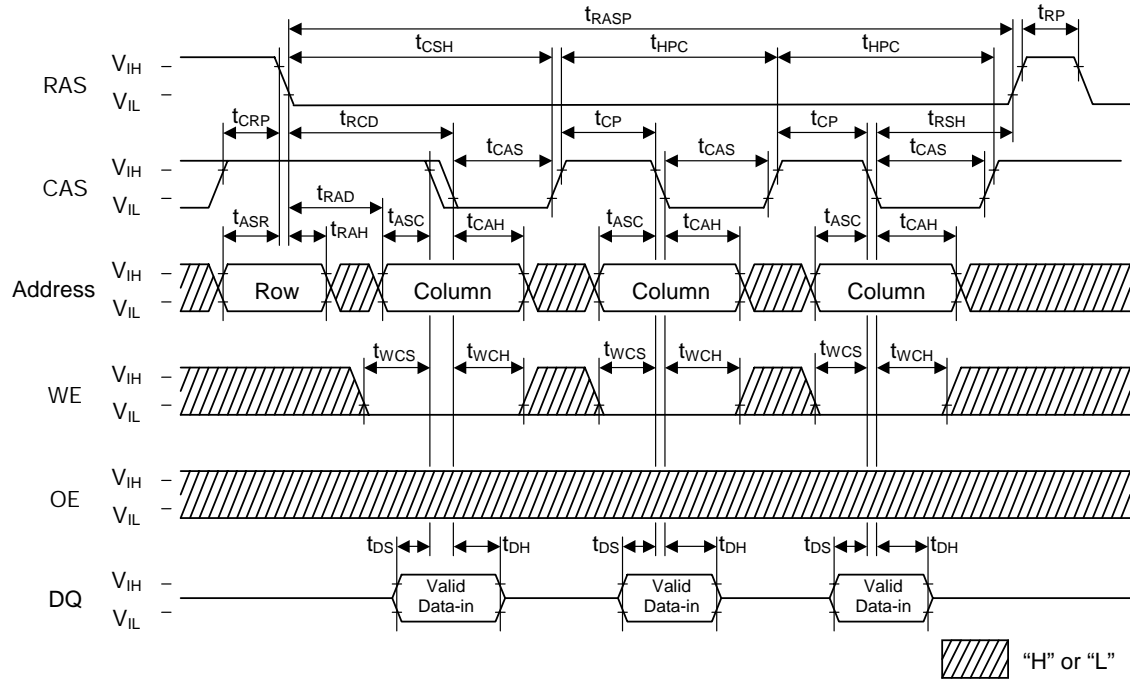
Fast Page Mode Read Cycle (Part-1)



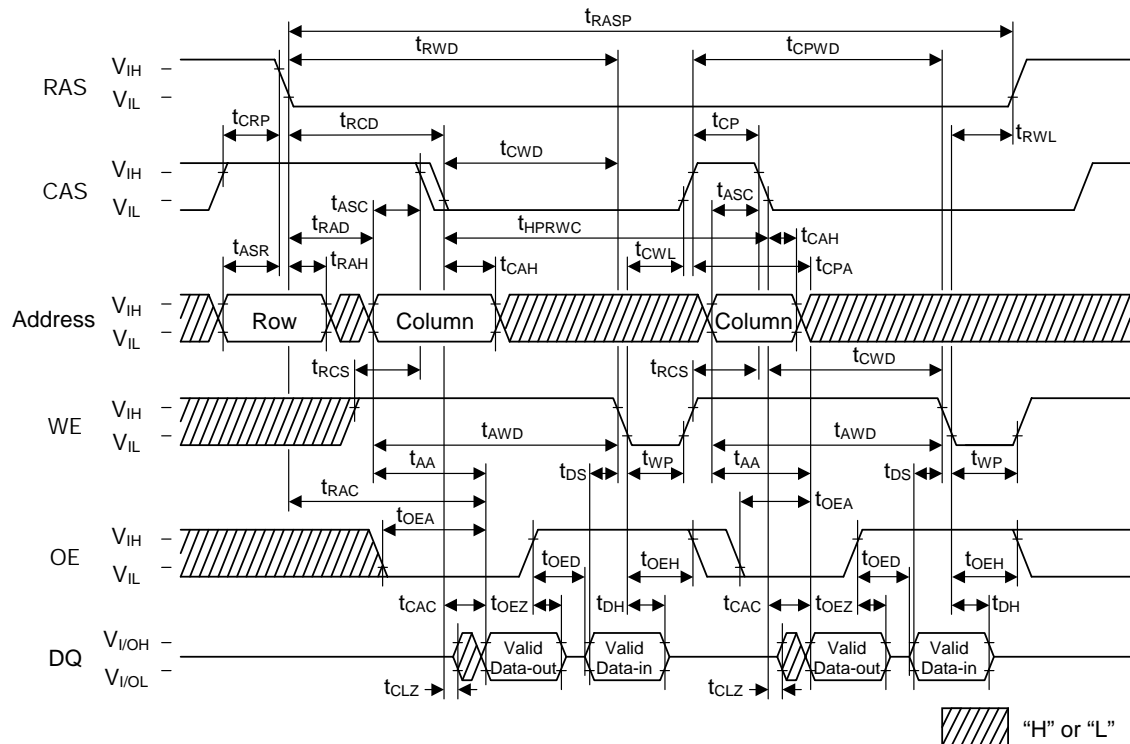
Fast Page Mode Read Cycle (Part-2)



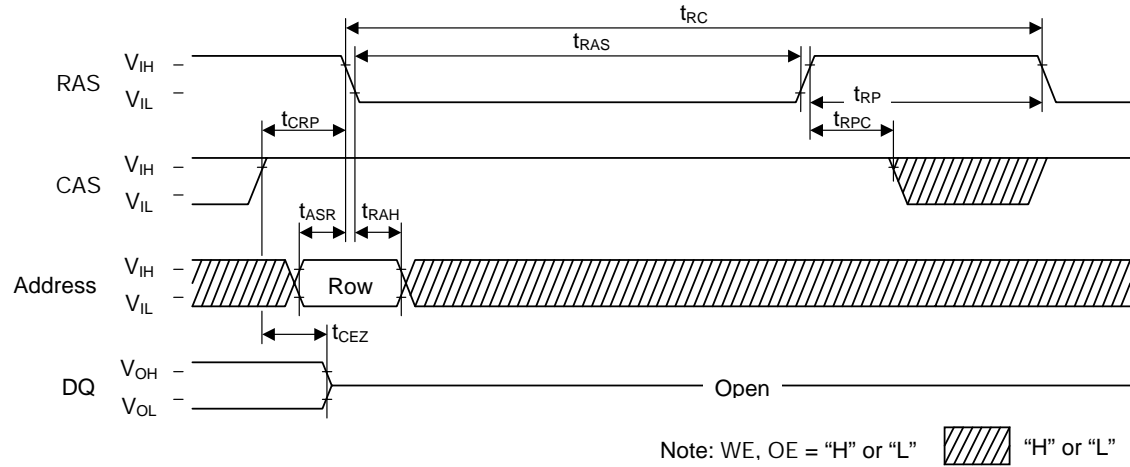
Fast Page Mode Write Cycle (Early Write)



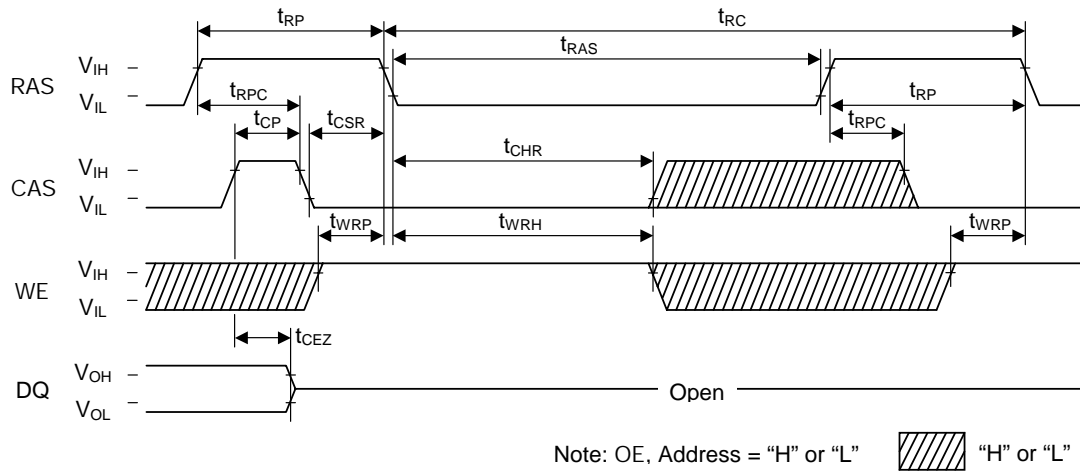
Fast Page Mode Read Modify Write Cycle



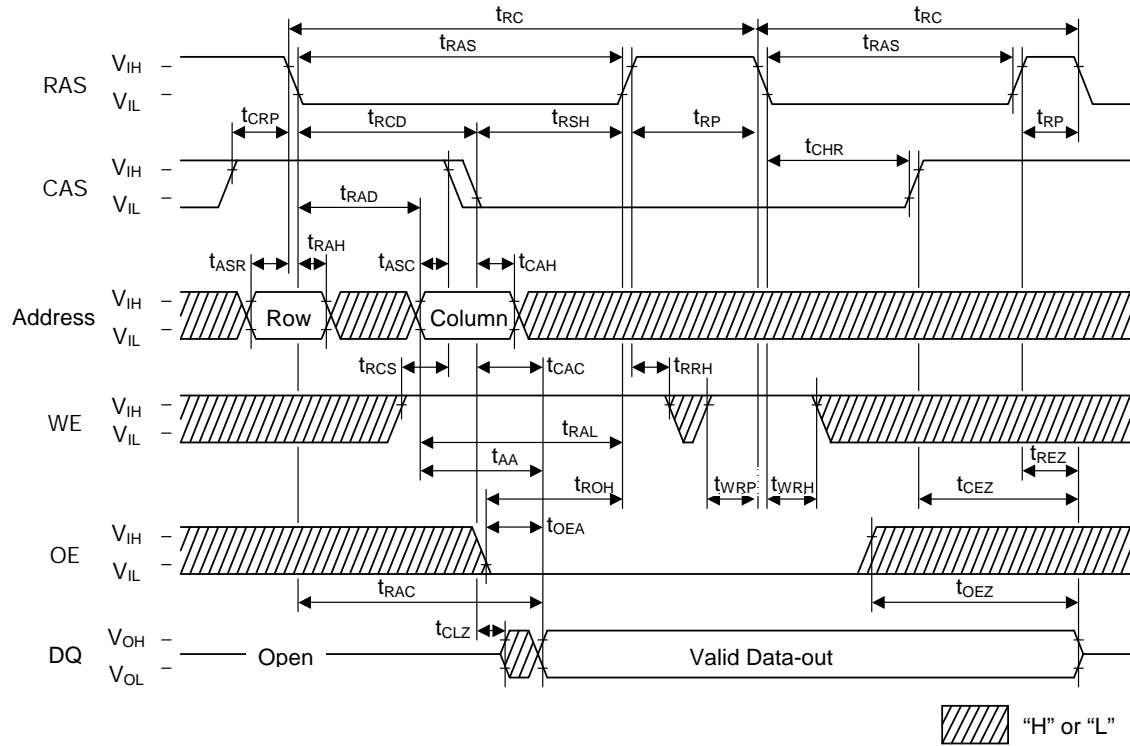
RAS-only Refresh Cycle



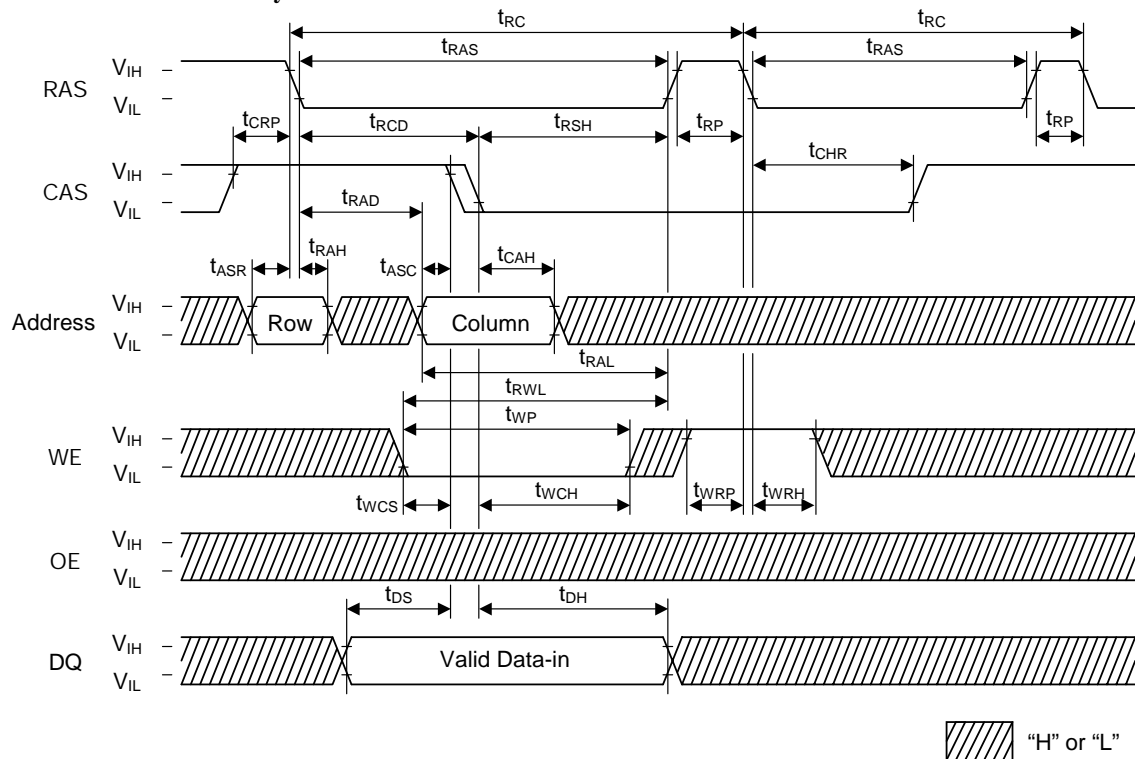
CAS before RAS Refresh Cycle



Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDD51V65405E-01	Jul., 1, 2002	–	–	Preliminary edition 1
FEDD51V65405E-01	Dec., 27, 2002	–	–	Final edition
FEDD51V65405E-02	Oct., 30, 2003	–	–	Fixed errata
FEDD51V65405E-03	Jul. 19, 2005	3	–	Block Diagram deleted

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