

## N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)
N-Channel	20	0.052 at V <sub>GS</sub> = 4.5 V	6.1 <sup>a</sup>	3.9 nc
		0.084 at V <sub>GS</sub> = 2.5 V	4.8 <sup>a</sup>	
P-Channel	-20	0.090 at V <sub>GS</sub> = -4.5 V	-4.8 <sup>a</sup>	3.8 nc
		0.160 at V <sub>GS</sub> = -2.5 V	-3.6 <sup>a</sup>	

### FEATURES

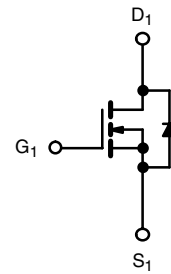
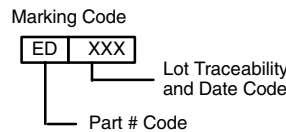
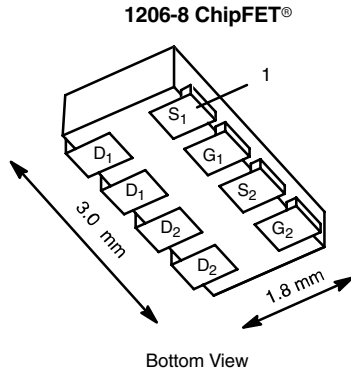
- TrenchFET® Power MOSFETs

### APPLICATIONS

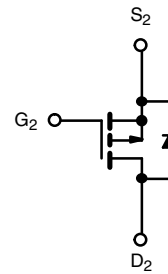
- Complementary MOSFET for Portable Devices
  - Ideal for Buck–Boost Circuits



RoHS  
COMPLIANT



N-Channel MOSFET



P-Channel MOSFET

Ordering Information: Si5509DC-T1-E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V <sub>DS</sub>	20	-20	V
Gate-Source Voltage		V <sub>GS</sub>	± 12		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	6.1 <sup>a</sup>	-4.8 <sup>a</sup>	A
	T <sub>C</sub> = 70 °C		4.9 <sup>a</sup>	-3.8 <sup>a</sup>	
	T <sub>A</sub> = 25 °C		5.0 <sup>b, c</sup>	-3.9 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		3.9 <sup>b, c</sup>	-3.1 <sup>b, c</sup>	
Pulsed Drain Current		I <sub>DM</sub>	10	-15	
Source-Drain Current Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	3.7	-3.7	
	T <sub>A</sub> = 25 °C		1.7 <sup>b, c</sup>	-1.7 <sup>b, c</sup>	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	4.5	4.5	W
	T <sub>C</sub> = 70 °C		2.88	2.88	
	T <sub>A</sub> = 25 °C		2.1 <sup>b, c</sup>	2.1 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		1.33 <sup>b, c</sup>	1.33 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ	Max	Typ	Max	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 sec	R <sub>thJA</sub>	50	60	50	60	°C/W
Maximum Junction-to-Foot (Drain)	Steady-State	R <sub>thJF</sub>	30	40	30	40	

Notes

- Based on T<sub>C</sub> = 25 °C.
- Surface Mounted on 1" x 1" FR4 Board.
- t = 5 sec
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W for both channels.



SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition		Min	Typ <sup>a</sup>	Max	Unit	
<b>Static</b>								
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	N-Ch	20			mV/°C	
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	P-Ch	-20				
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	N-Ch		18.4			
		I <sub>D</sub> = -250 μA	P-Ch		-15.1			
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	N-Ch		-3.4			
		I <sub>D</sub> = -250 μA	P-Ch		2.2			
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.7		2	V	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.7		-2		
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V	N-Ch			100	nA	
			P-Ch			-100		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA	
			P-Ch			-1		
			V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch				10
				P-Ch				-10
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	10			A	
			P-Ch	-15				
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.0 A	N-Ch		0.043	0.052	Ω	
			P-Ch		0.074	0.090		
			V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 3.9 A	N-Ch		0.068		0.084
				P-Ch		0.128		0.160
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	N-Ch		10.4		S	
			P-Ch		8.2			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	C <sub>iss</sub>	<b>N-Channel</b> V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz <b>P-Channel</b> V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	N-Ch		455		pF	
			P-Ch		300			
Output Capacitance	C <sub>oss</sub>		N-Ch		85			
			P-Ch		95			
Reverse Transfer Capacitance	C <sub>rss</sub>		N-Ch		50			
			P-Ch		65			
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 4.0 A V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -5 V, I <sub>D</sub> = -3.9 A <b>N-Channel</b> V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.0 A <b>P-Channel</b> V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.9 A	N-Ch		4.4	6.6	nC	
			P-Ch		4.1	6.2		
			N-Ch		3.8	5.7		
			P-Ch		3.9	5.9		
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.0 A <b>P-Channel</b> V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.9 A	N-Ch		0.9			
			P-Ch		0.7			
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch		0.95			
			P-Ch		1.25			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	N-Ch		1.9		Ω	
			P-Ch		8			



SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 2.5 Ω I <sub>D</sub> ≅ 4.0 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω  P-Channel V <sub>DD</sub> = -10 V, R <sub>L</sub> = 3.2 Ω I <sub>D</sub> ≅ -3.14 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 Ω	N-Ch		6	9	ns
			P-Ch		8	12	
Rise Time	t <sub>r</sub>		N-Ch		95	143	
			P-Ch		75	113	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		12	18	
			P-Ch		25	38	
Fall Time	t <sub>f</sub>		N-Ch		6	9	
			P-Ch		60	90	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	N-Ch			3.75	A
			P-Ch			-3.75	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>		N-Ch			10	A
			P-Ch			-15	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.4 A, V <sub>GS</sub> = 0 V	N-Ch		0.8	1.2	V
		I <sub>S</sub> = -1.5 A, V <sub>GS</sub> = 0 V	P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	N-Channel I <sub>F</sub> = 2.4 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C  P-Channel I <sub>F</sub> = -1.5 A, di/dt = -100 A/μs, T <sub>J</sub> = 25 °C	N-Ch		12	18	ns
			P-Ch		18	27	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		N-Ch		5	8	nC
			P-Ch		8	12	
Reverse Recovery Fall Time	t <sub>a</sub>	N-Ch		7.5		ns	
		P-Ch		14			
Reverse Recovery Rise Time	t <sub>b</sub>	N-Ch		4.5			
		P-Ch		4			

Notes

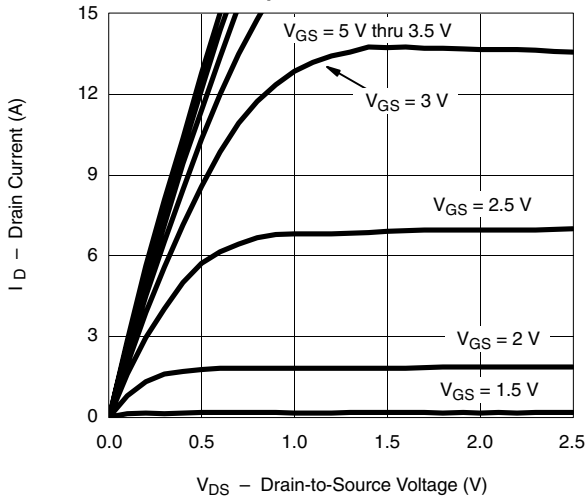
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

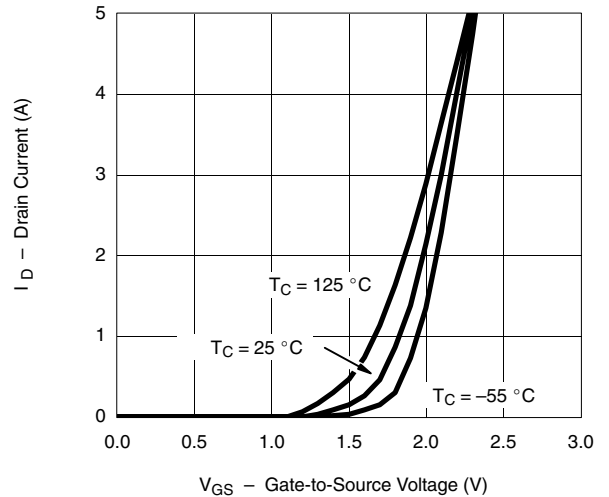
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**N-CHANNEL**

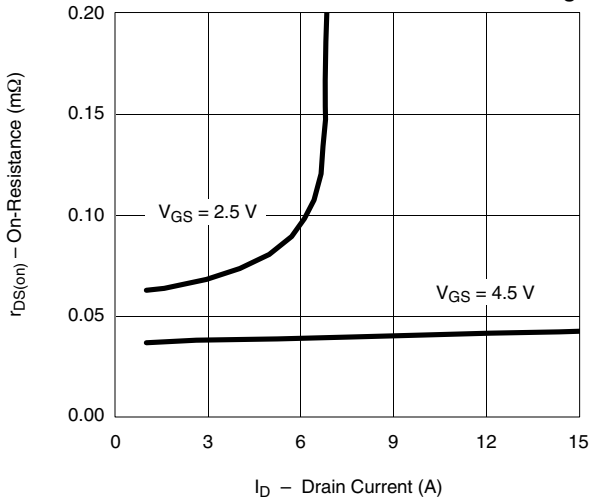
**Output Characteristics**



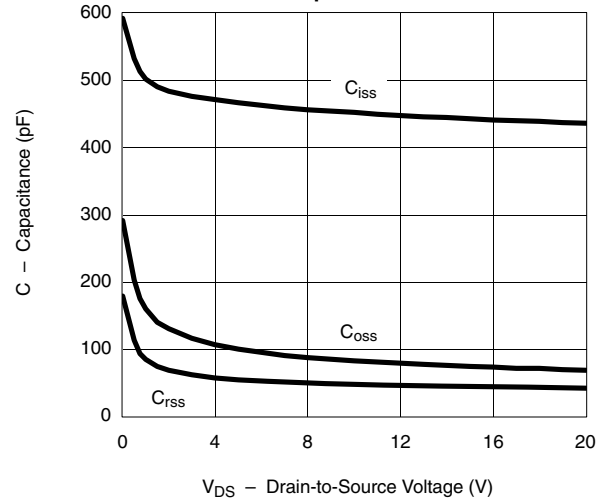
**Transfer Characteristics**



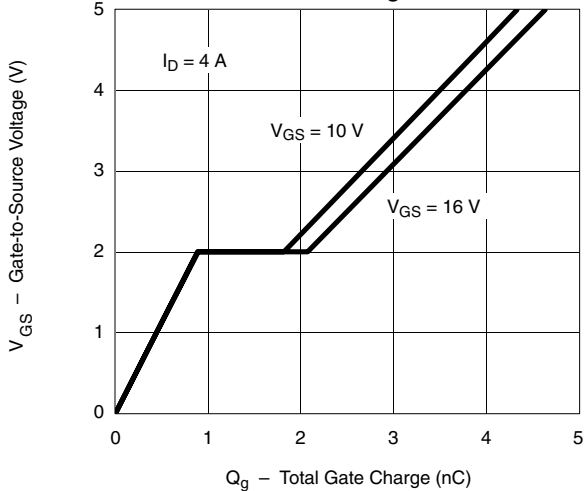
**On-Resistance vs. Drain Current and Gate Voltage**



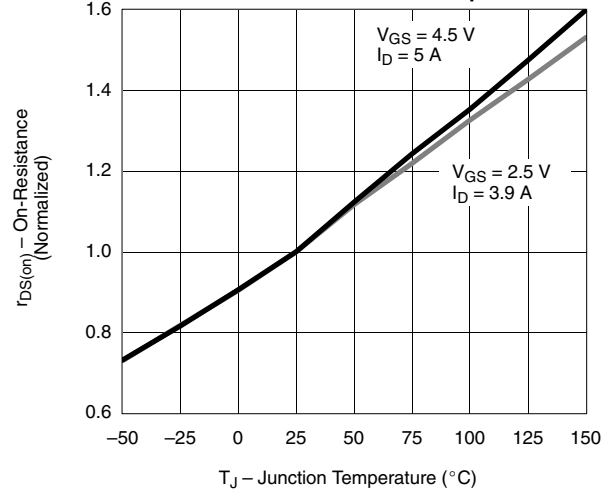
**Capacitance**



**Gate Charge**



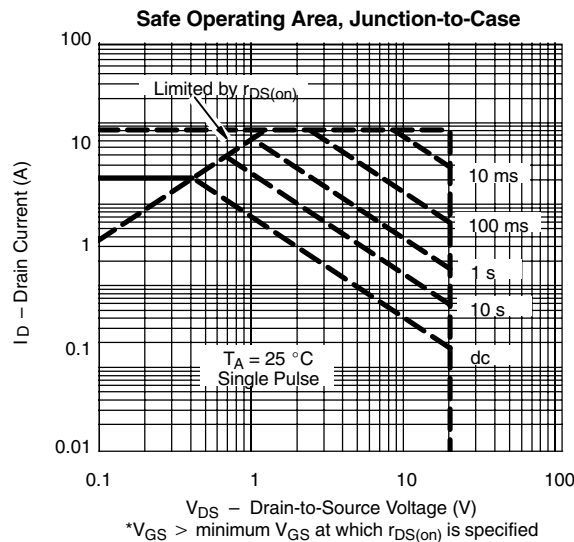
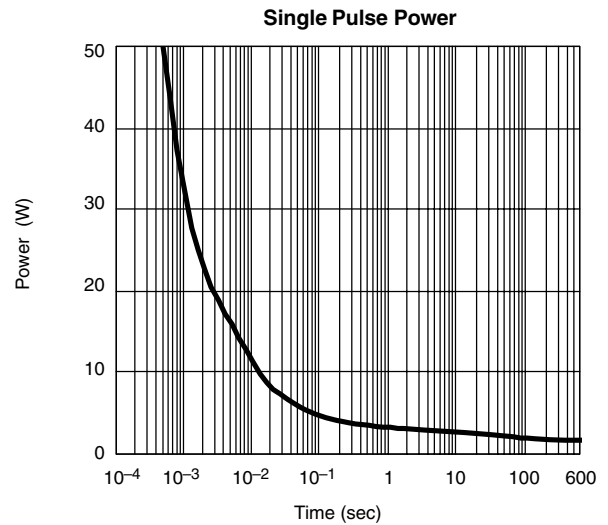
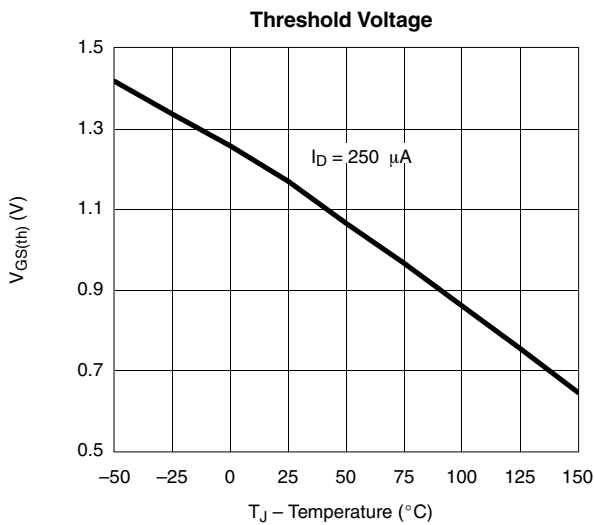
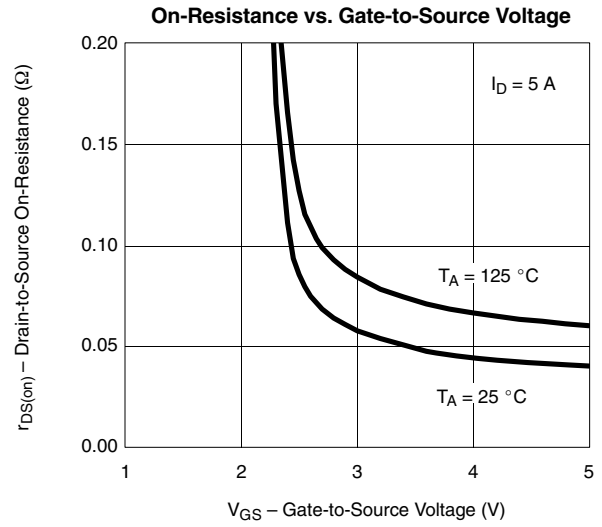
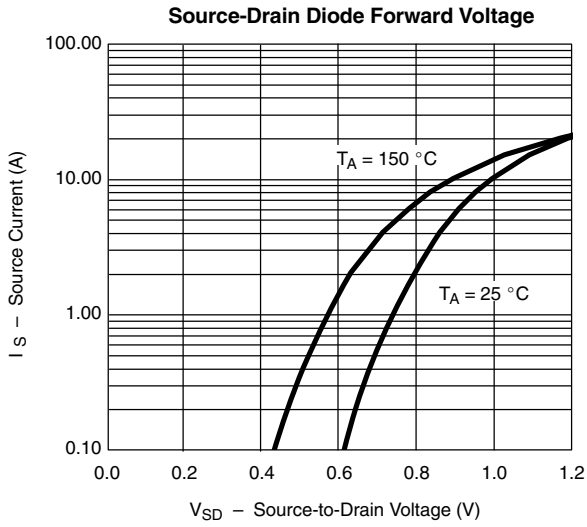
**On-Resistance vs. Junction Temperature**





**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

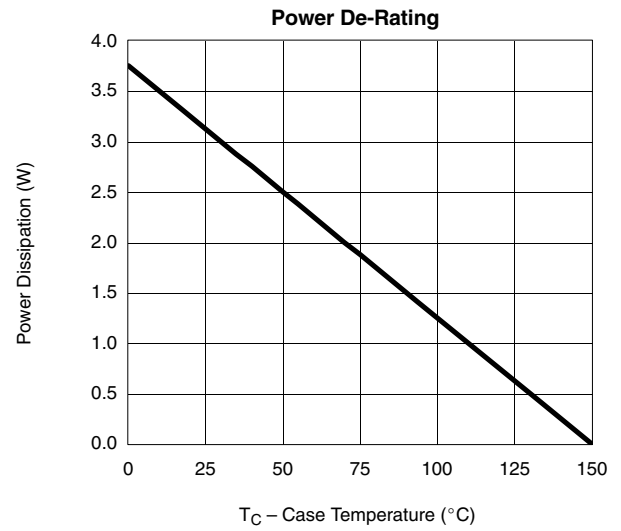
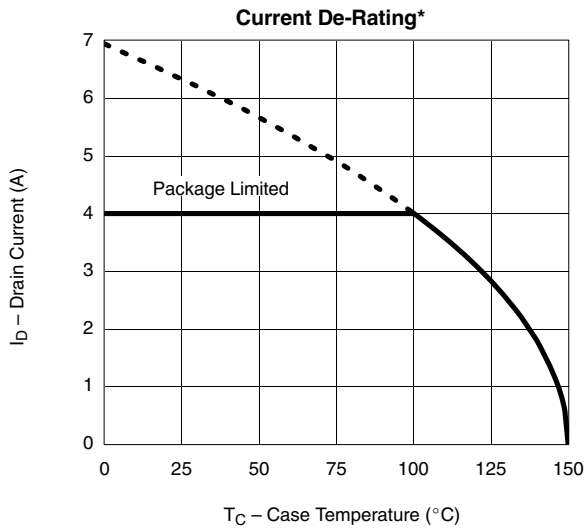
**N-CHANNEL**





**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**N-CHANNEL**

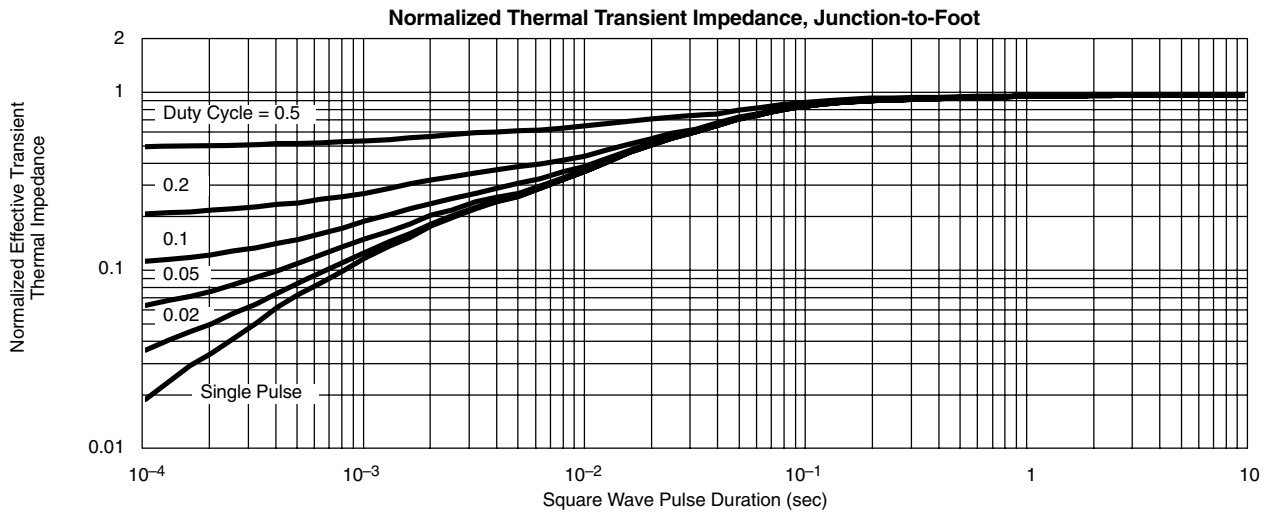
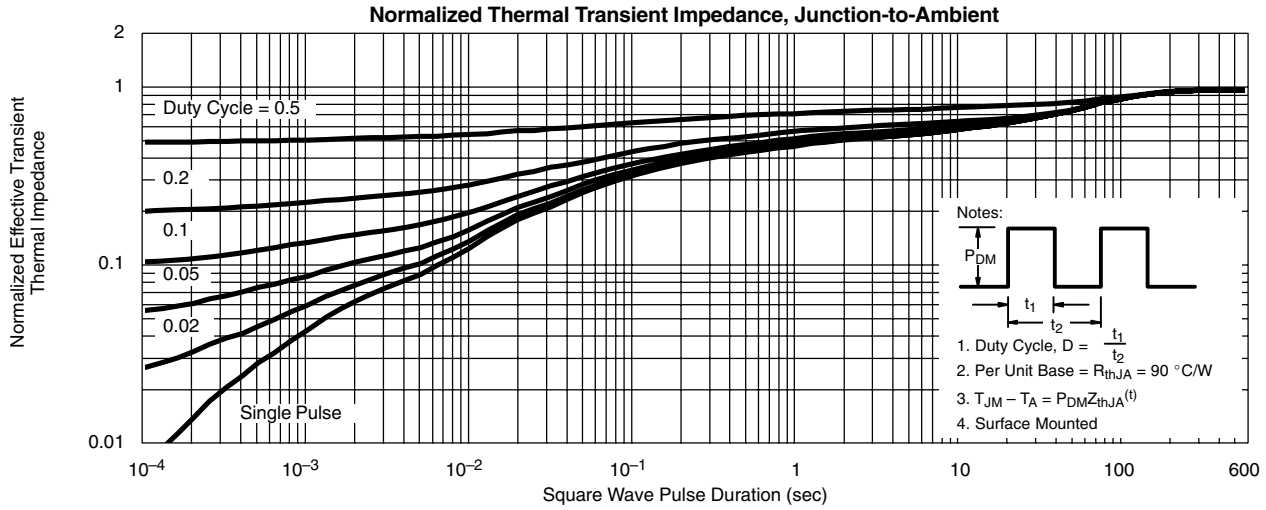


\*The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

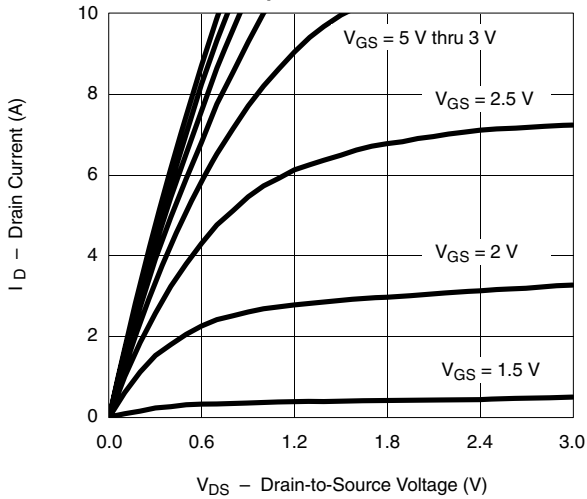
N-CHANNEL



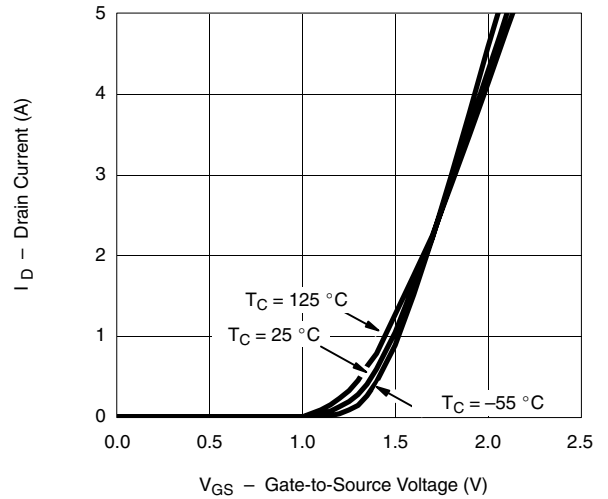
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**P-CHANNEL**

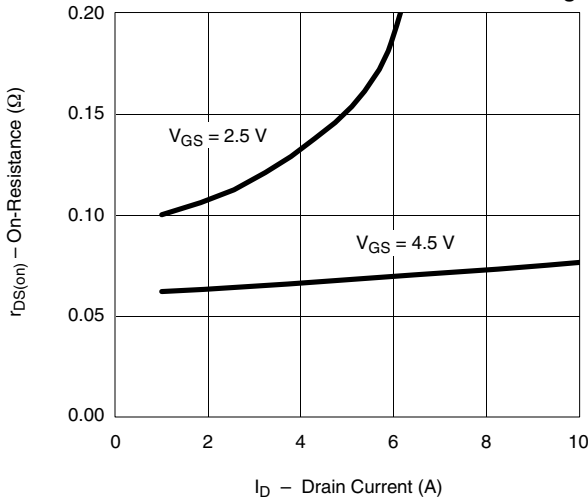
**Output Characteristics**



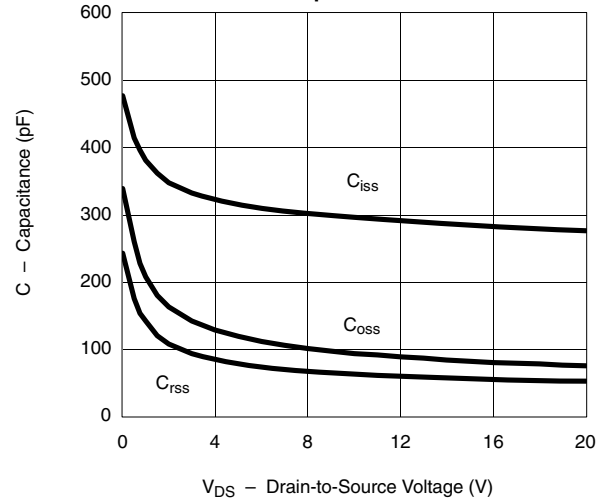
**Transfer Characteristics**



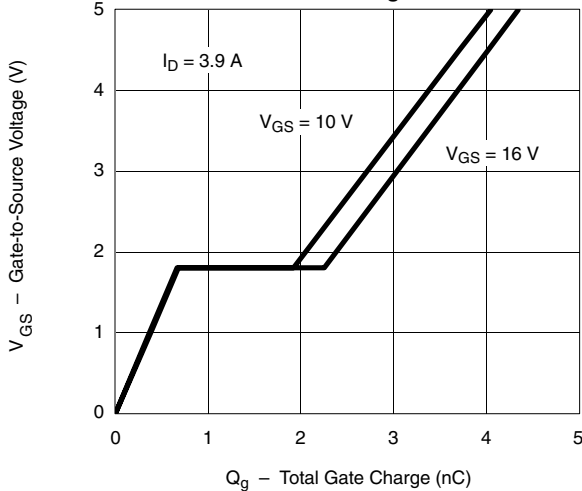
**On-Resistance vs. Drain Current and Gate Voltage**



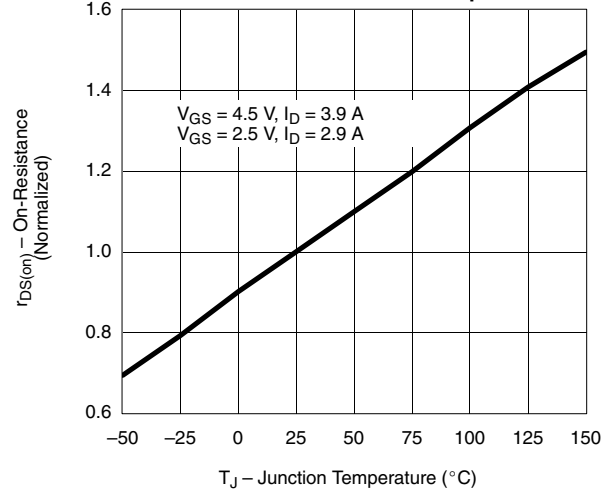
**Capacitance**



**Gate Charge**



**On-Resistance vs. Junction Temperature**

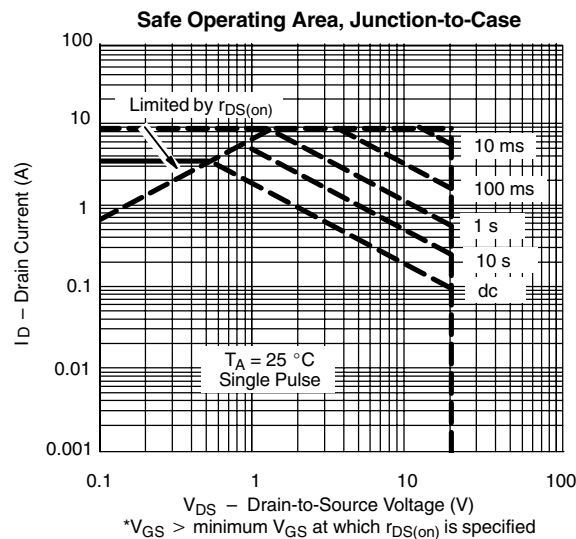
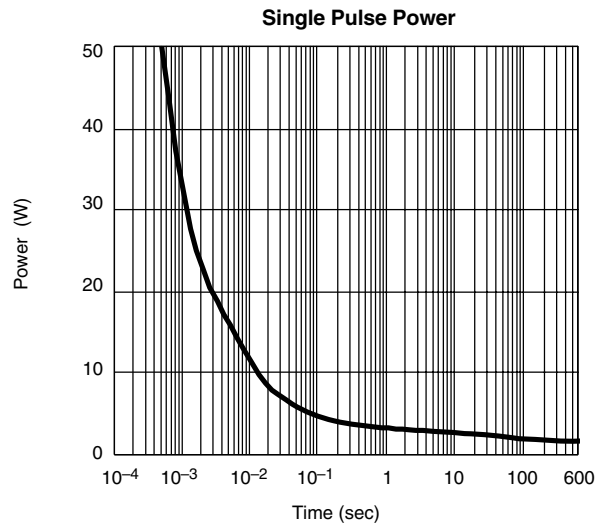
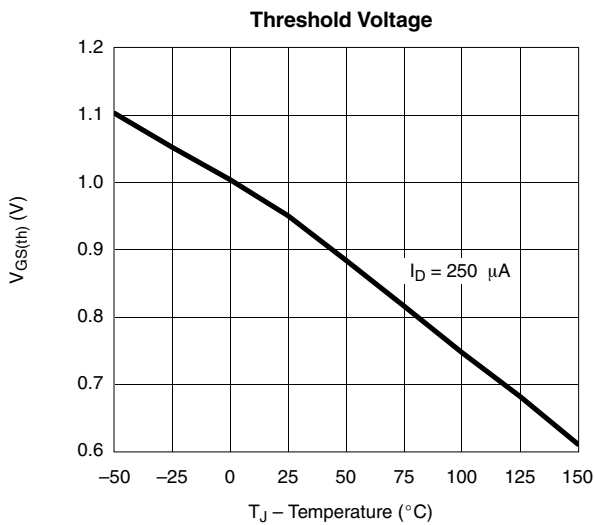
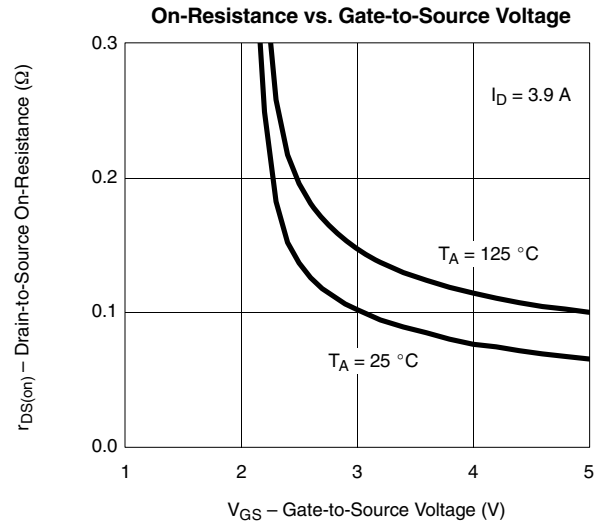
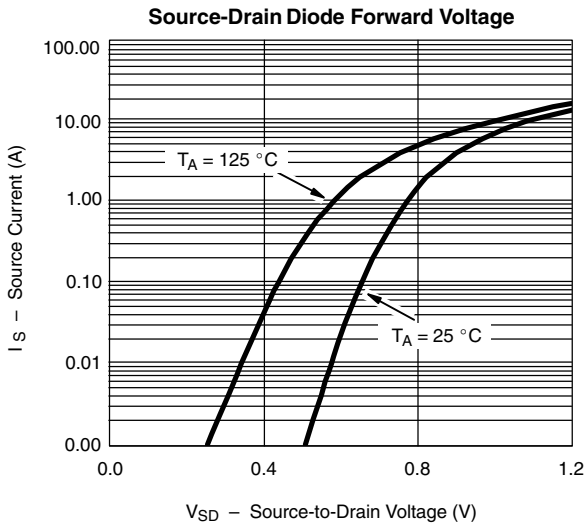






**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

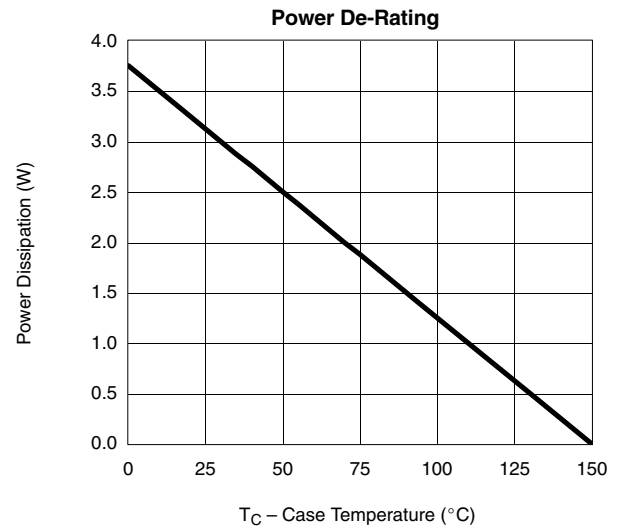
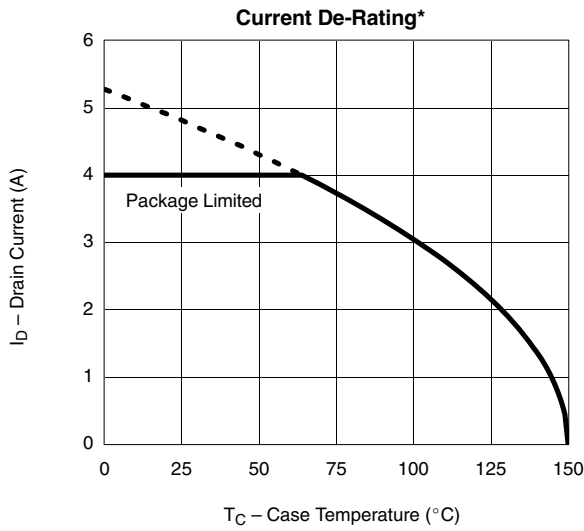
**P-CHANNEL**





**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**P-CHANNEL**

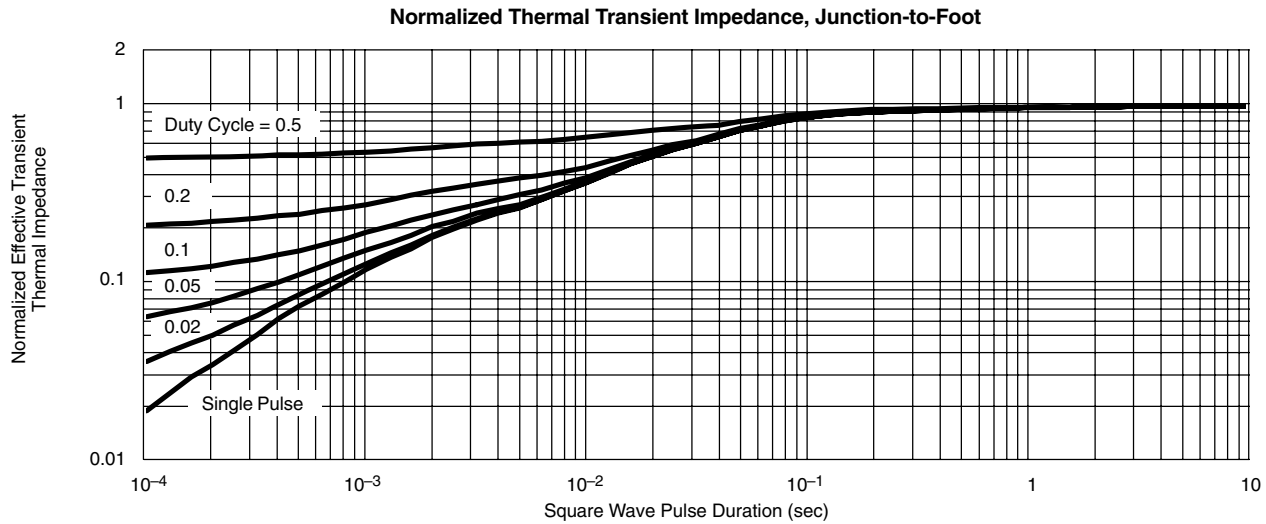
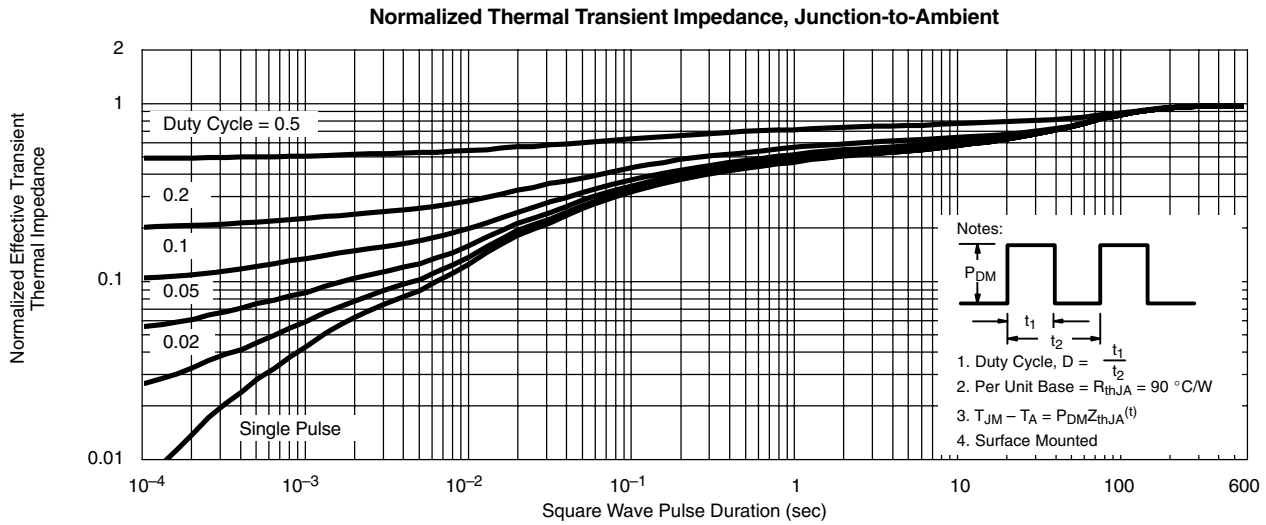


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TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL



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