



New Product

Si5424DC
Vishay Siliconix

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ)
30	0.024 at $V_{GS} = 10$ V	6	11 nC
	0.030 at $V_{GS} = 4.5$ V	6	

FEATURES

- TrenchFET[®] Power MOSFET

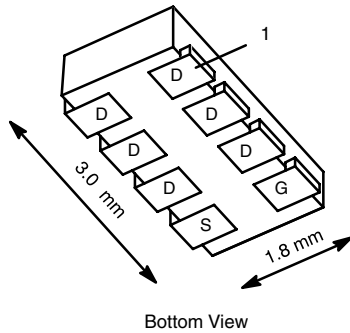
APPLICATIONS

- Load Switch
– Notebook PC

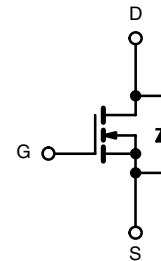
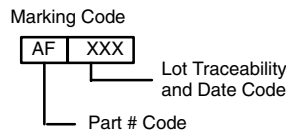


RoHS
COMPLIANT

ChipFET 1206-8



Bottom View



N-Channel MOSFET

Ordering Information: Si5424DC-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 25	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	6 ^a
		$T_C = 70$ °C	6 ^a
		$T_A = 25$ °C	6 ^a
		$T_A = 70$ °C	6 ^a
Pulsed Drain Current	I_{DM}	40	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	2.1 ^{b, c}
Avalanche Current	I_{AS}	16	mJ
Single Pulse Avalanche Energy	E_{AS}	12.8	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	6.25
		$T_C = 70$ °C	4.0
		$T_A = 25$ °C	2.5 ^{b, c}
		$T_A = 70$ °C	1.6 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	40	50	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	15	20	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 Board.
- $t = 5$ sec.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The ChipFET 1206-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		19.4		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			-4.6			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1		2.3	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 25 V			± 100	ns	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40			A	
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.8 A		0.020	0.024	Ω	
		V _{GS} = 4.5 V, I _D = 4.22 A		0.024	0.030		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.8 A		17		S	
Dynamic^b							
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		950		pF	
Output Capacitance	C _{oss}			230			
Reverse Transfer Capacitance	C _{rss}			180			
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 4.8 A		21	32	nC	
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 4.8 A		11	17		
Gate-Source Charge	Q _{gs}			3.2			
Gate-Drain Charge	Q _{gd}		4.2				
Gate Resistance	R _g	f = 1 MHz		2.2		Ω	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 2.63 Ω I _D ≅ 5.7 A, V _{GEN} = 4.5 V, R _g = 1 Ω		17	26	ns	
Rise Time	t _r			75	113		
Turn-Off Delay Time	t _{d(off)}			22	33		
Fall Time	t _f			12	18		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 2.5 Ω I _D ≅ 6 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15		
Rise Time	t _r			38	57		
Turn-Off Delay Time	t _{d(off)}			26	40		
Fall Time	t _f			9	14		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			6		A
Pulse Diode Forward Current	I _{SM}				40		
Body Diode Voltage	V _{SD}	I _S = 4.3 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 4.3 A, di/dt = 100 A/μs, T _J = 25 °C		24	36	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			11	17	nC	
Reverse Recovery Fall Time	t _a			9		ns	
Reverse Recovery Rise Time	t _b			15			

Notes

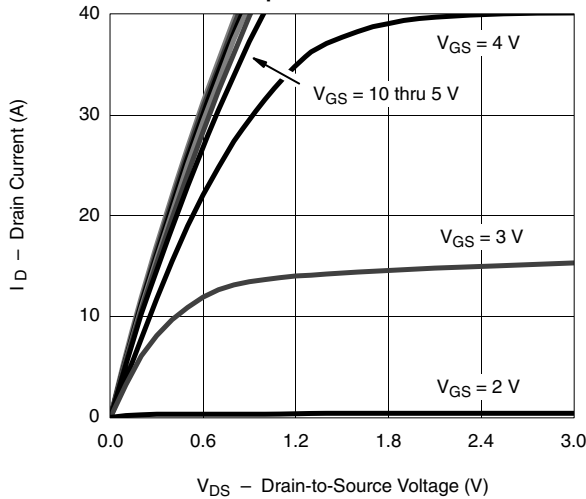
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

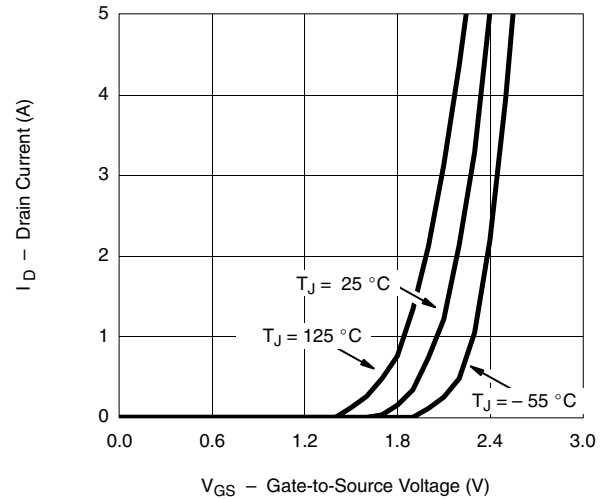


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

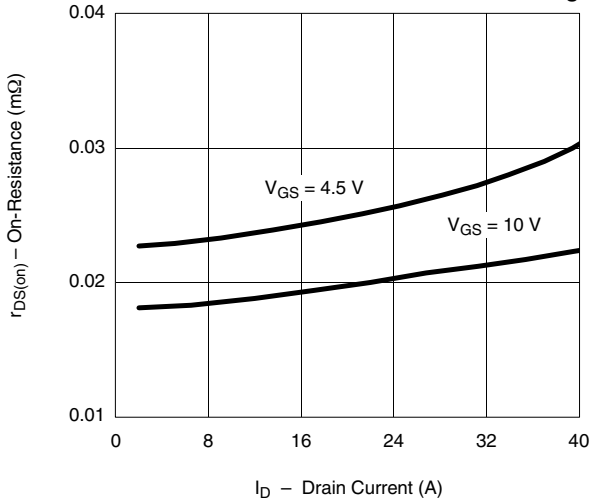
Output Characteristics



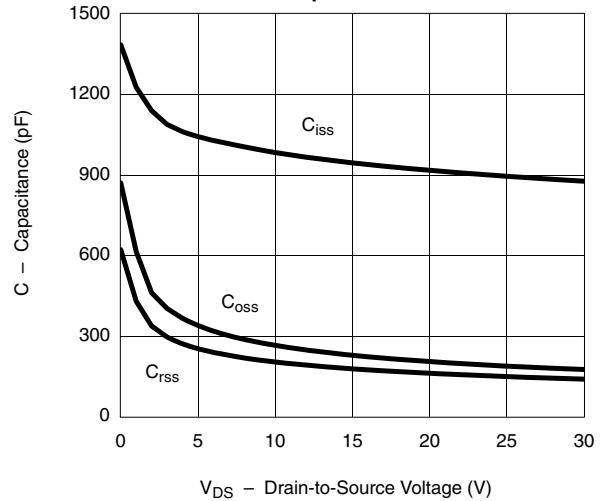
Transfer Characteristics



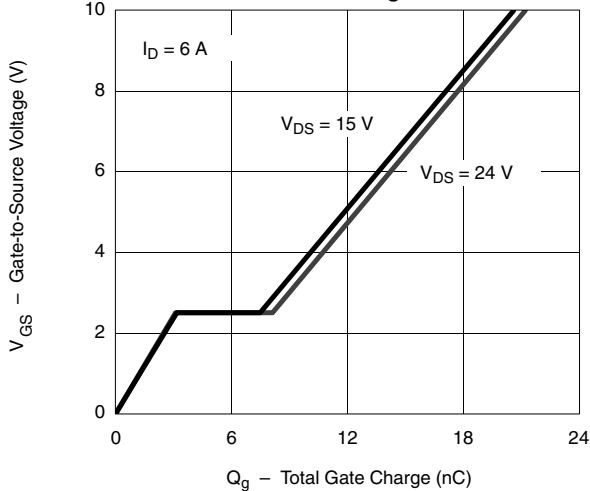
On-Resistance vs. Drain Current and Gate Voltage



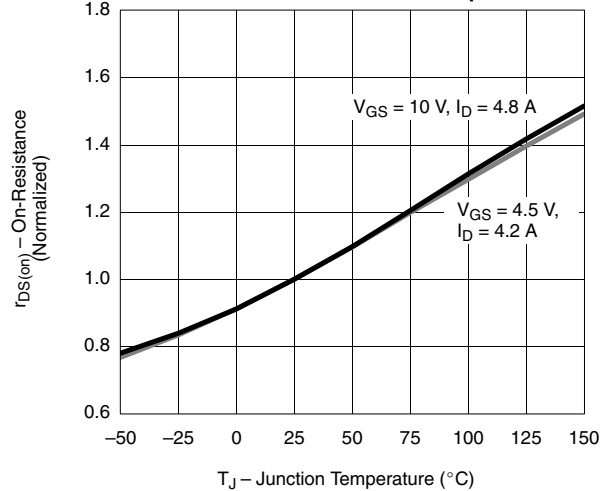
Capacitance



Gate Charge



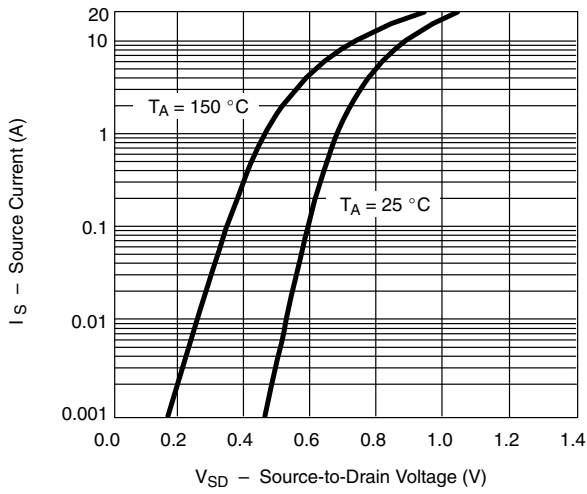
On-Resistance vs. Junction Temperature



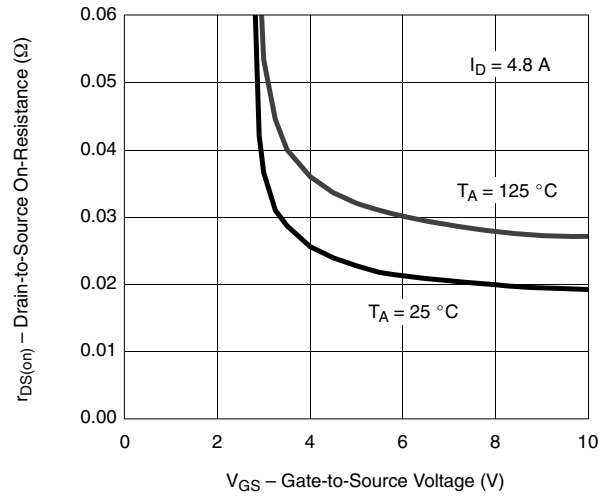


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

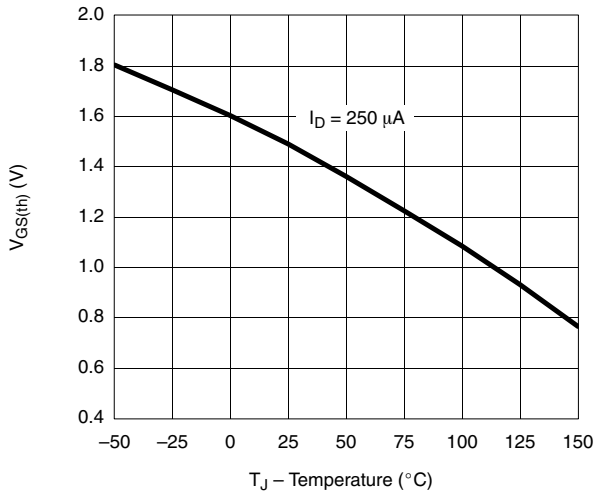
Source-Drain Diode Forward Voltage



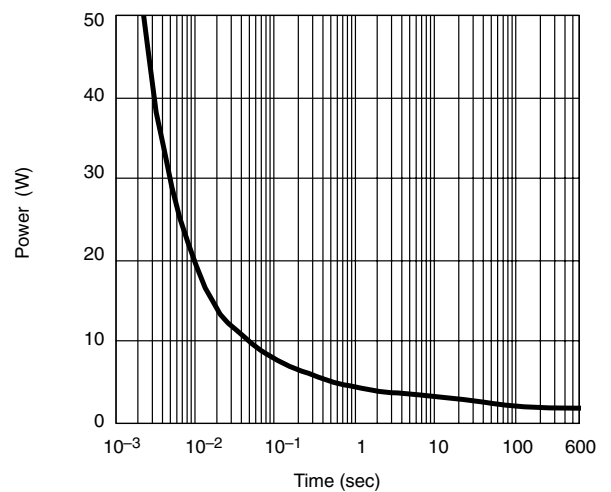
On-Resistance vs. Gate-to-Source Voltage



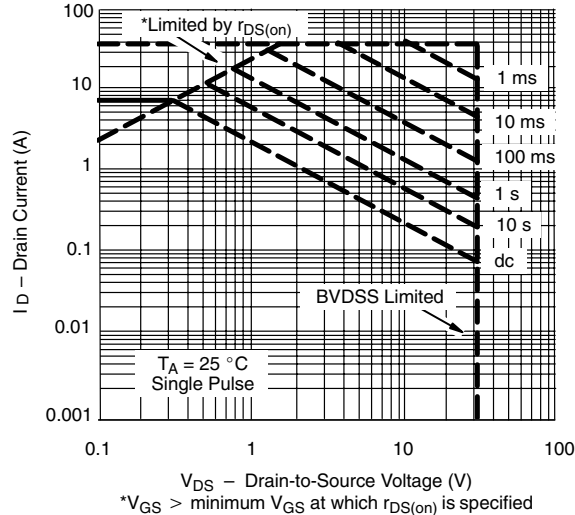
Threshold Voltage



Single Pulse Power

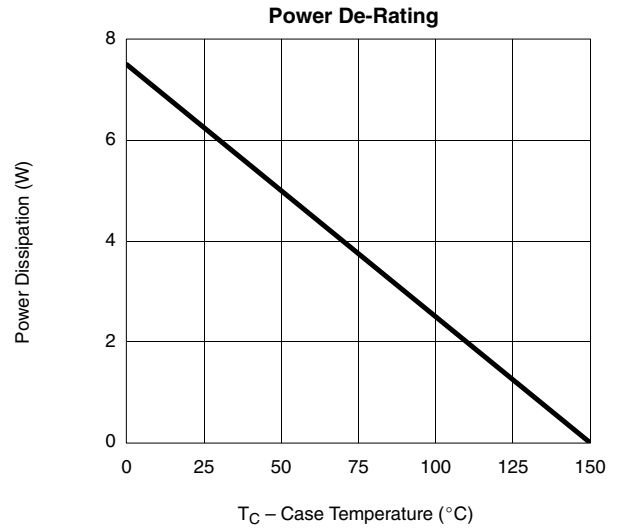
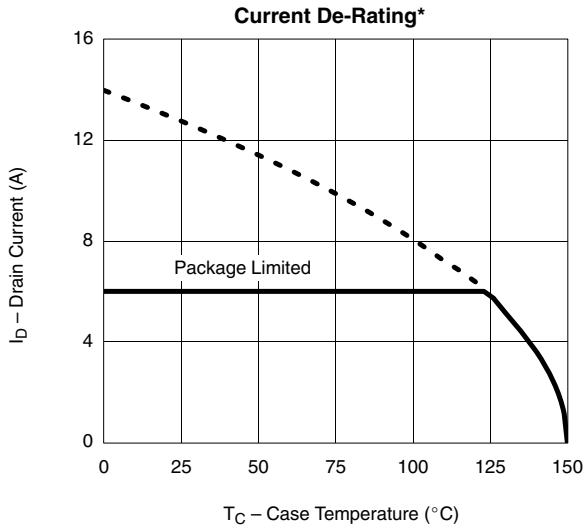


Safe Operating Area, Junction-to-Ambient





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

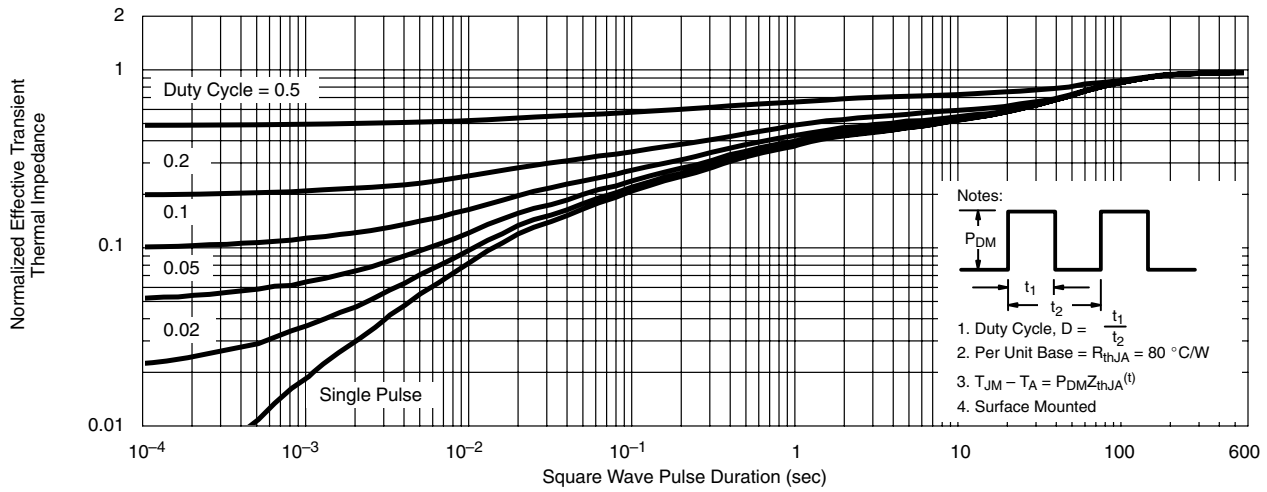


*The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

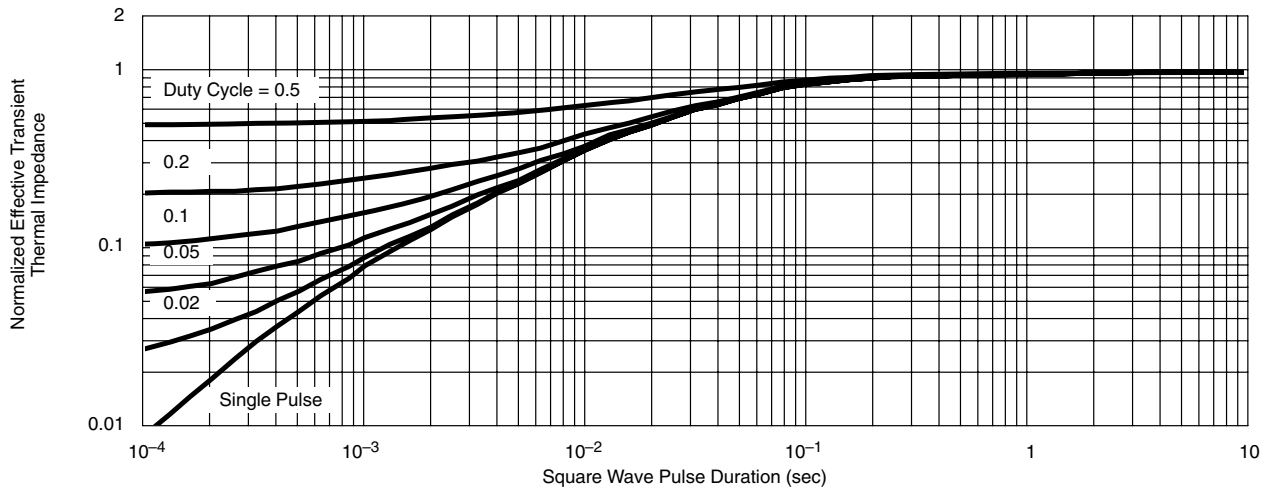


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



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