Structure Silicon monolithic integrated circuit

Product Name Cell Phone Camera, LCD Interface IC

Type **BU1561GV**

Feature Built-in JPEG Codec, SXGA Camera Module Interface, and QCIF+ LCD controller interface

• Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage 1(IO)	VDDIO1	-0.5～+3.5	V
Supply voltage2 (IO)	VDDIO2	-0.5～+3.5	V
Supply voltage3 (CORE)	VDD	-0.5～+2.2	V
Power dissipation	PD	430*1, 970*2	mW
Input voltage 1	VIN1	-0.5～VDDIO1+0.5	V
Input voltage2	VIN2	-0.5～VDDIO2+0.5	V
Storage temperature range	Tstg	-30～+125	°C

*1 IC only. If exceeding 25°C, 4.3mW should be reduced at the rating 1 °C.

*2 When packaging a glass epoxy board of 70*70*1.6mm. If exceeding 25°C, 9.7 mW should be reduced at the rating 1°C.

* Anti radiation design is not provided.

* Operation is not guaranteed.

• Operating conditions (Ta=-20°C～+85°C)

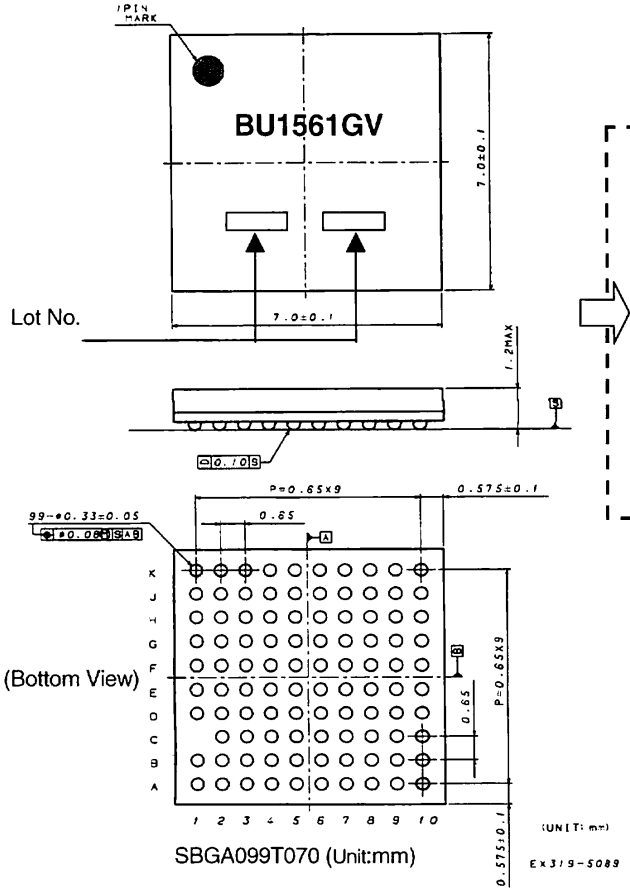
Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage 1(IO)	VDDIO1	1.70	1.80	3.00	V
Supply voltage2 (IO)	VDDIO2	2.70	2.85	3.00	V
Supply voltage3 (CORE)	VDD	1.70	1.80	1.90	V
Input "H" voltage 1	VIH1	0.8*VDDIO	-	VDDIO+0.3	V
Input "L" voltage 1	VIL1	-0.3	-	0.2*VDDIO	V
Input "H" voltage 2	VIH2	0.85*VDDIO	-	VDDIO+0.3	V
Input "L" voltage 2	VIL2	-0.3	-	0.15*VDDIO	V
Input voltage range	VIN-VDDIO1,2	-0.3	-	VDDIO+0.3	V

* Supply power in the order of VDD -> VDDIO1 -> VDDIO2.

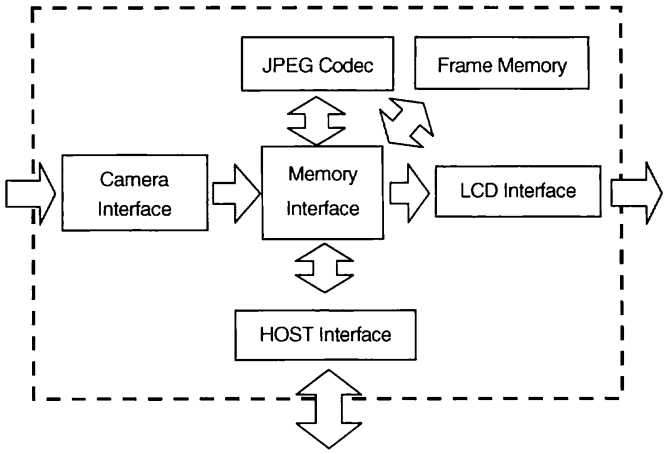
• Electric Characteristics (Unless otherwise specified, VDD=1.80V, VDDIO=2.85V, GND=0.0V, Ta=25°C, F_{PIN}=13.0MHz, F_{SYS}=52.0MHz.(Using PLL))

Parameter	Symbol	Specification			Unit	Conditions
		MIN	TYP	MAX		
Input frequency	F_{IN}	-	-	30.0	MHz	XIN (Duty 50±5%), at PLL OFF
Internal action frequency	F_{SYS}	-	-	52.0	MHz	Internal SCLK frequency
Internal PLL input frequency	F_{PIN}	11.7	-	14.3	MHz	Internal PLL-block input frequency
Action consumption current	IDD	-	23.0	-	mA	At camera ON, LCD display ON At viewer operating
Static consumption current	IDDst	-	-	50	µA	At suspend mode setting
Input "H" current 1	IIH1	-10	-	10	µA	VIH=VDDIO1
Input "H" current 2	IIH2	25	50	100	µA	Pull-down terminal, VIH=VDDIO1
Input "H" current 3	IIH3	-10	-	10	µA	Pull-up terminal, VIH=VDDIO1
Input "L" current 1	IIL1	-10	-	10	µA	VIL=GND
Input "L" current 2	IIL2	-10	-	10	µA	Pull-down terminal, VIL=GND
Input "L" current 3	IIL3	-100	-50	-25	µA	Pull-up terminal, VIL=GND
Input "H" voltage1	VIH1	VDDIO *0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O terminal)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO *0.2	V	Normal input (including input mode of I/O terminal)
Input "H" voltage 2	VIH2	VDDIO *0.85	-	VDDIO +0.3	V	Hysteresis input
Input "L" voltage 2	VIL2	-0.3	-	VDDIO *0.15	V	Hysteresis input
Hysteresis voltage width 1	Vhys1	-	0.6	-	V	Hysteresis input
Hysteresis voltage width 2	Vhys2	-	0.9	-	V	Hysteresis input (XIN)
Output "H" voltage 1	VOH1	VDDIO -0.4	-	VDDIO	V	IOH1=-1.0mA(DC) (Including output mode of I/O terminal)
Output "L" voltage 1	VOL1	0.0	-	0.4	V	IOL1=1.0mA(DC) (Including output mode of I/O terminal)
Output "H" voltage 2	VOH2	VDDIO -0.4	-	VDDIO	V	IOH2=-1.0mA(DC), XOUT terminal

• External Dimensional Drawing and Mark Drawing



• Block Diagram



Rev. B

• Land No. and Pin Name

Land No.	Pin Name	Function
K2	A1	HOST address
J1	A2	
K8	CAMCKI	Camera I/F
K9	CAMCKO	
H5	CAMD0	
G5	CAMD1	
F6	CAMD2	
G6	CAMD3	
J6	CAMD4	
K6	CAMD5	
K7	CAMD6	
J7	CAMD7	
J5	CAMHS	
K5	CAMVS	
J3	CSB	HOST chip select
H1	D0	HOST data bus
G3	D1	
G2	D2	
G1	D3	
F1	D4	
F2	D5	
F3	D6	
F4	D7	
E3	D8/EXGIO0	
E2	D9/EXGIO1	
E1	D10/EXGIO2	
D1	D11/EXGIO3	
D2	D12/EXGIO4	
D3	D13/EXGIO5	
C2	D14/EXGIO6	
B1	D15/EXGIO7	
H6	GIO2/KEY2	GPIO
K4	INT	Interrupt
F7	KEY0	Key I/F
D5	KEY1	
E8	LCDA0	LCD I/F
F9	LCDCS1B	
F8	LCDCS2B	
E10	LCDD0	
D10	LCDD1	
D9	LCDD2	
C10	LCDD3	
C9	LCDD4	
A9	LCDD5	
B8	LCDD6/SCL	
A8	LCDD7/SI	
A7	LCDD8	
A6	LCDD9	
B6	LCDD10	
C6	LCDD11	

Land No.	Pin Name	Function
D6	LCDD12	LCD I/F
C5	LCDD13	
B5	LCDD14	
A5	LCDD15	
E7	LCDRDB	
E6	LCDWRB	
H10	LEDCNT/GIO1	LED control
B4	PWM0/GIO0	PWM output
G8	PWM1/GIO3	
G9	PWM2/GIO4	
G10	PWM3/GIO5	
H4	RDB	HOST read
A4	RESETB	Reset
J10	SDA	Serial I/F
H9	SDC	
C7	TEST	Test
F10	VD/GIO6	VD out
K3	WRB	HOST write
B7	X16_8	Bus type select
A2	XIN	Oscillator
B3	XOUT	
B9	VDD	Core VDD
F5		
J9		
B2	VDDIO1	IO1 VDD
C4		
J2		
E9	VDDIO2	IO2 VDD
H7		
D4	GND	GND
D7		
E4		
G4		
G7		
A1	N.C.	Non Connection
A10		
A3		
B10		
C1		
C3		
C8		
D8		
E5		
H2		
H3		
H8		
J4		
J8		
K1		
K10		

• Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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