Clock generator for digital still camera

BU2385KN

BU2385KN is a clock generator IC that can generate multiple frequencies (clocks) from one oscillator. Excellent jitter characteristic is achieved through the built-in high-performance 3-channel PLL. High-quality sound and image equivalent to the oscillating module are the result of this feature. Clocks can be easily changed for other applications. The internal dividing control allows the frequency to be switched outside.

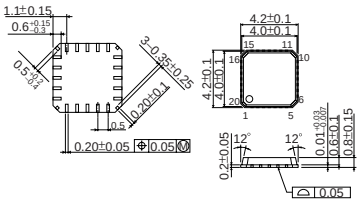
●Applications

Digital still camera

●Features

1) Multiple frequency clock signals can be generated by the built-in 3-channel PLL through connecting crystal oscillator.
2) QFN20V package
3) 3.3V single power supply
4) For crystal 14.318182MHz・28.636363MHz
5) No need additional components.
(BU2385KN have PLL loop filter in side).

●External dimensions (Unit : mm)



QFN20V

●Absolute maximum ratings (Ta=25°C)

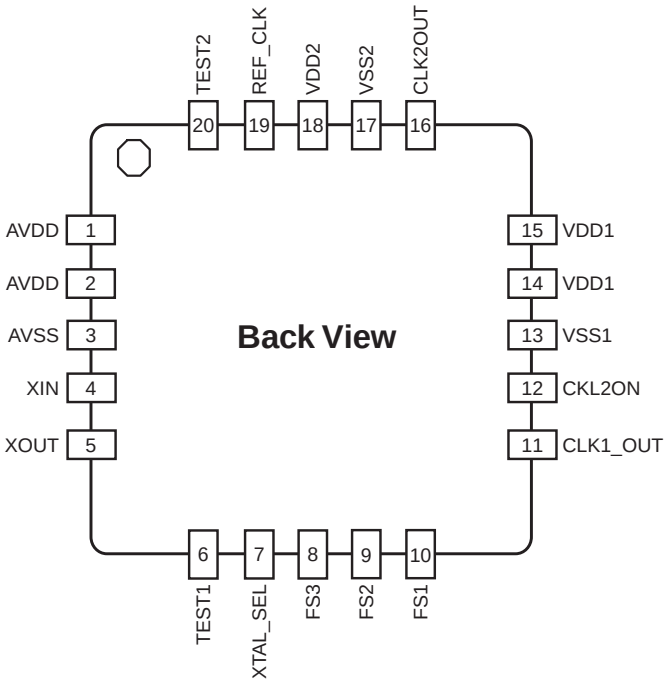
Parameter	Symbol	Limits	Unit
Applied voltage	VDD	−0.5 to +7.0	V
Input voltage	VIN	−0.3 to V_{DD}+0.3	V
Storage temperature range	Tstg	−30 to +125	℃
Power dissipation	Pd	530	mW

∗ An operation is not guaranteed.
∗ In case it is used at Ta=25℃ or more, 5.3mW is reduced at every 1℃.
∗ Radiation resistance design is not used.
∗ Power dissipation is measured when BU2385KN is placed in the board.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.0	–	3.6	V
Input H voltage range	V_{IH}	0.8V_{DD}	–	V_{DD}	V
Input L voltage range	V_{IL}	0.0	–	0.2V_{DD}	V
Operation temperature range	Topr	−5	–	+70	℃
Output maximum load	C_L	–	–	15	pF

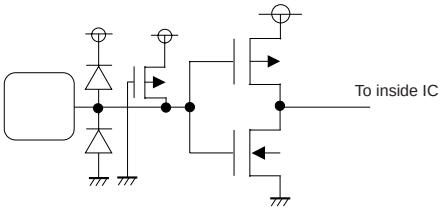
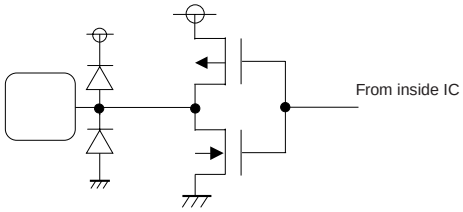
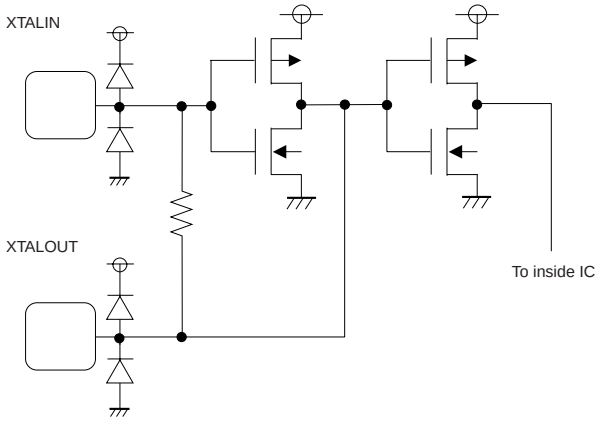
●**Block diagram**



●**Explanation for terminal function**

PIN No.	PIN NAME	Function
1	AVDD	Analog VDD
2	AVDD	Analog VDD
3	AVSS	Analog GND
4	XIN	Standard crystal input
5	XOUT	Standard crystal output
6	TEST 1	Input for test mode (normally open) with pull–down
7	XTAL_SEL	Crystal select with pull up H : 28.636363MHz L : 14.318182MHz
8	FS3	CLK1,2 output select with pull up
9	FS2	CLK1,2 output select with pull up
10	FS1	REFCLK output select with pull up
11	CLK1OUT	71.877274M / 90.314686M / 96.016044M / 114.54546M clock output
12	CLK2ON	CLK2 output control with pull up H : enable L : disable
13	VSS 1	GND for CLK 1, 2 clock output and Logic circuit
14	VDD 1	VDD for CLK 1, 2,clock output and Logic circuit
15	VDD 1	VDD for CLK 1, 2,clock output and Logic circuit
16	CLK2OUT	96.016044M / 48.008022M clock output
17	VSS 2	REF_CLK GND
18	VDD 2	REF_CLK VDD
19	REF_CLK	14.318182M / 17.734450M clock output
20	TEST2	Input for test mode (normally open) with pull–down

●PIN Input / Output equivalent circuit

PIN No.	Equival circuit
Input PIN 7, 8, 9, 10, 12 with pull–up (6 : TEST1, 20 : TEST2 with pull down)	
Output PIN 11, 16, 19	
Crystal PIN 4, 5	

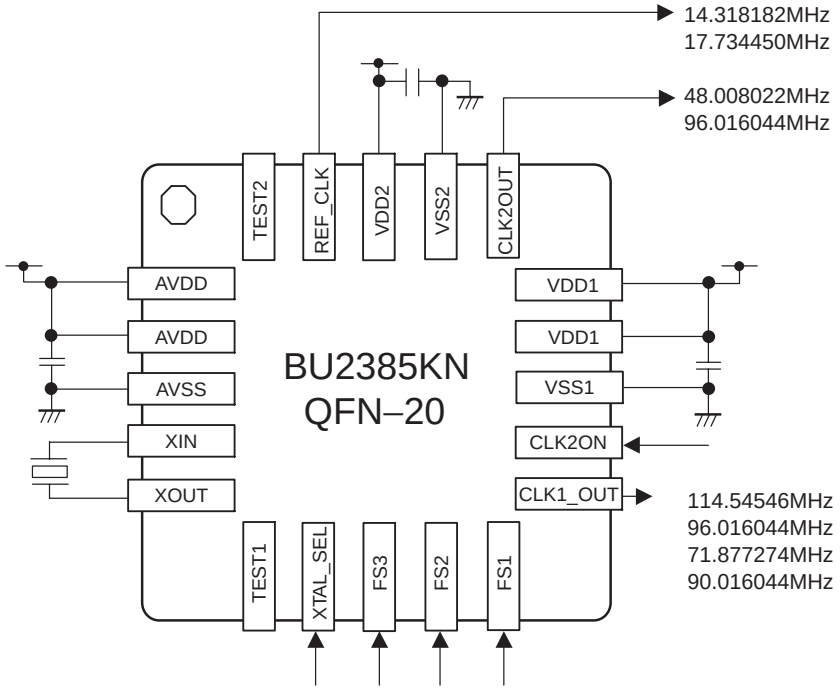
●**Electrical characteristics** (Unless otherwise noted, Ta=25°C, V_{CC}=3.3V)

While crystal shows 28.636363MHz, XTAL_SEL=H, in case of 14.31818MHz, TXAL_SEL=L

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	IDD	–	40	50	mA	No load
output frequency						
CLK1 FS2:H FS3:H	Fclk1-1	–	96.016044	–		Xtal ∗ (228/17)/2
FS2:H FS3:L	Fclk1-2	–	71.877274	–		Xtal ∗ (251/25)/2
FS2:L FS3:L	Fclk1-3	–	114.54546	–	MHz	Xtal ∗ (224/14)/2
FS2:L FS3:H	Fclk1-4	–	90.314686	–	MHz	Xtal ∗ (164/13)/2
CLK2 FS2:L FS3:L	Fclk2-1	–	96.016044	–	MHz	Xtal ∗ (228/17)/2
FS2,3:HL LH HH	Fclk2-2	–	48.008022	–	MHz	Xtal ∗ (228/17)/4
REFCLK FS1:H	Fref1-1	–	14.318182	–	MHz	Crystal direct output
FS1:L	Fref1-2	–	17.734450	–	MHz	Xtal ∗ (706/57)/10
Duty1 at under 100MHz	Duty1	45	50	55	%	Measured at 1/2VDD
Duty2 at upper 100MHz	Duty2	–	50	–	%	Measured at 1/2VDD
Rise time	Tr	–	2.5	–	nsec	Time between 0.2VDD and 0.8VDD
Fall time	Tf	–	2.5	–	nsec	Time between 0.2VDD and 0.8VDD
Period Jitter 1σ	P-J1σ	–	30	–	psec	∗1
Period Jitter MIN-MAX	P-J MINMAX	–	180	–	psec	∗2
Output Lock time	Tlock	–	–	1	msec	∗3

Note) When input frequency is 14.31818MHz, output frequency is above rated value.
∗1 Period Jitter 1σ : This value is the standard deviation of an output period when using Time Interval Analyzer with 10,000 sampling.
∗2 Period Jitter MIN-MAX : This value is the max range of an output period when using Time Interval Analyzer with 10,000 sampling.
∗3 Output Lock time : Time between voltage supply leads to 3.0V and output clock gets stable.

●**Application circuit**



Note) BU2385KN is placed on the board normally.
A decoupling capacitor (0.1µF) needs to be placed between Pin1,2 and Pin3, Pin13 and Pin14,15, Pin17 and Pin18.
The decoupling capacitor is as close to the above pins as possible.

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