March 2003
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# FIN1049
# LVDS Dual Line Driver with Dual Line Receiver

## General Description

This dual Driver-Receiver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The Driver accepts LVTTL inputs and translates them to LVDS outputs. The Receiver accepts LVDS inputs and translates them to LVTTL outputs. The LVDS levels have a typical differential output swing of 350mV which provide for low EMI at ultra low power dissipation even at high frequencies. The FIN1049 can accept LVPECL inputs for translating from LVPECL to LVDS. The En and Enb inputs are ANDed together to enable/disable the outputs. The enables are common to all four outputs. A single line driver and single line receiver function is also available in the FIN1019.

## Features

- Greater than 400 Mbps data rate
- 3.3V power supply operation
- Low power dissipation
- Fail safe protection for open-circuit conditions
- Meets or exceeds the TIA/EIA-644-A LVDS standard
- 16-pin TSSOP package saves space
- Flow-through pinout simplifies PCB layout
- Enable/Disable for all outputs
- Industrial operating temperature range: –40°C to +85°C

## Ordering Code:

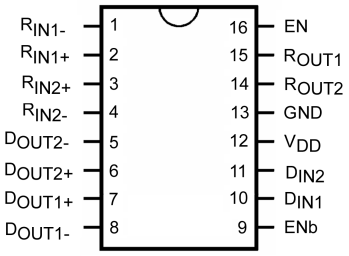
| Order Number | Package Number | Package Description |
|---|---|---|
| FIN1049MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## Pin Descriptions

| Pin Name | Description |
|---|---|
| $R_{IN1+}$, $R_{IN2+}$ | Non-Inverting LVDS Inputs |
| $R_{IN1-}$, $R_{IN2-}$ | Inverting LVDS Inputs |
| $D_{OUT1+}$, $D_{OUT2+}$ | Non-Inverting Driver Outputs |
| $D_{OUT1-}$, $D_{OUT2-}$ | Inverting Driver Outputs |
| EN, ENb | Driver Enable Pins for All Outputs |
| $R_{OUT1}$, $R_{OUT2}$ | LVTTL Output Pins for $R_{OUT1}$ and $R_{OUT2}$ |
| $D_{IN2}$, $D_{IN2}$ | LVTTL Input Pins for $D_{IN1}$ and $D_{IN2}$ |
| $V_{CC}$ | Power Supply (3.3V) |
| GND | Ground |

## Connection Diagram



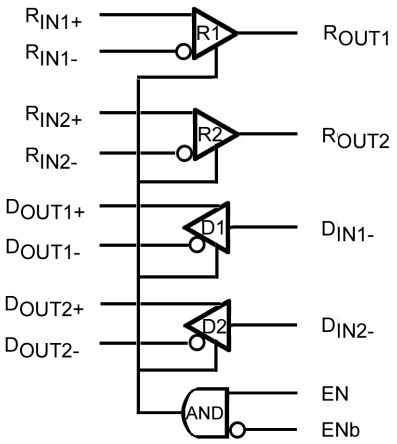
## Function Table

| Inputs | | Outputs (LVTTL) | | Inputs (LVDS) (Note 1) | | Outputs (LVDS) | |
|---|---|---|---|---|---|---|---|
| **EN** | **ENb** | $R_{OUT1}$ | $R_{OUT2}$ | $R_{IN\#+}$ | $R_{IN\#-}$ | $D_{OUT\#+}$ | $D_{OUT\#-}$ |
| H | L | ON | ON | | | ON | ON |
| H | H | Z | Z | | | Z | Z |
| L | H | Z | Z | | | Z | Z |
| L | L | Z | Z | | | Z | Z |
| H | L | H | H | Open Current Fail Safe Condition | | | |

H = HIGH Logic Level
L = LOW Logic Level or OPEN
X = Don't Care
Z = High Impedance

**Note 1:** Any unused Receiver Inputs should be left Open.

## Functional Diagram



## Absolute Maximum Ratings(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | –0.5V to +4.6V |
| LVDS DC Input Voltage ($V_{IN}$) | –0.5V to +4.6V |
| LVDS DC Output Voltage ($V_{OUT}$) | –0.5V to +4.6V |
| Driver Short Circuit Current ($I_{OSD}$) | Continuous 10mA |
| Storage Temperature Range ($T_{STG}$) | –65°C to +150°C |
| Max Junction Temperature ($T_J$) | 150°C |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |
| ESD (Human Body Model) | >7000V |
| ESD (Machine Model) | >250V |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 3.0V to 3.6V |
| Magnitude of Differential Voltage ($\|V_{ID}\|$) | 100mV to $V_{CC}$ |
| Operating Temperature ($T_A$) | –40°C to +85°C |

**Note 2:** The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

## DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ (Note 3) | Max | Units |
|---|---|---|---|---|---|---|
| LVDS Input DC Specifications ($R_{IN1+}$, $R_{IN1-}$, $R_{IN2+}$, $R_{IN2-}$) See Figure 1 and Table 1 | | | | | | |
| $V_{TH}$ | Differential Input Threshold HIGH | VCM = 1.2V, 0.05V, 2.35V | | 0.0 | 35.0 | mV |
| $V_{TL}$ | Differential Input Threshold LOW | | –100 | 0.0 | | mV |
| $V_{IC}$ | Common Mode Voltage Range | $V_{ID}$ = 100mV, $V_{CC}$ = 3.3V | $V_{ID}/2$ | | $V_{CC} - (V_{ID}/2)$ | V |
| $I_{IN}$ | Input Current | $V_{CC}$ = 0V or 3.6V, $V_{IN}$ = 0V or 2.8V | | | ±20.0 | mA |
| **CMOS/ LVTTL Input DC Specifications (EN, ENb, $D_{IN1}$, $D_{IN2}$)** | | | | | | |
| $V_{IH}$ | Input High Voltage (LVTTL) | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage (LVTTL) | | GND | | 0.8 | V |
| $I_{IN}$ | Input Current (EN, ENb, $D_{IN1}$, $D_{IN2}$, $R_{INx+}$, and $R_{INx-}$) | $V_{IN}$ = 0V or $V_{CC}$ | | | ±20.0 | µA |
| $V_{IK}$ | Input Clamp Voltage | $V_{IK}$ = –18mA | –1.5 | –0.7 | | V |
| **LVDS Output DC Specifications ($D_{OUT1+}$, $D_{OUT1-}$, $D_{OUT2+}$, $D_{OUT2-}$)** | | | | | | |
| $V_{OD}$ | Output Differential Voltage | $R_L$ = 100Ω, Driver Enabled, See Figure 2 | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change from Differential LOW-to-HIGH | | | | 35.0 | mV |
| $V_{OS}$ | Offset Voltage | | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Offset Magnitude Change from Differential LOW-to-HIGH | | | | 25.0 | mV |
| $I_{OS}$ | Short Circuit Output Current | $D_{OUT+}$ = 0V & $D_{OUT-}$ = 0V, Driver Enabled | | | –9.0 | mA |
| $I_{OSD}$ | | $V_{OD}$ = 0V, Driver Enabled | | | –9.0 | mA |
| $I_{OFF}$ | Power-Off Input or Output Current | $V_{CC}$ = 0V, $V_{OUT}$ = 0V or $V_{CC}$ | | | ±20.0 | µA |
| $I_{OZD}$ | Disabled Output Leakage Current | Driver Disabled, $D_{OUT+}$ = 0V or $V_{CC}$ or $D_{OUT-}$ = 0V or $V_{CC}$ | | | ±10.0 | µA |
| **CMOS/LVTTL Output DC Specifications ($R_{OUT1}$, $R_{OUT2}$)** | | | | | | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –2mA, $V_{ID}$ = 200mV | 2.7 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2mA, $V_{ID}$ = 200mV | | | 0.250 | V |
| $I_{OZ}$ | Disabled Output Leakage Current | Driver Disabled, $R_{OUTn}$ = 0V or $V_{CC}$ | | | ±10.0 | µA |
| $I_{CC}$ | Power Supply Current (Note 4) | Drivers Enabled, Any Valid Input Condition | | | 25.0 | mA |
| $I_{CCZ}$ | Power Supply Current | Drivers Disabled | | | 10.0 | mA |
| $C_{IND}$ | Input Capacitance | LVDS Input | | 3.0 | | pF |
| $C_{OUT}$ | Output Capacitance | LVDS Output | | 4.0 | | pF |
| $C_{INT}$ | Input Capacitance | LVTTL Input | | 3.5 | | pF |

**Note 3:** All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3V.

**Note 4:** Both driver and receiver inputs are static. All LVDS outputs have 100Ω load. None of the outputs have any lumped capacitive load.

## AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ (Note 5) | Max | Units |
|---|---|---|---|---|---|---|
| **Switching Characteristics - LVDS Outputs** | | | | | | |
| $t_{PLHD}$ | Differential Propagation Delay LOW-to-HIGH | See Figures 3, 4 | | | 2.0 | ns |
| $t_{PHLD}$ | Differential Propagation Delay HIGH-to-LOW | | | | 2.0 | ns |
| $t_{TLHD}$ | Differential Output Rise Time (20% to 80%) | | 0.2 | | 1.0 | ns |
| $t_{THLD}$ | Differential Output Fall Time (80% to 20%) | | 0.2 | | 1.0 | ns |
| $t_{SK(P)}$ | Pulse Skew $\lvert t_{PLH} - t_{PHL} \rvert$ | | | | 0.35 | ns |
| $t_{SK(LH)}$, $t_{SK(HL)}$ | Channel-to-Channel Skew (Note 6) | | | | 0.35 | ns |
| $t_{SK(PP)}$ | Part-to-Part Skew (Note 7) | | | | 1.0 | ns |
| $t_{PZHD}$ | Differential Output Enable Time from Z-to-HIGH | See Figures 5, 6 | | | 6.0 | ns |
| $t_{PZLD}$ | Differential Output Enable Time from A-to-LOW | | | | 6.0 | ns |
| $t_{PHZD}$ | Differential Output Disable Time from HIGH-to-Z | | | | 3.0 | ns |
| $t_{PLZD}$ | Differential Output Disable Time from LOW-to-Z | | | | 3.0 | ns |
| $f_{MAXD}$ | Maximum Frequency (Note 8) | See Figure 3 | 200 | | | MHz |
| **Switching Characteristics - LVTTL Outputs** | | | | | | |
| $t_{PHL}$ | Propagation Delay HIGH-to-LOW | Measured from 20% to 80% signal | 0.5 | 1.0 | 3.5 | ns |
| $t_{PLH}$ | Propagation Delay LOW-to-HIGH | $V_{ID}$ = 200mV; | 0.5 | 1.0 | 3.5 | ns |
| $t_{SK1}$ | Pulse Skew | Distributed Load | 0.0 | 35.0 | 400 | ps |
| $t_{SK2}$ | Channel-to-Channel Skew | $C_L$ = 15pF and 50Ω; | 0.0 | 50.0 | 500 | ps |
| $t_{SK3}$ | Part-to-Part Skew | $R_L$ = 1KΩ; | 0.0 | | 1.0 | ns |
| $t_{LHR}$ | Transition Time LOW-to-HIGH | $V_{OS}$ = 1.2V; | 0.1 | 0.25 | 1.4 | ns |
| $t_{HLR}$ | Transition Time HIGH-to-LOW | See Figures 7, 8 | 0.1 | 0.18 | 1.4 | ns |
| $t_{PHZ}$ | Disable Time HIGH-to-Z | See Figures 9, 10 | 2.2 | 4.5 | 8.0 | ns |
| $t_{PLZ}$ | Disable Time LOW-to-Z | | 1.3 | 3.5 | 8.0 | ns |
| $t_{PZH}$ | Enable Time Z-to-HIGH | | 1.8 | 3.0 | 7.0 | ns |
| $t_{PZL}$ | Enable Time Z-to-LOW | | 0.9 | 1.4 | 7.0 | ns |
| $f_{MAXT}$ | Maximum Frequency (Note 9) | See Figure 7 | 200 | | | MHz |

**Note 5:** All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3V.

**Note 6:** $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

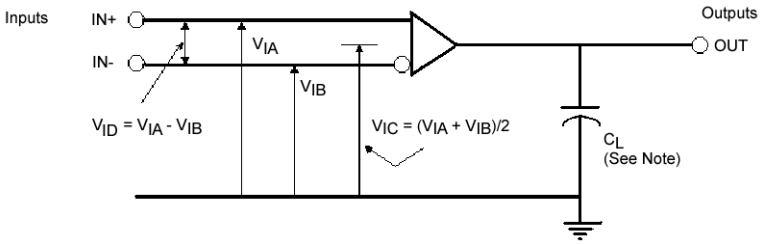
**Note 7:** $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

**Note 8:** $f_{MAX}$ generator input conditions: $t_r = t_f < 1$ns (10% to 90%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45% / 55%, $V_{OD} > 250$mV, all channels switch.

**Note 9:** $f_{MAXT}$ generator input conditions: $t_r = t_f < 1$ns (10% to 90%), 50% duty cycle, $V_{ID}$ = 200mV, $V_{CM}$ = 1.2V. Output criteria: duty cycle = 45% / 55%, $V_{OH} > 2.7$V. $V_{OL} < 0.25$V, all channels switching.

## Required Specifications

1. Human Body Model ESD and Machine Model ESD should be measured using MIL-STD-883C method 3015.7 standard.
2. Latch-up immunity should be tested to the EIA/JEDEC Standard Number 78 (EIA/JESD78).

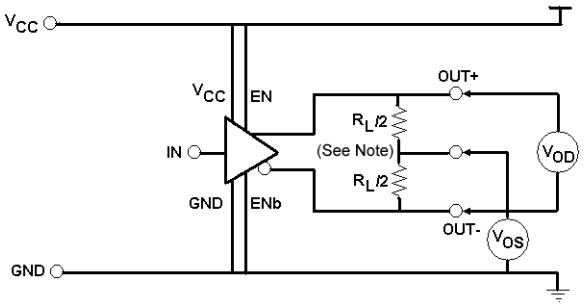



Note: $C_L$ = 15pF, includes all probe and jig capacitances

**FIGURE 1. Differential Receiver Voltage Definitions Test Circuit**

**TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages**

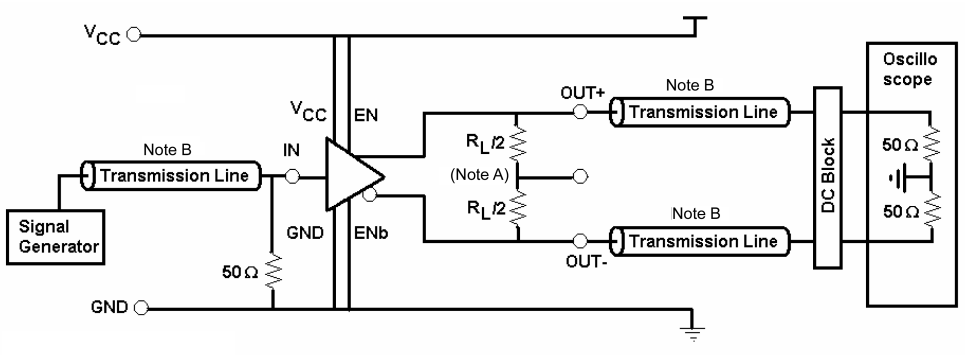
| Applied Voltages (V) | | Resulting Differential Input Voltage (mV) | Resulting Common Mode Input Voltage (V) |
|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ |
| 1.25 | 1.15 | 100 | 1.2 |
| 1.15 | 1.25 | –100 | 1.2 |
| $V_{CC}$ | $V_{CC}$ - 0.1 | 100 | $V_{CC}$ - 0.05 |
| $V_{CC}$ - 0.1 | $V_{CC}$ | –100 | $V_{CC}$ - 0.05 |
| 0.1 | 0.0 | 100 | 0.05 |
| 0.0 | 0.1 | –100 | 0.05 |
| 1.75 | 0.65 | 1100 | 1.2 |
| 0.65 | 1.75 | –1100 | 1.2 |
| $V_{CC}$ | $V_{CC}$ - 1.1 | 1100 | $V_{CC}$ - 0.55 |
| $V_{CC}$ - 1.1 | $V_{CC}$ | –1100 | $V_{CC}$ - 0.55 |
| 1.1 | 0.0 | 1100 | 0.55 |
| 0.0 | 1.1 | –1100 | 0.55 |




Note: $R_L$ = 100Ω

**FIGURE 2. LVDS Output Circuit for DC Test**

## Required Specifications (Continued)




Note A: $R_L = 100\Omega$

Note B: $Z_O = 50\Omega$ and $C_T = 15$ pF Distributed

**FIGURE 3. LVDS Output Propagation Delay and Transition Time Test Circuit**

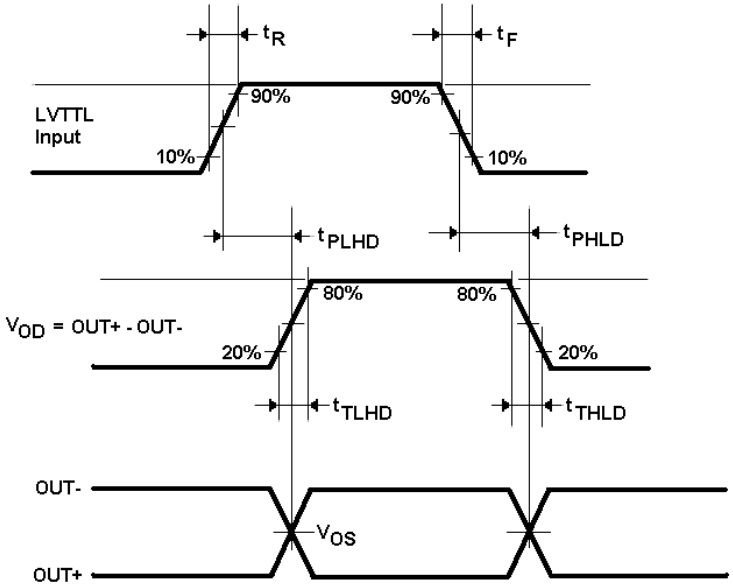
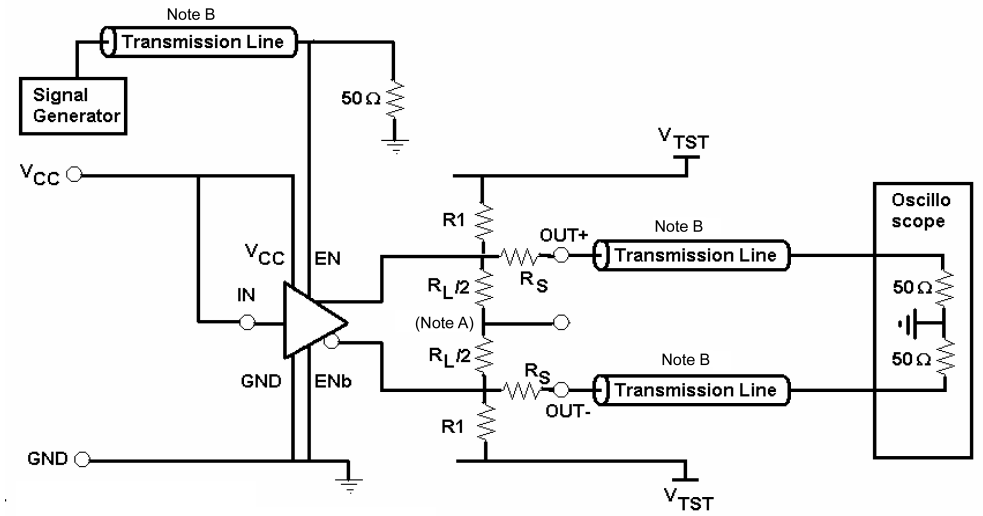



**FIGURE 4. LVTTL Input to LVDS Output AC Waveform**

## Required Specifications (Continued)




Note A: $R_L = 100\Omega$

Note B: $Z_O = 50\Omega$ and $C_T = 15$ pF Distributed

Note: R1 = 1000Ω, $R_S = 950\Omega$

Note: $V_{TST} = 2.4V$

**FIGURE 5. LVDS Output Enable / Disable Delay Test Circuit**

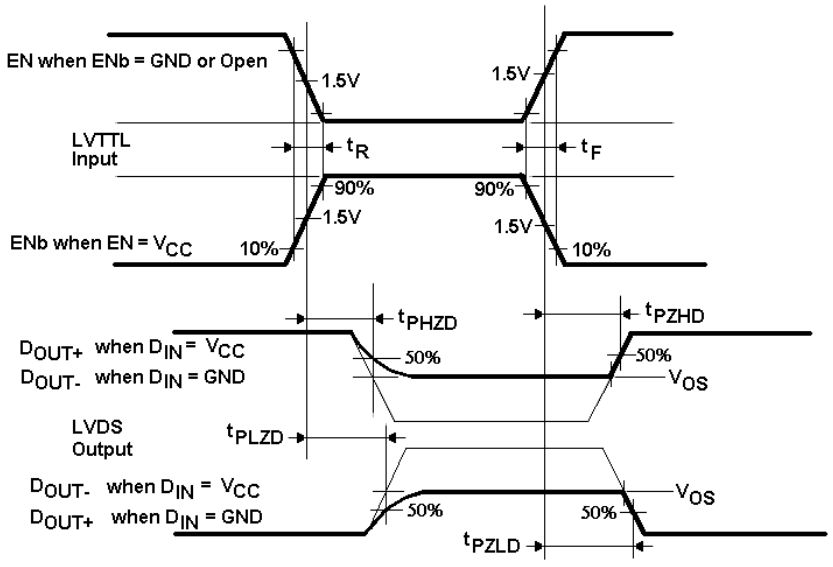
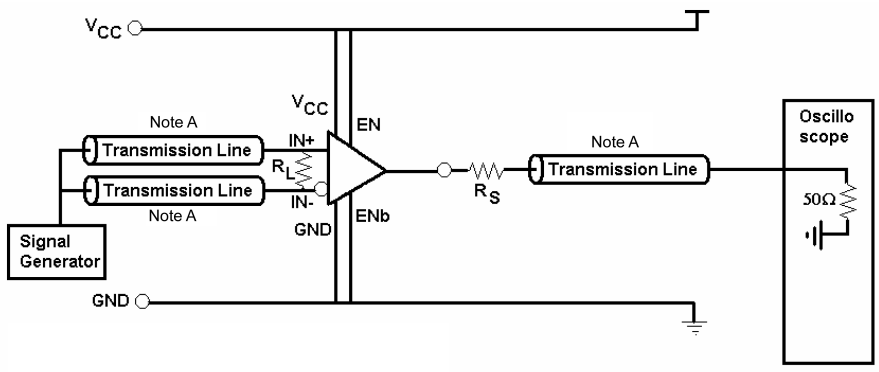



**FIGURE 6. LVDS Output Enable / Disable Timing Waveforms**

## Required Specifications (Continued)




Note A: $Z_O = 50\Omega$ and $C_T = 15$ pF Distributed

Note: $R_L = 100\Omega$ and $R_S = 950\Omega$

**FIGURE 7. LVTTL Output Propagation Delay and Transition Time Test Circuit**

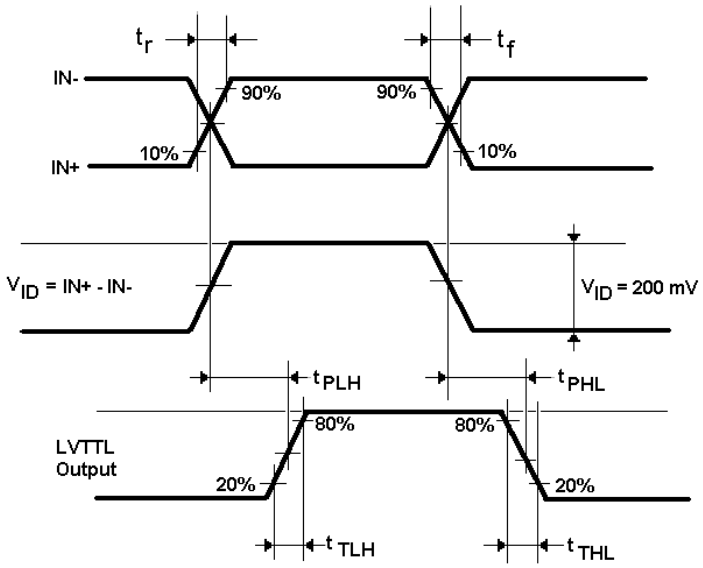
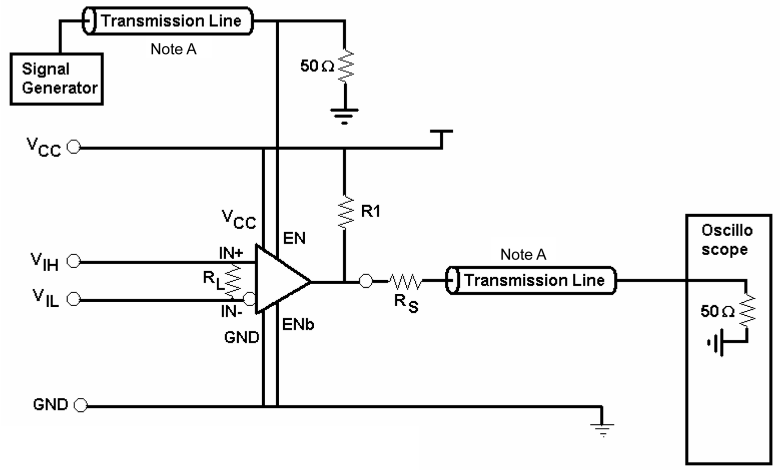



**FIGURE 8. LVDS Input to LVTTL Output Propagation Delay and Transition Time Waveforms**

## Required Specifications (Continued)




Note A: $Z_O = 50\Omega$ and $C_T = 15$ pF Distributed

Note: $R_L = 100\Omega$, R1 = 1000Ω, and $R_S = 950\Omega$

**FIGURE 9. LVTTL Output Enable / Disable Test Circuit**

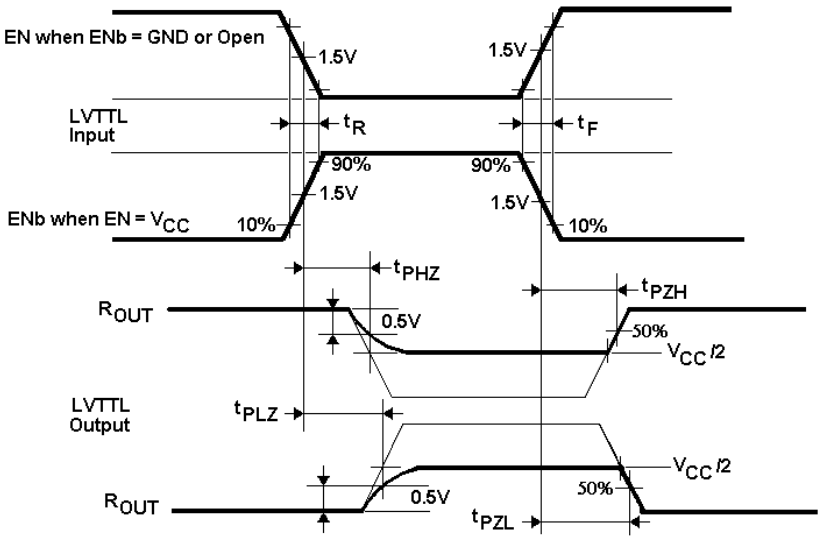
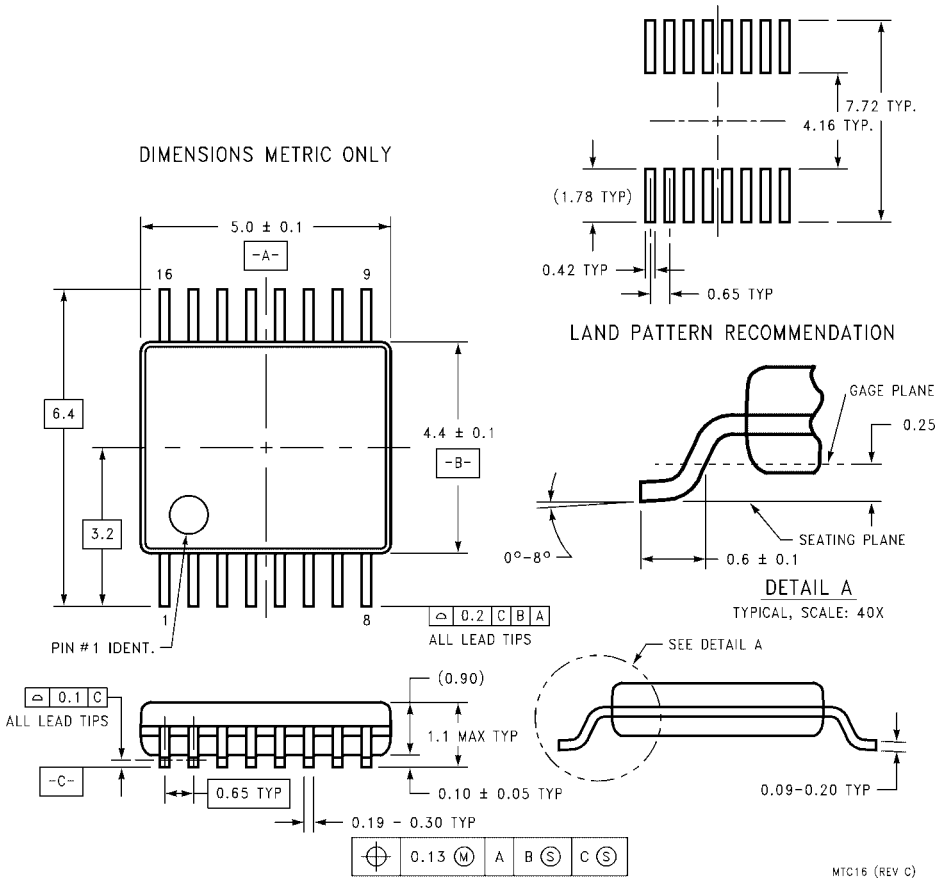



**FIGURE 10. LVTTL Output Enable / Disable Timing Waveforms**

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**



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