

Bi-Directional P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V _{S1S2} (V)	r _{S1S2(on)} (Ω)	I _{S1S2} (A)
-20	0.060 @ V _{GS} = -4.5 V	-4.4
	0.080 @ V _{GS} = -2.5 V	-3.9
	0.105 @ V _{GS} = -1.8 V	-3.4

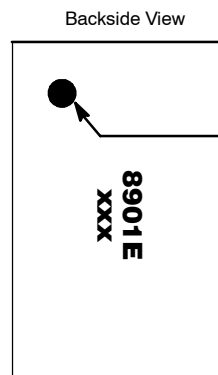
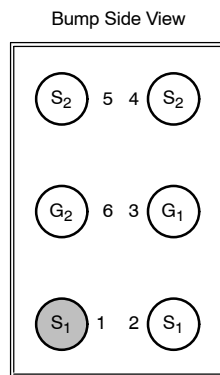
FEATURES

- TrenchFET® Power MOSFET
- Ultra-Low r_{SS(on)}
- ESD Protected: 6000 V
- New MICRO FOOT® Chipscale Packaging Reduces Footprint Area, Profile (0.65 mm) and On-Resistance Per Footprint Area

APPLICATIONS

- Smart Batteries for Portable Devices

MICRO FOOT

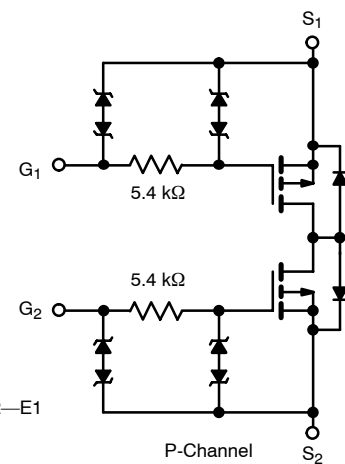


Pin 1 Identifier

Device Marking:

8901E = P/N Code
xxx = Date/Lot Traceability Code

Ordering Information: Si8901EDB-T2—E1



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Source1—Source2 Voltage	V _{S1S2}	-20		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Source1—Source2 Current (T _J = 150 °C) ^a	I _{S1S2}	T _A = 25 °C	-4.4	-3.5	A
		T _A = 85 °C	-3.2	-2.5	
Pulsed Source1—Source2 Current	I _{SM}	-10			
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	1.7	1	W
		T _A = 85 °C	0.8	0.5	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150			
Package Reflow Conditions ^c	VPR	215		°C	
	IR/Convection	220			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 5 sec	60	75	°C/W
		Steady State	95	120	
Maximum Junction-to-Foot ^b	R _{thJF}	18	22		

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- The Foot is defined as the top surface of the package.
- Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

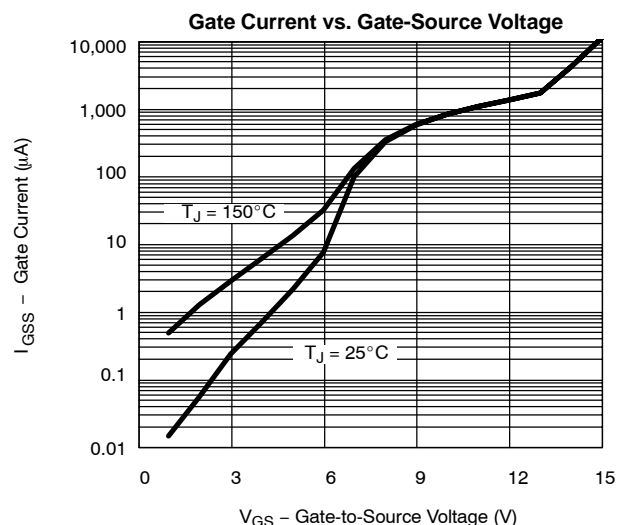
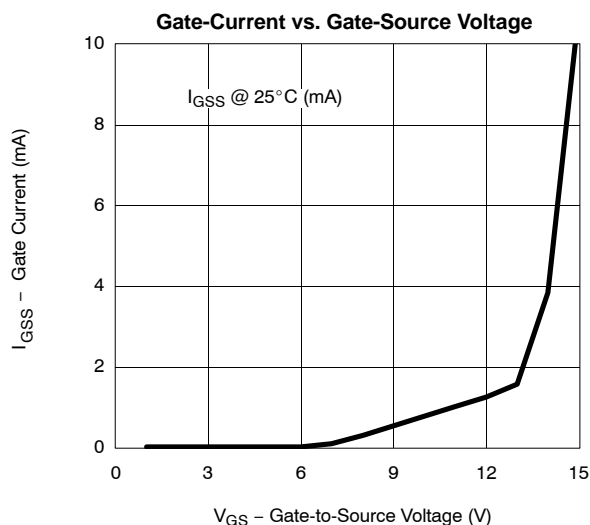
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{SS} = V _{GS} , I _D = -350 μA	-0.45		-1.0	V
Gate-Body Leakage	I _{GSS}	V _{SS} = 0 V, V _{GS} = ±4.5 V			±4	μA
		V _{SS} = 0 V, V _{GS} = ±12 V			±10	mA
Zero Gate Voltage Source Current	I _{S1S2}	V _{SS} = -20 V, V _{GS} = 0 V			-1	μA
		V _{SS} = -20 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Source Current ^a	I _{S(on)}	V _{SS} = -5 V, V _{GS} = -4.5 V	-5			A
Source1—Source2 On-State Resistance ^a	r _{S1S2(on)}	V _{GS} = -4.5 V, I _{SS} = -1 A		0.048	0.060	Ω
		V _{GS} = -2.5 V, I _{SS} = -1 A		0.062	0.080	
		V _{GS} = -1.8 V, I _{SS} = -1 A		0.081	0.105	
Forward Transconductance ^a	g _{fs}	V _{SS} = -10 V, I _{SS} = -1 A		7		S
Dynamic^b						
Turn-On Delay Time	t _{d(on)}	V _{SS} = -10 V, R _L = 10 Ω I _{SS} ≅ -1 A, V _{GEN} = -4.5 V, R _g = 6 Ω		2.3	3.5	μs
Rise Time	t _r			2.2	3.5	
Turn-Off Delay Time	t _{d(off)}			1.3	2	
Fall Time	t _f			9	14	

Notes

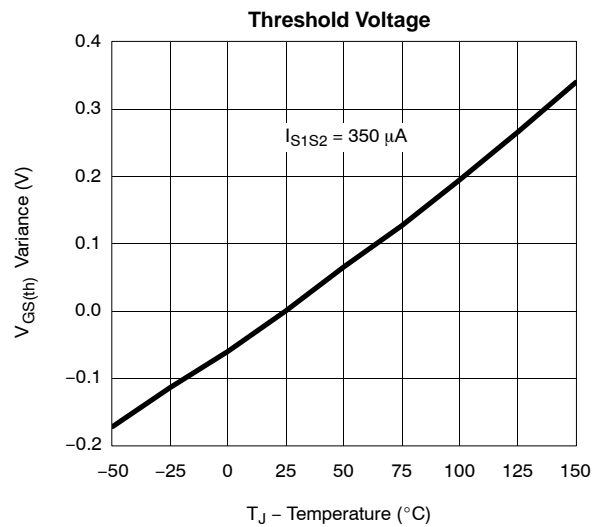
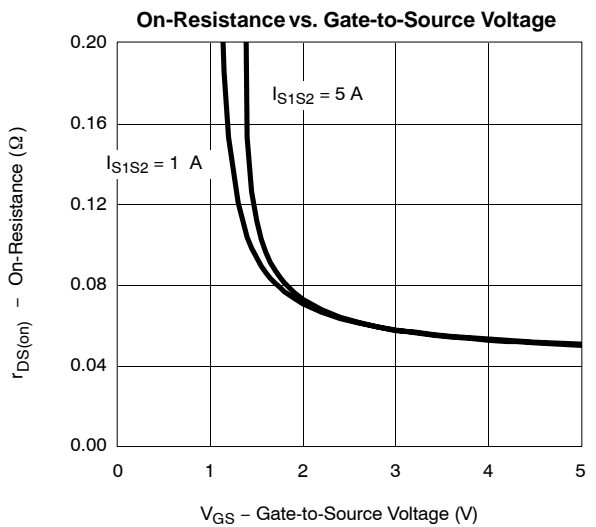
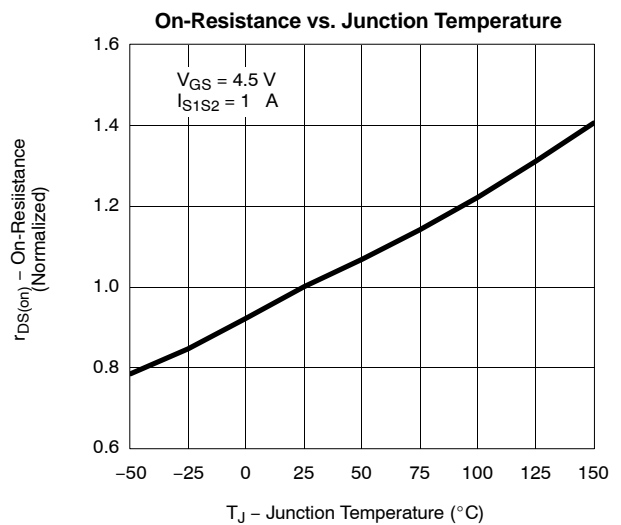
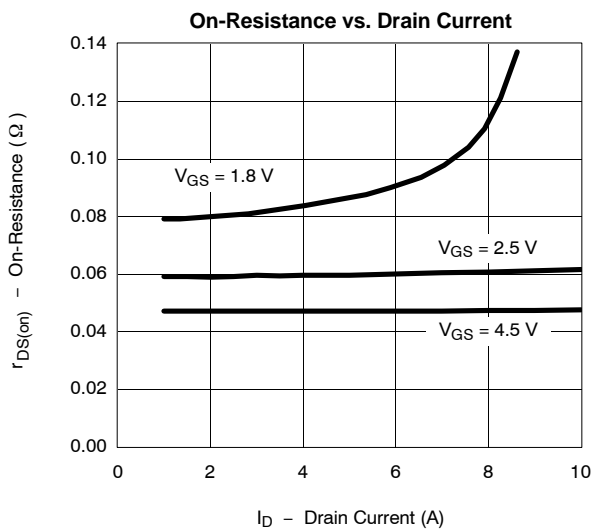
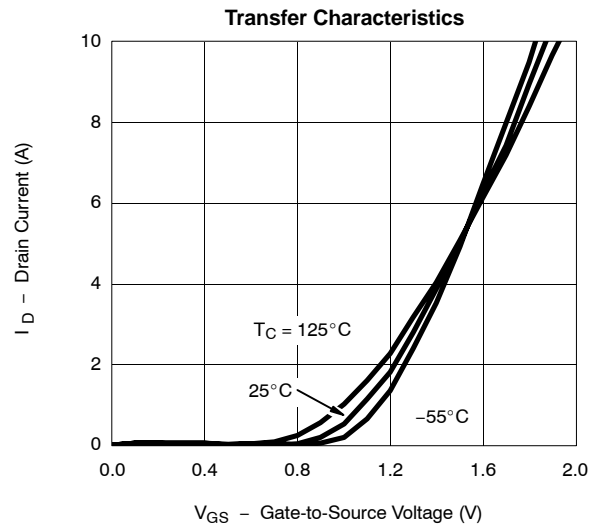
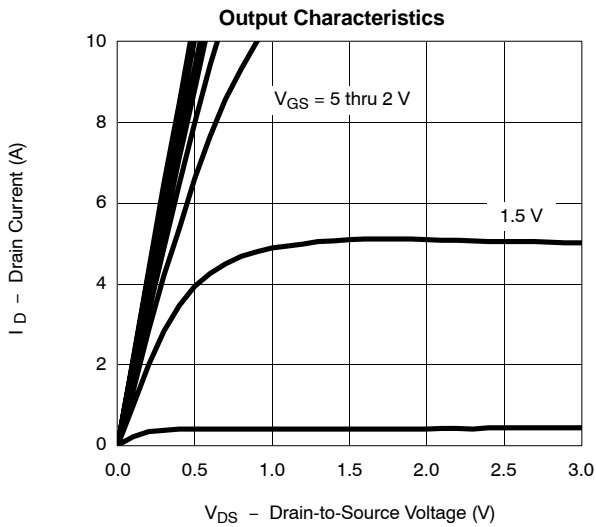
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

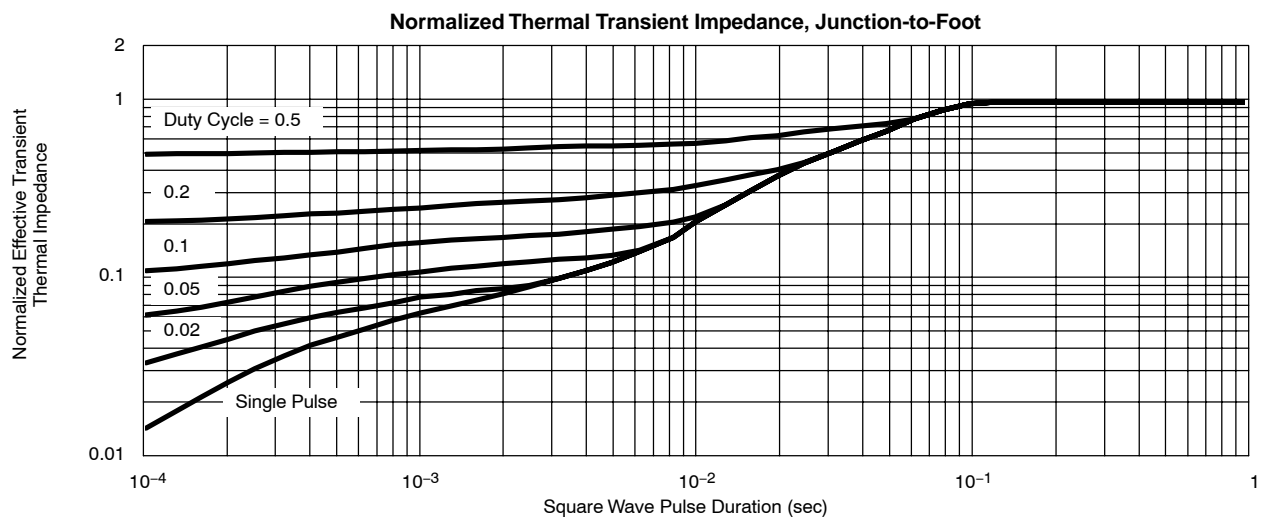
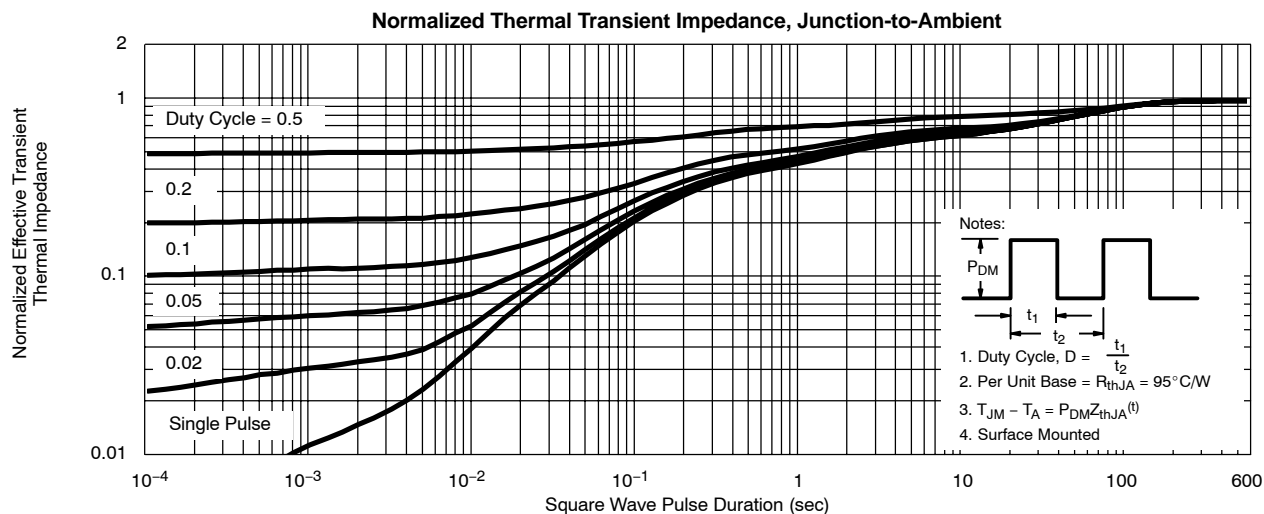
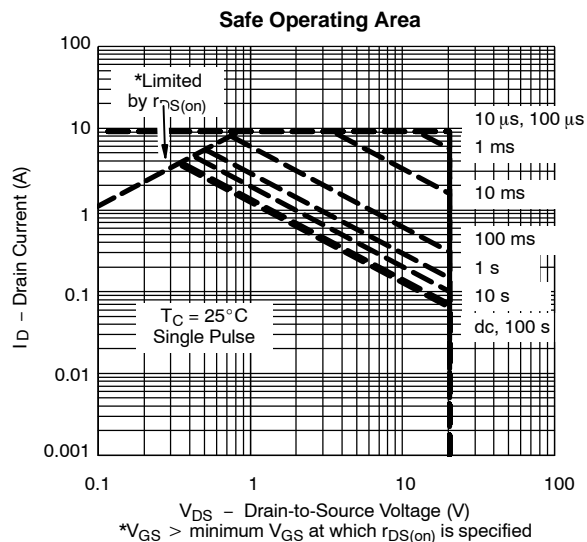
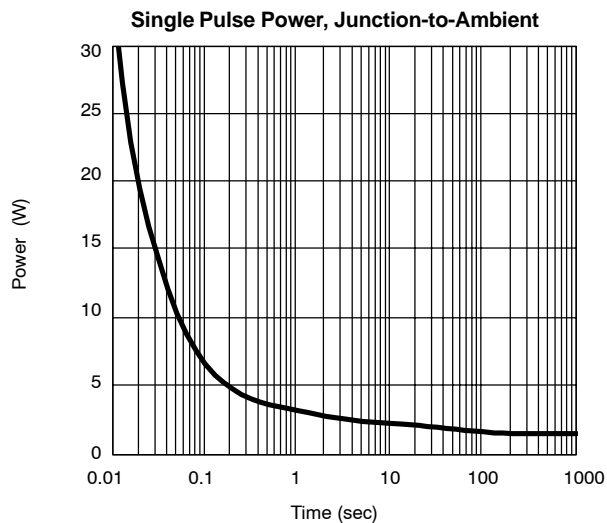
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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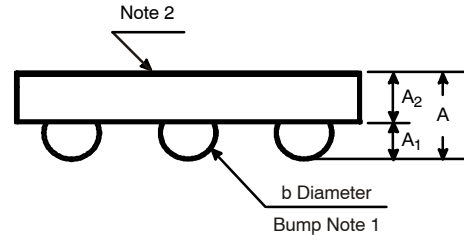
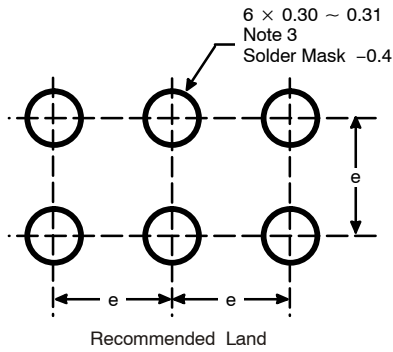


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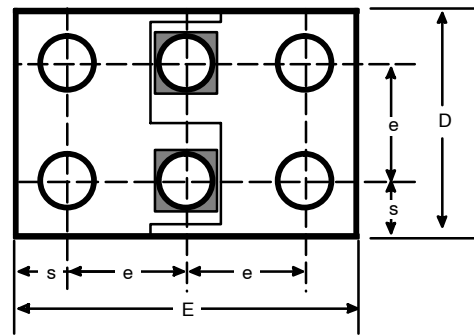


PACKAGE OUTLINE

MICRO FOOT: 6-BUMP (2 X 3, 0.8-mm PITCH)



Mark on Backside of Die



NOTES (Unless Otherwise Specified):

1. 6 solder bumps are Eutetic 63Sn/37Pb with diameter 0.37 – 0.41 mm
2. Backside surface is coated with a Ag/Ni/Ti layer
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.600	0.650	0.0236	0.0256
A ₁	0.260	0.290	0.102	0.114
A ₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.52	1.6	0.0598	0.0630
E	2.32	2.4	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
s	0.380	0.400	0.0150	0.0157

* Use millimeters as the primary measurement.

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