P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.065 @ V_{GS} = −4.5 V	−4.9
	0.095 @ V_{GS} = −2.5 V	−4.1

FEATURES

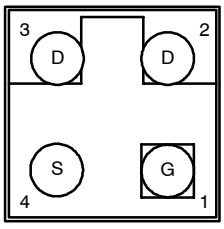
- TrenchFET® Power MOSFET
- New MICRO FOOT® Chipscale Packaging Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area
- Pin Compatible to Industry Standard Si3443DV

APPLICATIONS

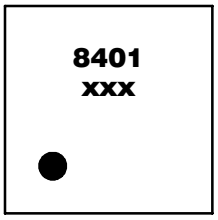
- PA, Battery and Load Switch
- Battery Charger Switch
- PA Switch

MICRO FOOT

Bump Side View

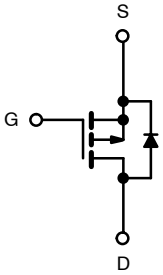


Backside View



Device Marking: 8401
xxx = Date/Lot Traceability Code

Ordering Information: Si8401DB-T1
Si8401DB-T1—E1 (Lead (Pb)-Free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	−20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	−4.9	−3.6	A
	T_A = 70°C		−3.9	−2.8	
Pulsed Drain Current		I_{DM}	−10		
continuous Source Current (Diode Conduction)[a]		I_S	−2.5	−2.5	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.77	1.47	W
	T_A = 70°C		1.77	0.94	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Package Reflow Conditions[b]	VPR		215/245[c]		°C
	IR/Convection		220/250[c]		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	35	45	°C/W
	Steady State		72	85	
Maximum Junction-to-Foot (drain)	Steady State	R_{thJF}	16	20	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.
c. Package reflow conditions for lead-free.

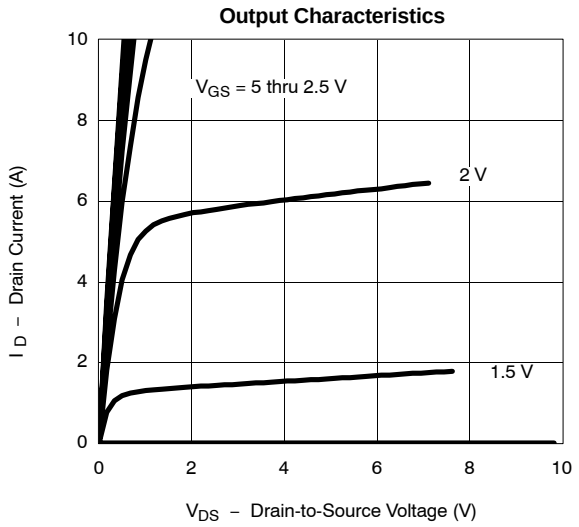
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

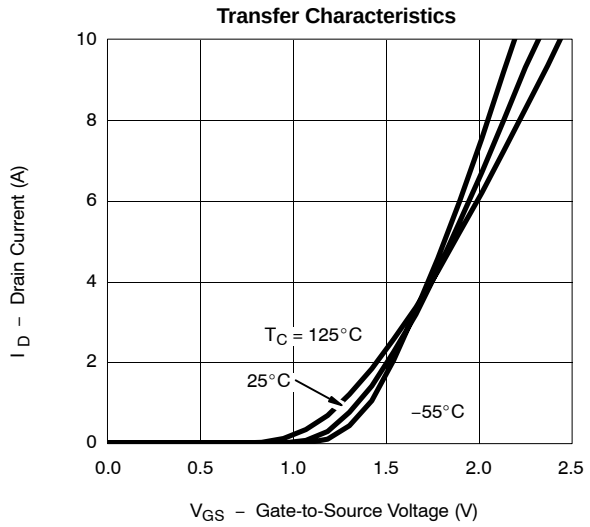
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.45	−0.9	1.4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−5			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −1 A		0.057	0.065	Ω
		V_{GS} = −2.5 V, I_D = −1 A		0.080	0.095	
Forward Transconductance[a]	g_{fs}	V_{DS} = −10 V, I_D = −1 A		6		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1 A, V_{GS} = 0 V		−0.73	−1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −1 A		11	17	nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			2.9		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω		17	25	ns
Rise Time	t_r			28	45	
Turn-Off Delay Time	$t_{d(off)}$			88	135	
Fall Time	t_f			60	90	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1 A, di/dt = 100 A/μs		40	60	
Reverse Recovery Charge	Q_{rr}			20	30	nC

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

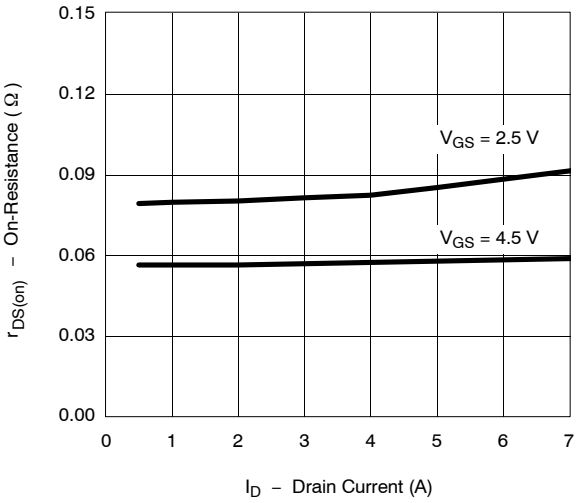
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



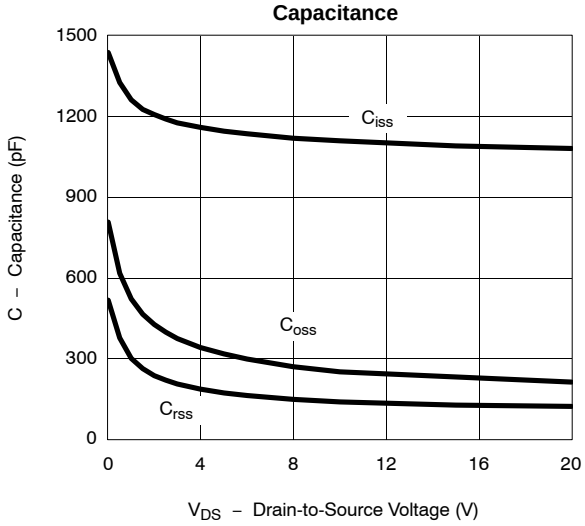


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

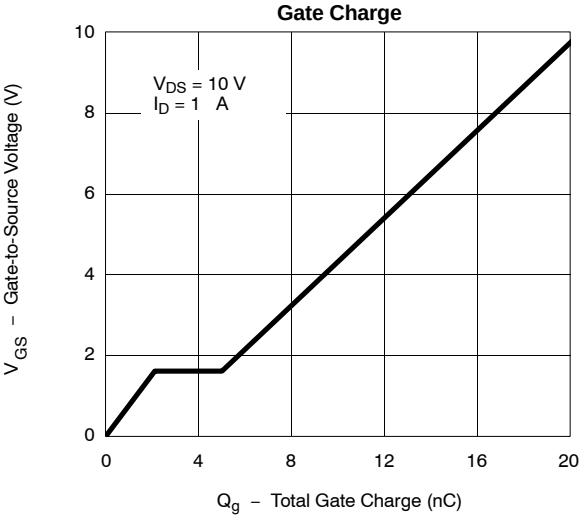
On-Resistance vs. Drain Current



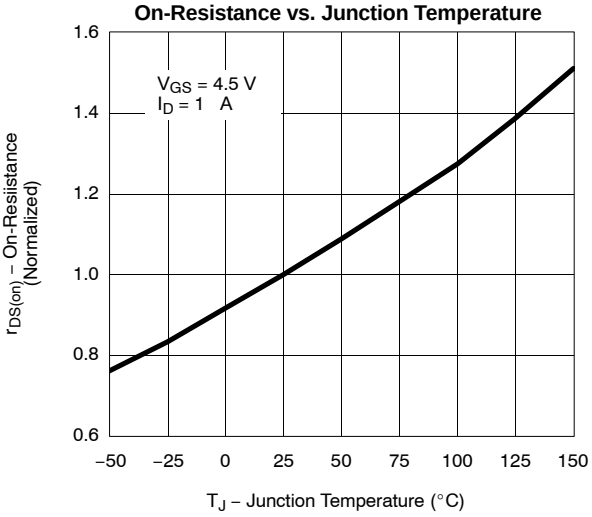
Capacitance



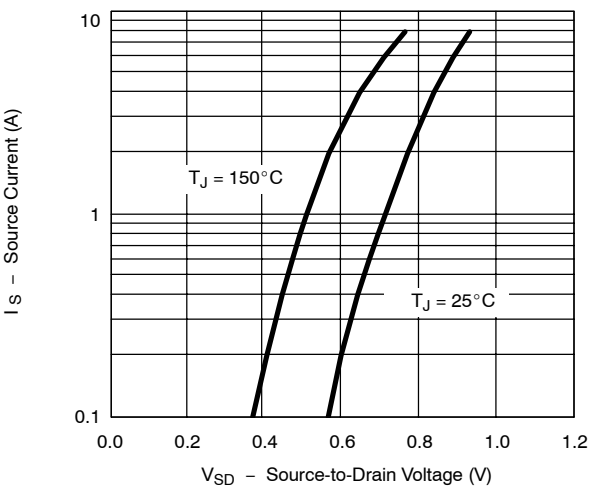
Gate Charge



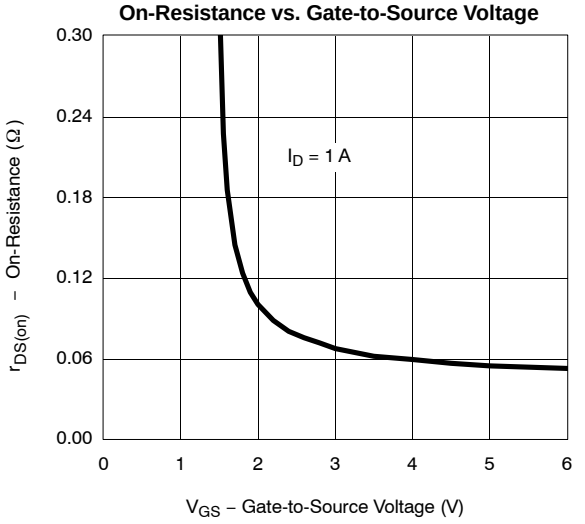
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

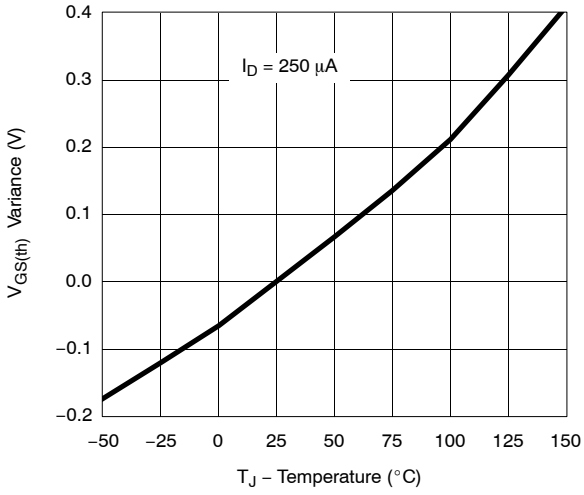


On-Resistance vs. Gate-to-Source Voltage

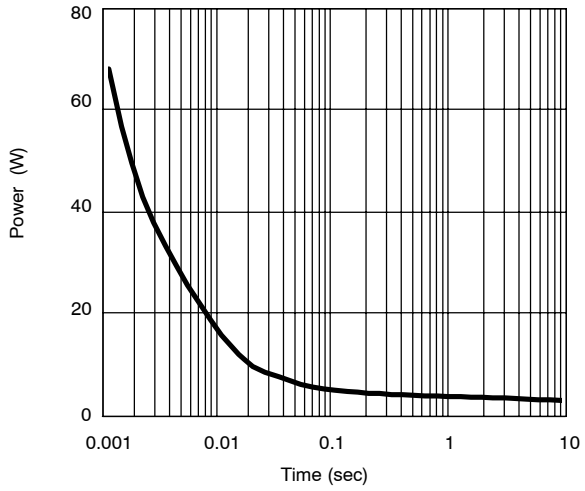


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

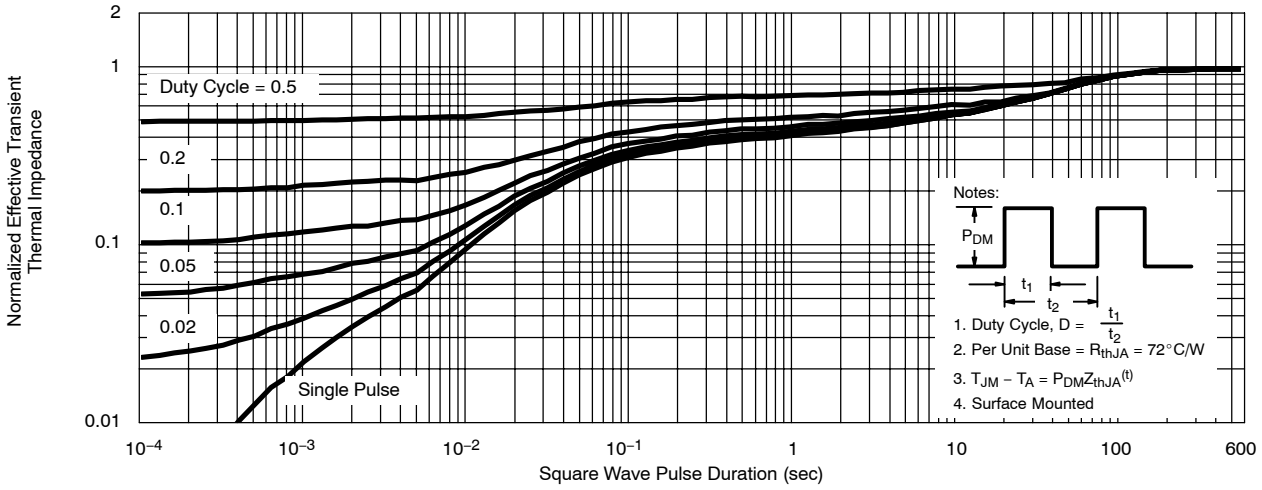
Threshold Voltage



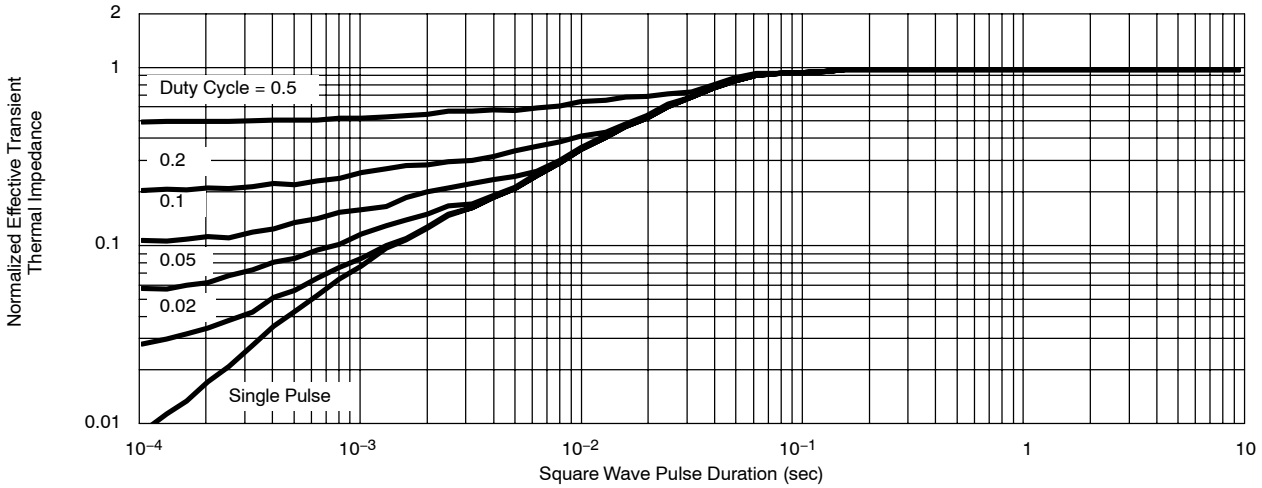
Single Pulse Power, Juncion-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

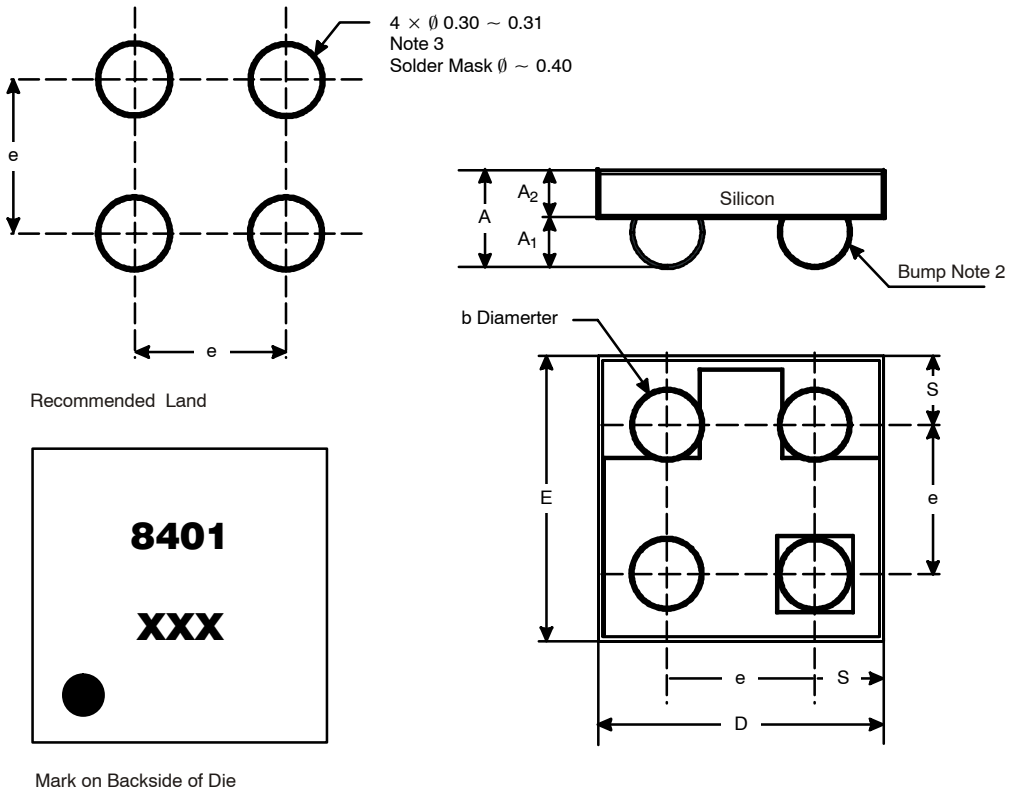


Normalized Thermal Transient Impedance, Junction-to-Foot



PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 X 2, 0.8-mm PITCH)



NOTES (Unless Otherwise Specified):

1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are Eutectic solder 63/57 Sn/Pb. (Sn 3.8 Ag, 0.7 Cu for Pb-free bumps)
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.600	0.650	0.0236	0.0256
A_1	0.260	0.290	0.0102	0.0114
A_2	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.750	0.850	0.0295	0.0335
S	0.370	0.380	0.0146	0.0150

* Use millimeters as the primary measurement.

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