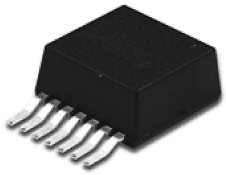
National Semiconductor

April 1, 2010

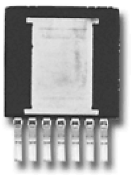
LMZ10505

5A SIMPLE SWITCHER® Power Module with 5.5V Maximum Input Voltage

Easy to Use 7 Pin Package



Isometric View



Bottom View

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TO-PMOD 7 Pin Package
10.16 x 13.77 x 4.57 mm (0.4 x 0.39 x 0.18 in)
θ_{JA} = 20°C/W, θ_{JC} = 1.9°C/W (*Note 3*)
RoHS Compliant

Electrical Specifications

- 25W maximum total output power
- Up to 5A output current
- Input voltage range 2.95V to 5.5V
- Output voltage range 0.8V to 5V
- ±1.63% feedback voltage accuracy over temperature
- Efficiency up to 96%

Key Features

- Integrated shielded inductor
- Flexible startup sequencing using external soft-start, tracking, and precision enable
- Protection against in-rush currents and faults such as input UVLO and output short-circuit
- -40°C to +125°C junction temperature operating range
- Single exposed pad and standard pinout for easy mounting and manufacturing
- Pin-to-pin compatible with
  LMZ10503 (3A/15W max)
  LMZ10504 (4A/20W max)
- Fully enable for WEBENCH® and Power Designer

Applications

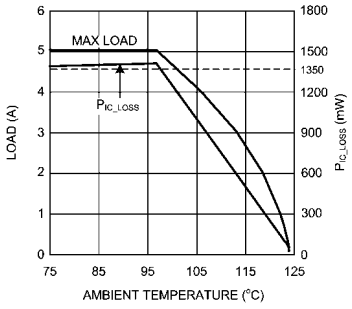
- Point-of-load conversions from 3.3V and 5V rails
- Space constrained applications
- Extreme temperatures/no air flow environments
- Noise sensitive applications (i.e. transceiver, medical)

Performance Benefits

- Operates at high ambient temperatures
- High efficiency up to 96% reduces system heat generation
- Low radiated emissions (EMI) complies with EN55022 class B standard (*Note 4*)
- Passes 10V/m radiated immunity EMI test standard EN61000 4-3
- Low output voltage ripple of 10 mV allows for powering noise-sensitive transceiver and signaling ICs
- Fast transient response for powering FPGAs and ASICs

System Performance

Current Derating (V_{OUT} = 3.3V)



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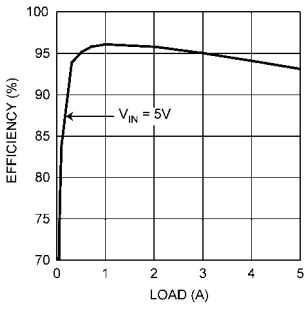
Efficiency (V_{OUT} = 3.3V)



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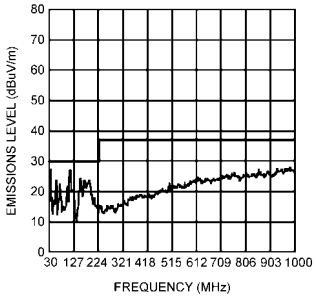
Radiated Emissions (EN 55022, Class B)



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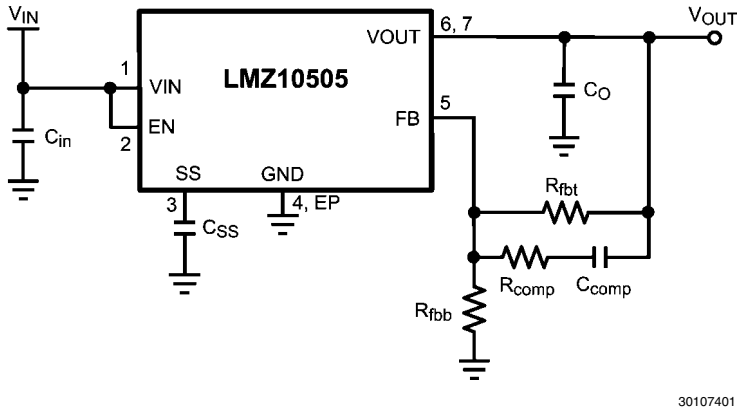
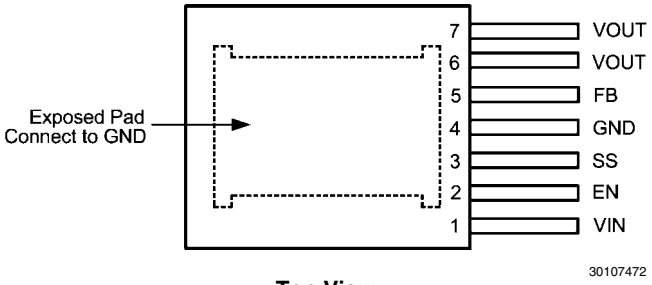
Note 1: θ_{JA} measured on a 2.25" x 2.25" (5.8 cm x 5.8 cm) four layer board. Refer to *PCB Layout Diagrams* or Evaluation Board Application Note: AN-2022.

Note 2: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See Figure 5 and layout for information on device under test.

Typical Application Circuit



Connection Diagram



Top View
7-Lead TO-PMOD

Ordering Information

Order Number	Supplied As	Package Type	NSC Package Drawing	Package Marking
LMZ10505TZE-ADJ	45 Units in a Rail	TO-PMOD-7	TZA07A	LMZ10505TZ-ADJ
LMZ10505TZ-ADJ	250 Units in Tape and Reel			
LMZ10505TZX-ADJ	500 Units in Tape and Reel			

Pin Descriptions

Pin Number	Name	Description
1	VIN	Power supply input. A low ESR input capacitance should be located as close as possible to the VIN pin and exposed pad (EP).
2	EN	Active high enable input for the device.
3	SS	Soft-start control pin. An internal 2 µA current source charges an external capacitor connected between SS and GND pins to set the output voltage ramp rate during startup. The SS pin can also be used to configure the tracking feature.
4	GND	Power ground and signal ground. Provide a direct connection to the EP. Place the bottom feedback resistor as close as possible to GND and FB pin.
5	FB	Feedback pin. This is the inverting input of the error amplifier used for sensing the output voltage. Keep the copper area of this node small.

Pin Number	Name	Description
6, 7	VOUT	The output terminal of the internal inductor. Connect the output filter capacitor between VOUT pin and EP.
EP	Exposed Pad	Exposed pad is used as a thermal connection to remove heat from the device. Connect this pad to the PC board ground plane in order to reduce thermal resistance value. EP must also provide a direct electrical connection to the input and output capacitors ground terminals. Connect EP to pin 4.

Absolute Maximum Ratings (*Note 5*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN, VOUT, EN, FB, SS to GND	-0.3V to 6.0V
ESD Susceptibility (*Note 6*)	±2 kV
Power Dissipation	Internally Limited
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Peak Reflow Case Temperature (30 sec)	245°C

Operating Ratings (*Note 5*)

VIN to GND	2.95V to 5.5V
Junction Temperature (T_J)	-40°C to 125°C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C only; limits in bold face type apply over the operating junction temperature range T_J of -40°C to 125°C. Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = V_{EN} = 3.3V, unless otherwise indicated in the conditions column.

Symbol	Parameter	Conditions	Min (*Note 7*)	Typ (*Note 8*)	Max (*Note 7*)	Units
SYSTEM PARAMETERS						
V_{FB}	Total Feedback Voltage Variation Including Line and Load Regulation	V_{IN} = 2.95V to 5.5V V_{OUT} = 2.5V I_{OUT} = 0A to 5A	**0.78**	0.8	**0.82**	V
V_{FB}	Feedback Voltage Variation	V_{IN} = 3.3V, V_{OUT} = 2.5V I_{OUT} = 0A	**0.787**	0.8	**0.812**	V
V_{FB}	Feedback Voltage Variation	V_{IN} = 3.3V, V_{OUT} = 2.5V I_{OUT} = 5A	**0.785**	0.798	**0.81**	V
$V_{IN(UVLO)}$	Input UVLO Threshold (Measured at VIN pin)	Rising		2.6	**2.95**	V
		Falling	**1.95**	2.4		
I_{SS}	Soft-Start Current	Charging Current		2		µA
I_Q	Non-Switching Input Current	V_{FB} = 1V		1.55	**3**	mA
I_{SD}	Shut Down Quiescent Current	V_{IN} = 5.5V, V_{EN} = 0V		267	**500**	µA
I_{OCL}	Output Current Limit (Average Current)	V_{OUT} = 2.5V	**5.1**	7.3	**8.7**	A
f_{FB}	Frequency Fold-back	In current limit		250		kHz
PWM SECTION						
f_{SW}	Switching Frequency		**750**	1000	**1160**	kHz
D_{range}	PWM Duty Cycle Range		**0**		**100**	%
ENABLE CONTROL						
V_{EN-IH}	EN Pin Rising Threshold			1.23	**1.8**	V
V_{EN-IF}	EN Pin Falling Threshold		**0.8**	1.06		V
THERMAL CONTROL						
T_{SD}	T_J for Thermal Shutdown			145		°C
T_{SD-HYS}	Hysteresis for Thermal Shutdown			10		°C
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	(*Note 3*)		20		°C/W
θ_{JC}	Junction to Case	No air flow		1.9		°C/W

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C only; limits in bold face type apply over the operating junction temperature range T_J of -40°C to 125°C. Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = V_{EN} = 3.3V, unless otherwise indicated in the conditions column.

Symbol	Parameter	Conditions	Min (*Note 7*)	Typ (*Note 8*)	Max (*Note 7*)	Units
PERFORMANCE PARAMETERS						
ΔV_{OUT}	Output Voltage Ripple	Refer to *Table 3* V_{OUT} = 2.5V Bandwidth Limit = 2 MHz		10		mV_{pk-pk}
ΔV_{OUT}	Output Voltage Ripple	Refer to *Table 5* Bandwidth Limit = 20 MHz		5		mV_{pk-pk}
ΔV_{FB} / V_{FB}	Feedback Voltage Line Regulation	ΔV_{IN} = 2.95V to 5.5V I_{OUT} = 0A		0.04		%
ΔV_{OUT} / V_{OUT}	Output Voltage Line Regulation	ΔV_{IN} = 2.95V to 5.5V I_{OUT} = 0A, V_{OUT} = 2.5V		0.04		%
ΔV_{FB} / V_{FB}	Feedback Voltage Load Regulation	I_{OUT} = 0A to 5A		0.25		%
ΔV_{OUT} / V_{OUT}	Output Voltage Load Regulation	I_{OUT} = 0A to 5A V_{OUT} = 2.5V		0.25		%
Efficiency						
η	Peak Efficiency (1A) V_{IN} = 5V	V_{OUT} = 3.3V		96.1		%
		V_{OUT} = 2.5V		94.8		
		V_{OUT} = 1.8V		93.1		
		V_{OUT} = 1.5V		92		
		V_{OUT} = 1.2V		90.4		
		V_{OUT} = 0.8V		86.8		
η	Peak Efficiency (1A) V_{IN} = 3.3V	V_{OUT} = 2.5V		95.7		%
		V_{OUT} = 1.8V		94.1		
		V_{OUT} = 1.5V		93.0		
		V_{OUT} = 1.2V		91.6		
		V_{OUT} = 0.8V		88.3		
η	Full Load Efficiency (5A) V_{IN} = 5V	V_{OUT} = 3.3V		93.1		%
		V_{OUT} = 2.5V		91.2		
		V_{OUT} = 1.8V		88.5		
		V_{OUT} = 1.5V		86.7		
		V_{OUT} = 1.2V		84.1		
		V_{OUT} = 0.8V		78.2		
η	Full Load Efficiency (5A) V_{IN} = 3.3V	V_{OUT} = 2.5V		89.8		%
		V_{OUT} = 1.8V		86.9		
		V_{OUT} = 1.5V		85.1		
		V_{OUT} = 1.2V		82.5		
		V_{OUT} = 0.8V		76.2		

Note 3: θ_{JA} measured on a 2.25" x 2.25" (5.8 cm x 5.8 cm) four layer board, with one ounce copper, thirty six 10mil thermal vias, no air flow, and 1W power dissipation. Refer to *PCB Layout Diagrams* or Evaluation Board Application Note: AN-2022.

Note 4: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See *Table 9* and layout for information on device under test.

Note 5: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 6: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22-AI14S.

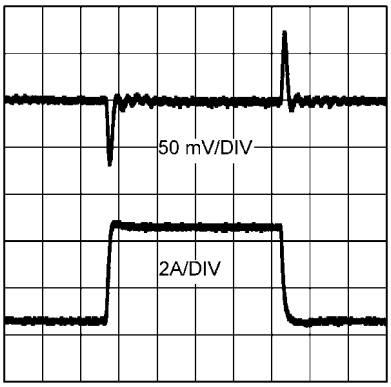
Note 7: Min and Max limits are 100% production tested at an ambient temperature (T_A) of 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 8: Typical numbers are at 25°C and represent the most likely parametric norm.

Typical Performance Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = V_{EN} = 5.0V, C_{IN} is 47 µF 10V X5R ceramic capacitor; $T_{AMBIENT}$ = 25°C for efficiency curves and waveforms.

Load Transient Response
V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{OUT} = 0.5A to 4.5A to 0.5A step
20 MHz Bandwidth Limited
Refer to *Table 5* for BOM, includes optional components



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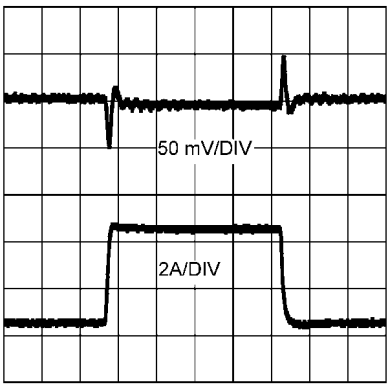
Load Transient Response
V_{IN} = 5.0V, V_{OUT} = 2.5V, I_{OUT} = 0.5A to 4.5A to 0.5A step
20 MHz Bandwidth Limited
Refer to *Table 5* for BOM, includes optional components



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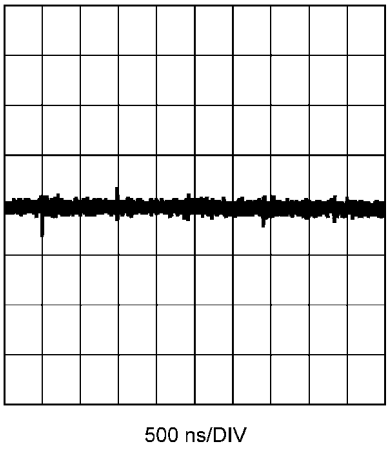
Output Voltage Ripple
V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{OUT} = 5A, 20 mV/DIV
Refer to *Table 5* for BOM



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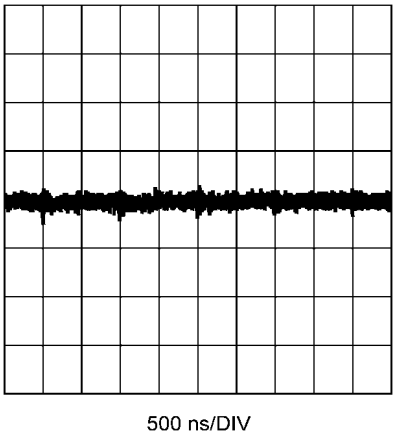
Output Voltage Ripple
V_{IN} = 5.0V, V_{OUT} = 2.5V, I_{OUT} = 5A, 20 mV/DIV
Refer to *Table 5* for BOM



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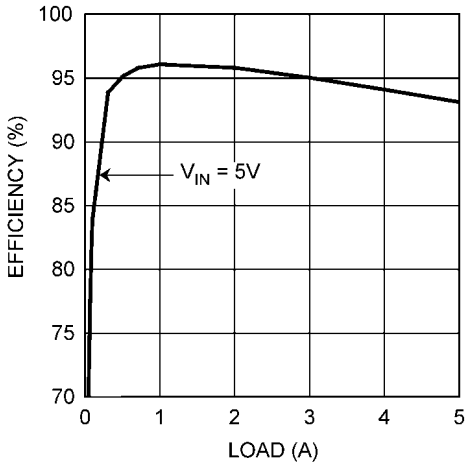
Efficiency
V_{OUT} = 3.3V



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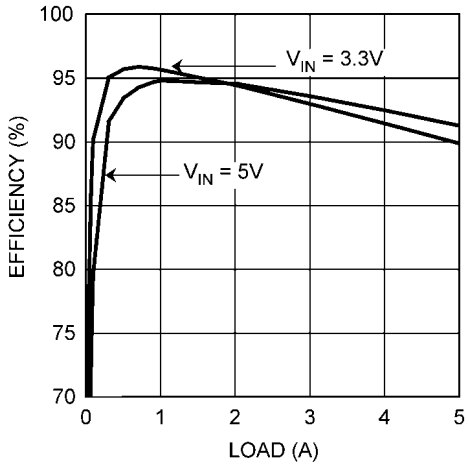
Efficiency
V_{OUT} = 2.5V



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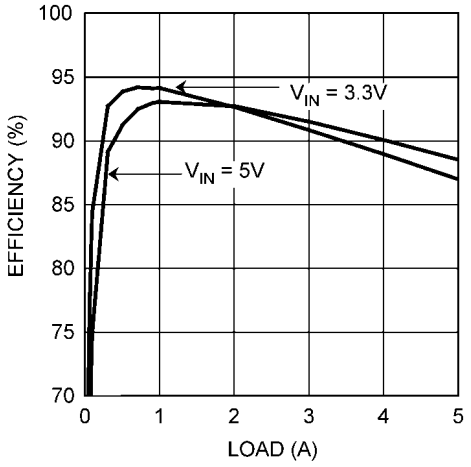
Efficiency
V_{OUT} = 1.8V



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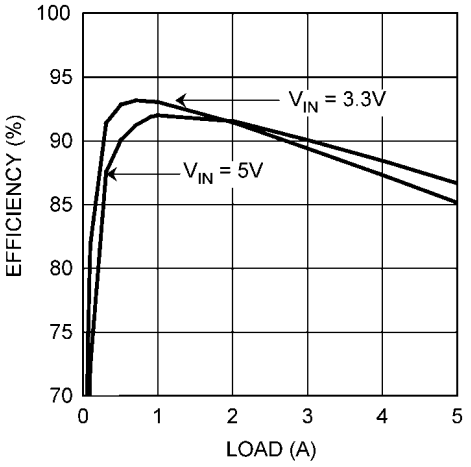
Efficiency
V_{OUT} = 1.5V



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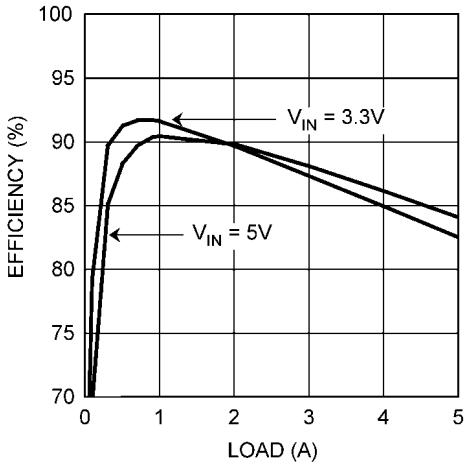
Efficiency
V_{OUT} = 1.2V



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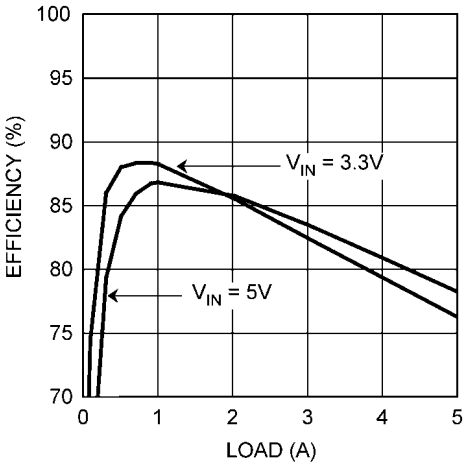
Efficiency
V_{OUT} = 0.8V



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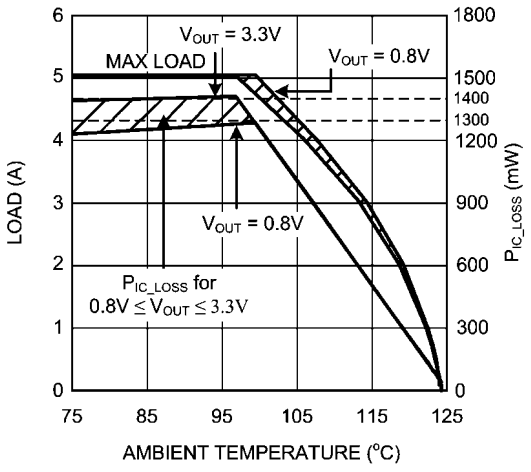
Current Derating
V_{IN} = 5V, θ_{JA} = 20°C / W



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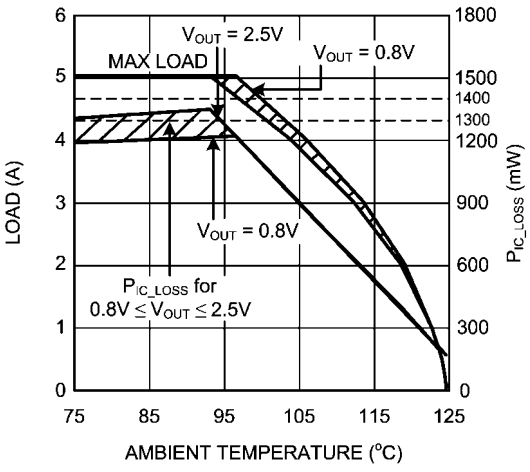
Current Derating
V_{IN} = 3.3V, θ_{JA} = 20°C / W



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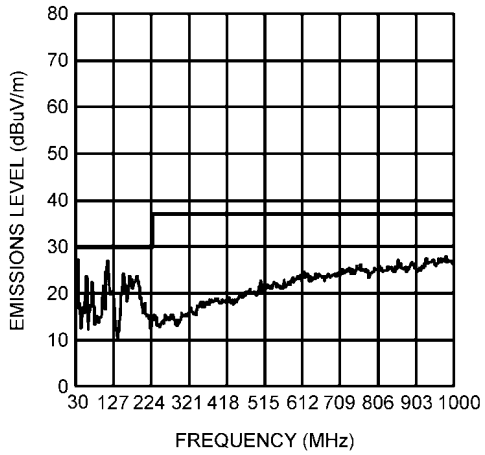
Radiated Emissions (EN 55022, Class B)
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 5A
Evaluation Board



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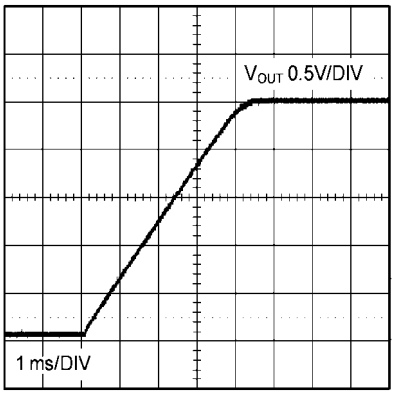
Startup
V_{OUT} = 2.5V, I_{OUT} = 0A



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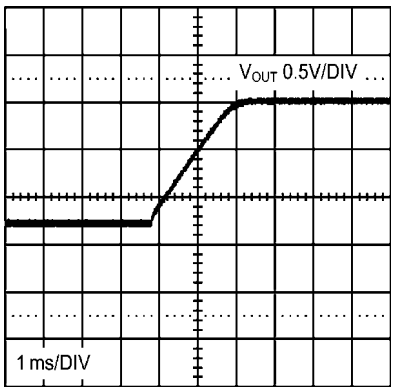
Pre-biased Startup
V_{OUT} = 2.5V, I_{OUT} = 0A



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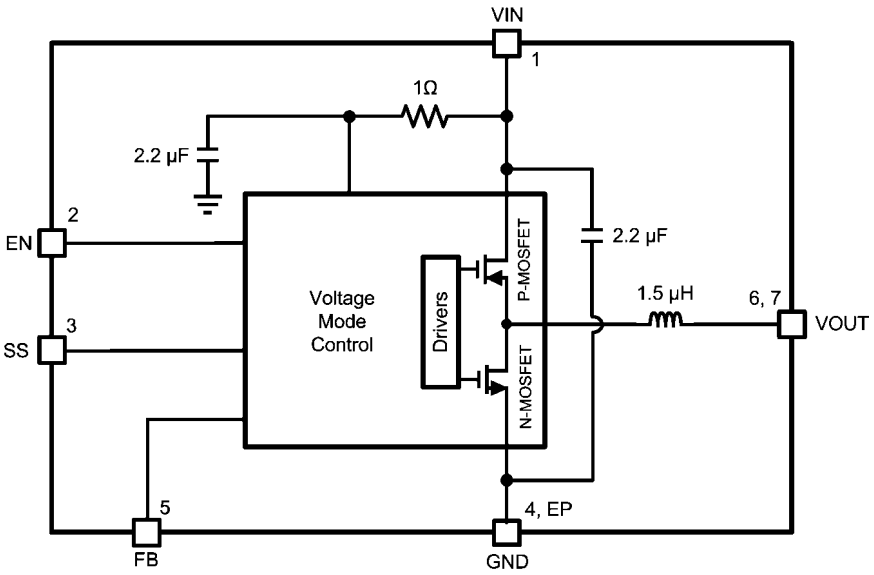
Block Diagram



General Description

The LMZ10505 SIMPLE SWITCHER® power module is a complete, easy-to-use DC-DC solution capable of driving up to a 5A load with exceptional power conversion efficiency, output voltage accuracy, line and load regulation. The LMZ10505 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ10505 can accept an input voltage rail between 2.95V and 5.5V and deliver an adjustable and highly accurate output voltage as low as 0.8V. One megahertz fixed frequency PWM switching provides a predictable EMI characteristic. Two external compensation components can be adjusted to set the fastest response time, while allowing the option to use ceramic and/or electrolytic output capacitors. Externally programmable soft-start capacitor facilitates controlled startup. The LMZ10505 is a reliable and robust solution with the following features: lossless cycle-by-cycle peak current limit to protect for over current or short-circuit fault, thermal shutdown, input under-voltage lock-out, and pre-biased startup.

Design Guideline And Operating Description

Design Steps

LMZ10505 is fully supported by Webench® and offers the following: component selection, performance, electrical, and thermal simulations as well as the Build-It board, for a reduced design time. On the other hand, all external components can be calculated by following the design procedure below.

1. Determine the input voltage and output voltage. Also, make note of the ripple voltage and voltage transient requirements.
2. Determine the necessary input and output capacitance.
3. Calculate the feedback resistor divider.
4. Select the optimized compensation component values.
5. Estimate the power dissipation and board thermal requirements.
6. Follow the PCB design guideline.
7. Learn about the LMZ10505 features such as enable, input UVLO, soft-start, tracking, pre-biased startup, current limit, and thermal shutdown.

Design Example

For this example the following application parameters exist.

- V_{IN} = 5V
- V_{OUT} = 2.5V
- I_{OUT} = 5A
- ΔV_{OUT} = 20 mV_{pk-pk}
- ΔV_{o_tran} = ±20 mV_{pk-pk}

Input Capacitor Selection

A 22 µF or 47 µF high quality dielectric (X5R, X7R) ceramic capacitor rated at twice the maximum input voltage is typically sufficient. The input capacitor must be placed as close as possible to the VIN pin and GND exposed pad to substantially eliminate the parasitic effects of any stray inductance or resistance on the PC board and supply lines.

Neglecting capacitor equivalent series resistance (ESR), the resultant input capacitor AC ripple voltage is a triangular waveform. The minimum input capacitance for a given peak-to-peak value (ΔV_{IN}) of V_{IN} is specified as follows:

$$C_{in} \geq \frac{I_{OUT} \times D \times (1 - D)}{f_{SW} \times \Delta V_{IN}}$$

where the PWM duty cycle, D, is given by:

$$D = \frac{V_{OUT}}{V_{IN}}$$

If ΔV_{IN} is 1% of V_{IN}, this equals to 50 mV and f_{SW} = 1 MHz

$$C_{in} \geq \frac{5A \times \left(\frac{2.5V}{5V}\right) \times \left(1 - \frac{2.5V}{5V}\right)}{1\ MHz \times 50\ mV} \geq 25\ \mu F$$

A second criteria before finalizing the C_{in} bypass capacitor is the RMS current capability. The necessary RMS current rating of the input capacitor to a buck regulator can be estimated by

$$I_{Cin(RMS)} = I_{OUT} \times \sqrt{D(1-D)}$$

$$I_{Cin(RMS)} = 5A \times \sqrt{\frac{2.5V}{5V}\left(1 - \frac{2.5V}{5V}\right)} = 2.5A$$

With this high AC current present in the input capacitor, the RMS current rating becomes an important parameter. The maximum input capacitor ripple voltage and RMS current occur at 50% duty cycle. Select an input capacitor rated for at least the maximum calculated $I_{Cin(RMS)}$.

Additional bulk capacitance with higher ESR may be required to damp any resonance effects of the input capacitance and parasitic inductance.

Output Capacitor Selection

In general, 22 µF to 100 µF high quality dielectric (X5R, X7R) ceramic capacitor rated at twice the maximum output voltage is sufficient given the optimal high frequency characteristics and low ESR of ceramic dielectrics. Although, the output capacitor can also be of electrolytic chemistry for increased capacitance density.

Two output capacitance equations are required to determine the minimum output capacitance. One equation determines the output capacitance (C_O) based on PWM ripple voltage. The second equation determines C_O based on the load transient characteristics. Select the largest capacitance value of the two.

The minimum capacitance, given the maximum output voltage ripple (ΔV_{OUT}) requirement, is determined by the following equation:

$$\Delta C_{OUT} = \frac{\Delta i_L}{8 \times f_{SW} \times [\Delta V_{OUT} - (\Delta i_L \times R_{ESR})]}$$

Where the peak to peak inductor current ripple (Δi_L) is equal to:

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

R_{ESR} is the total output capacitor ESR, L is the inductance value of the internal power inductor, where L = 1.5 µH, and f_{SW} = 1 MHz. Therefore, per the design example:

$$\Delta i_L = \frac{(5V - 2.5V) \times \frac{2.5V}{5V}}{1.5\ \mu H \times 1\ MHz} = 833\ mA$$

The minimum output capacitance requirement due to the PWM ripple voltage is:

$$C_O \geq \frac{833\ mA}{8 \times 1\ MHz \times [20\ mV - (833\ mA \times 3\ m\Omega)]}$$

$$C_O \geq 6\ \mu F$$

Three miliohms is a typical R_{ESR} value for ceramic capacitors.

The following equation provides a good first pass capacitance requirement for a load transient:

$$C_o \geq \frac{I_{step} \times V_{FB} \times L \times V_{IN}}{4 \times V_{OUT} \times (V_{IN} - V_{OUT}) \times \Delta Vo\_tran}$$

Where I_{step} is the peak to peak load step (10% to 90% of the maximum load for this example), V_{FB} = 0.8V, and ΔV_{o_tran} is the maximum output voltage deviation, which is ±20 mV.

Therefore the capacitance requirement for the given design parameters is:

$$C_o \geq \frac{4A \times 0.8V \times 1.5\ \mu H \times 5V}{4 \times 2.5V \times (5V - 2.5V) \times 20\ mV}$$

$$C_o \geq 48\ \mu F$$

In this particular design the output capacitance is determined by the load transient requirements.

Table 1 lists some examples of commercially available capacitors that can be used with the LMZ10505.

TABLE 1. Recommended Output Filter Capacitors

C_O (µF)	Voltage (V), R_{ESR} (mΩ)	Make	Manufacturer	Part Number	Case Size
22	6.3, < 5	Ceramic, X5R	TDK	C3216X5R0J226M	1206
47	6.3, < 5	Ceramic, X5R	TDK	C3216X5R0J476M	1206
47	6.3, < 5	Ceramic, X5R	TDK	C3225X5R0J476M	1210
47	10.0, < 5	Ceramic, X5R	TDK	C3225X5R1A476M	1210
100	6.3, < 5	Ceramic, X5R	TDK	C3225X5R0J107M	1210
100	6.3, 50	Tantalum	AVX	TPSD157M006#0050	D, 7.5 x 4.3 x 2.9 mm
100	6.3, 25	Organic Polymer	Sanyo	6TPE100MPB2	B2, 3.5 x 2.8 x 1.9 mm
150	6.3, 18	Organic Polymer	Sanyo	6TPE150MIC2	C2, 6.0 x 3.2 x 1.8 mm
330	6.3, 18	Organic Polymer	Sanyo	6TPE330MIL	D3L, 7.3 x 4.3 x 2.8 mm
470	6.3, 23	Niobium Oxide	AVX	NOME37M006#0023	E, 7.3 x 4.3 x 4.1 mm

Output Voltage Setting

A resistor divider network from V_{OUT} to the FB pin determines the desired output voltage as follows:

$$V_{OUT} = 0.8V \times \frac{R_{fbt} + R_{fbb}}{R_{fbb}}$$

R_{fbt} is defined based on the voltage loop requirements and R_{fbb} is then selected for the desired output voltage. Resistors are normally selected as 0.5% or 1% tolerance. Higher accuracy resistors such as 0.1% are also available.

The feedback voltage (at V_{OUT} = 2.5V) is accurate to within -2.5% / +2.5% over temperature and over line and load regulation. Additionally, the LMZ10505 contains error nulling circuitry to substantially eliminate the feedback voltage variation over temperature as well as the long term aging effects of the internal amplifiers. In addition the zero nulling circuit dramatically reduces the 1/f noise of the bandgap amplifier and reference. The manifestation of this circuit action is that the duty cycle will have two slightly different but distinct operating points, each evident every other switching cycle.

Loop Compensation

The LMZ10505 preserves flexibility by integrating the control components around the internal error amplifier while utilizing three small external compensation components from V_{OUT} to FB. An integrated type II (two pole, one zero) voltage-mode compensation network is featured. To ensure stability, an external resistor and small value capacitor can be added across the upper feedback resistor as a pole-zero pair to complete a type III (three pole, two zero) compensation network. The compensation components recommended in *Table 2* provide type III compensation at an optimal control loop performance. The typical phase margin is 45° with a bandwidth of 80 kHz. Calculated output capacitance values not listed in *Table 2* should be verified before designing into production. A detailed application note is available to provide verification support, AN-2013. In general, calculated output capacitance values below the suggested value will have reduced phase margin and higher control loop bandwidth. Output capacitance values above the suggested values will experience a lower bandwidth and increased phase margin. Higher bandwidth is associated with faster system response to sudden changes such as load transients. Phase margin changes the characteristics of the response. Lower phase margin is associated with underdamped ringing and higher phase margin is associated with overdamped response. Losing all phase margin will cause the system to be unstable; an optimized area of operation is 30° to 60° of phase margin, with a bandwidth of 100 kHz ±20 kHz.

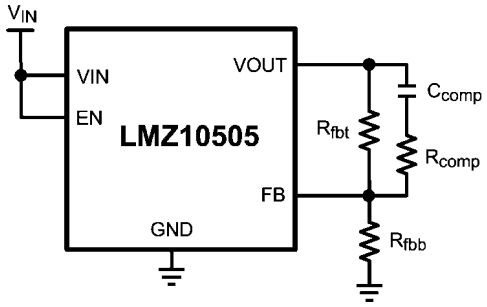


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TABLE 2. LMZ10505 Compensation Component Values

V_{IN} (V)	C_O (µF)	ESR (mΩ)		R_{fbt} (kΩ)	C_{comp} (pF)	R_{comp} (kΩ)
		Min	Max			
5.0	22	2	20	200	27	1.5
	47	2	20	124	56	1.4
	100	1	10	82.5	120	1
	150	1	5	63.4	180	1.21
	150	10	25	63.4	220	16.5
	150	26	50	44.2	220	23.7
	220	15	30	63.4	220	23.7
	220	31	60	76.8	220	57.6
3.3	22	2	20	118	39	9.09
	47	2	20	76.8	82	8.45
	100	1	10	49.9	180	4.12
	150	1	5	40.2	330	2.0
	150	10	25	43.2	330	11.5
	150	26	50	49.9	270	25.5
	220	15	30	40.2	390	15.4
	220	31	60	48.7	330	35.7

Note: In the special case where the output voltage is 0.8V, it is recommended to remove R_{fbb} and keep R_{fbt}, R_{comp}, and C_{comp} for a type III compensation.

Estimate Power Dissipation And Board Thermal Requirements

Use the current derating curves in the typical performance characteristics section to obtain an estimate of power loss (P_{IC_LOSS}). For the design case of V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 5A, $T_{A(MAX)}$ = 85°C , and $T_{J(MAX)}$ = 125°C, the device must see a thermal resistance from case to ambient (θ_{CA}) of less than:

$$\theta_{CA} < \frac{T_{J(MAX)} - T_{A(MAX)}}{P_{IC\_LOSS}} - \theta_{JC}$$

$$\theta_{CA} < \frac{125°C - 85°C}{1.36\ W} - 1.9\ \frac{°C}{W} < 27.5\ \frac{°C}{W}$$

Given the typical thermal resistance from junction to case (θ_{JC}) to be 1.9°C/W (typ.). Continuously operating at a T_J greater than 125°C will have a shorten life span.

To reach θ_{CA} = 27.5°C/W, the PCB is required to dissipate heat effectively. With no airflow and no external heat, a good estimate of the required board area covered by 1oz. copper on both the top and bottom metal layers is:

$$\text{Board Area\_cm}^2 \geq \frac{500}{\theta_{CA}} \cdot \frac{°C \times cm^2}{W}$$

$$\text{Board Area\_cm}^2 \geq \frac{500}{27.5\ \frac{°C}{W}} \cdot \frac{°C \times cm^2}{W}$$

As a result, approximately 18 square cm of 1oz. copper on top and bottom layers is required for the PCB design.

The PCB copper heat sink must be connected to the exposed pad (EP). Approximately thirty six, 10mils (254 µm) thermal vias spaced 59mils (1.5 mm) apart must connect the top copper to the bottom copper. For an extended discussion and formulations of thermal rules of thumb, refer to AN-2020. For an example of a high thermal performance PCB layout with θ_{JA} of 20°C/W, refer to the evaluation board application note AN-2022 and for results of a study of the effects of the PCB designs, refer to AN-2026.

PC Board Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

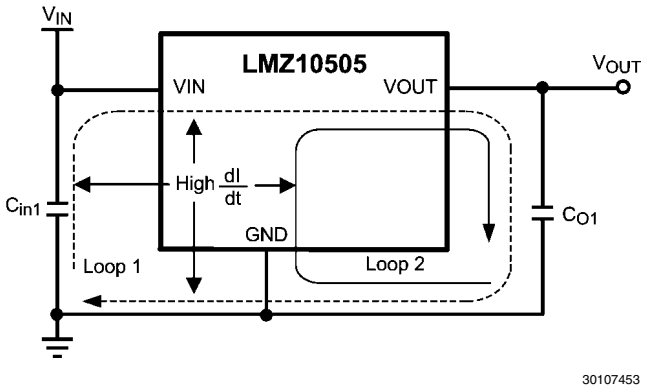


FIGURE 1. High Current Loops

1. Minimize area of switched current loops.

From an EMI reduction standpoint, it is imperative to minimize the high di/dt current paths. The high current that does not overlap contains high di/dt, see *Figure 1*. Therefore physically place input capacitor (C_{in1}) as close as possible to the LMZ10505 VIN pin and GND exposed pad to avoid observable high frequency noise on the output pin. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. Have a single point ground.

The ground connections for the feedback, soft-start, and enable components should be routed only to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly placed, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. Minimize trace length to the FB pin.

Both feedback resistors, R_{fbt} and R_{fbb}, and the compensation components, R_{comp} and C_{comp}, should be located close to the FB pin. Since the FB node is high impedance, keep the copper area as small as possible. This is most important as relatively high value resistors are used to set the output voltage.

4. Make input and output bus connections as wide as possible.

This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made at the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with minimum via diameter of 10mils (254 µm) thermal vias spaced 59mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

Additional Features

ENABLE

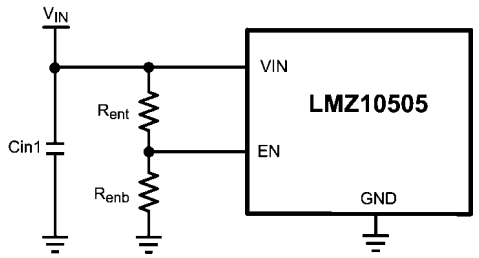
The LMZ10505 features an enable (EN) pin and associated comparator to allow the user to easily sequence the LMZ10505 from an external voltage rail, or to manually set the input UVLO threshold. The turn-on or rising threshold and hysteresis for this comparator are typically 1.23V and 0.15V respectively. The precise reference for the enable comparator allows the user to guarantee that the LMZ10505 will be disabled when the system demands it to be.

ENABLE AND UVLO

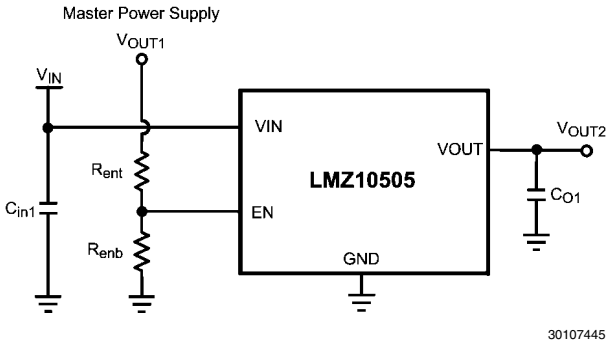
Using a resistor divider from VIN to EN as shown in the schematic diagram below, the input voltage at which the part begins switching can be increased above the normal input UVLO level according to

$$V_{IN(UVLO)} = 1.23V \times \frac{R_{trkb} + R_{trkt}}{R_{trkt}}$$

For example, suppose that the required input UVLO level is 3.69V. Choosing R_{enb} = 10 kΩ, then we calculate R_{ent} = 20 kΩ.



Alternatively, the EN pin can be driven from another voltage source to cater to system sequencing requirements commonly found in FPGA and other multi-rail applications. The following schematic shows an LMZ10505 that is sequenced to start based on the voltage level of a master system rail (V_{OUT1}).



SOFT-START

The LMZ10505 begins to operate when both the VIN and EN, voltages exceed the rising UVLO and enable thresholds, respectively. A controlled soft-start eliminates inrush currents during startup and allows the user more control and flexibility when sequencing the LMZ10505 with other power supplies.

In the event of either VIN or EN decreasing below the falling UVLO or enable threshold respectively, the voltage on the soft-start pin is collapsed by discharging the soft-start capacitor by a 14 µA (typ.) current sink to ground.

SOFT-START CAPACITOR

Determine the soft-start capacitance with the following relationship

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}}$$

where V_{FB} is the internal reference voltage (nominally 0.8V), I_{SS} is the soft-start charging current (nominally 2 µA) and C_{SS} is the external soft-start capacitance.

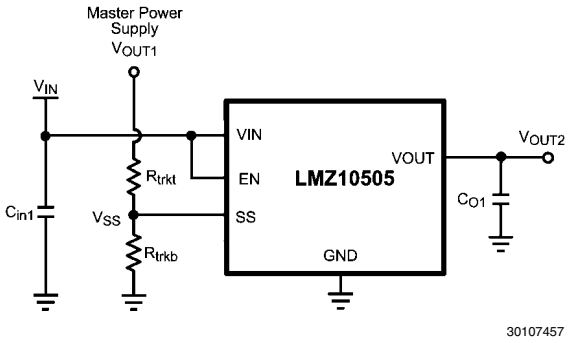
Thus, the required soft-start capacitor per unit output voltage startup time is given by

$$C_{SS} = 2.5 \text{ nF / ms}$$

For example, a 4 ms soft-start time will yield a 10 nF capacitance. The minimum soft-start capacitance is 680 pF.

TRACKING

The LMZ10505 can track the output of a master power supply during soft-start by connecting a resistor divider to the SS pin. In this way, the output voltage slew rate of the LMZ10505 will be controlled by a master supply for loads that require precise sequencing. When the tracking function is used, a small value soft-start capacitor should be connected to the SS pin to alleviate output voltage overshoot when recovering from a current limit fault.



TRACKING - EQUAL SOFT-START TIME

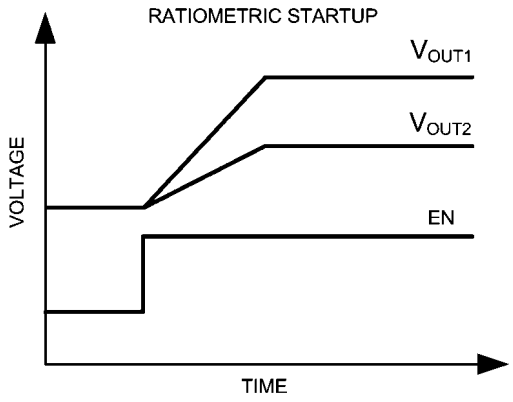
One way to use the tracking feature is to design the tracking resistor divider so that the master supply output voltage, V_{OUT1}, and the LMZ10505 output voltage, V_{OUT2}, both rise together and reach their target values at the same time. This is termed ratiometric startup. For this case, the equation governing the values of tracking divider resistors R_{trkb} and R_{trkt} is given by

$$R_{trkb} = \frac{R_{trkt}}{V_{OUT1} - 1.0V}$$

The above equation includes an offset voltage, of 200 mV, to ensure that the final value of the SS pin voltage exceeds the reference voltage of the LMZ10505. This offset will cause the LMZ10505 output voltage to reach regulation slightly before the master supply. A value of 33 kΩ 1% is recommended for R_{trkt} as a compromise between high precision and low quiescent current through the divider while minimizing the effect of the 2 µA soft-start current source.

For example, if the master supply voltage V_{OUT1} is 3.3V and the LMZ10505 output voltage was 1.8V, then the value of

R_{trkb} needed to give the two supplies identical soft-start times would be 14.3 kΩ. A timing diagram for this example, the equal soft-start time case, is shown below.



TRACKING - EQUAL SLEW RATES

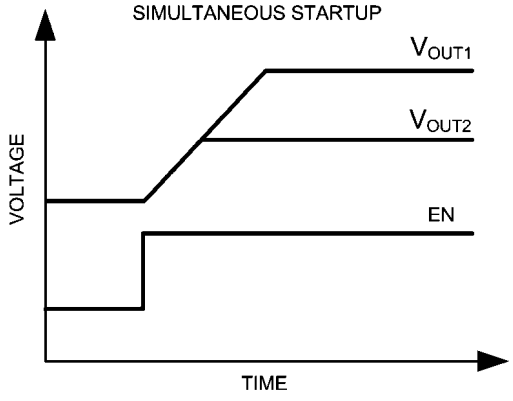
Alternatively, the tracking feature can be used to have similar output voltage ramp rates. This is referred to as simultaneous startup. In this case, the tracking resistors can be determined based on the following equation

$$R_{trkb} = \frac{0.8V}{V_{OUT2} - 0.8V} \times R_{trkt}$$

and to ensure proper overdrive of the SS pin

$$V_{OUT2} < 0.8 \times V_{OUT1}$$

For the example case of V_{OUT1} = 5V and V_{OUT2} = 2.5V, with R_{trkt} set to 33 kΩ as before, R_{trkb} is calculated from the above equation to be 15.5 kΩ. A timing diagram for the case of equal slew rates is shown below.



PRE-BIAS STARTUP CAPABILITY

At startup, the LMZ10505 is in a pre-biased state when the output voltage is greater than zero. This often occurs in many multi-rail applications such as when powering an ASIC, FPGA, or DSP. The output can be pre-biased in these applications through parasitic conduction paths from one supply rail to another. Even though the LMZ10505 is a synchronous converter, it will not pull the output low when a pre-bias condition exists. The LMZ10505 will not sink current during start-up until the soft-start voltage exceeds the voltage on the FB pin. Since the device does not sink current it protects the load from damage that might otherwise occur if current is conducted through the parasitic paths of the load.

CURRENT LIMIT

When a current greater than the output current limit (I_{OCL}) is sensed, the on-time is immediately terminated and the low side MOSFET is activated. The low side MOSFET stays on for the entire next four switching cycles. During these skipped pulses, the voltage on the soft-start pin is reduced by discharging the soft-start capacitor by a current sink on the soft-start pin of nominally 14 µA. Subsequent over-current events will drain more and more charge from the soft-start capacitor, effectively decreasing the reference voltage as the output droops due to the pulse skipping. Reactivation of the soft-start circuitry ensures that when the over-current situation is removed, the part will resume normal operation smoothly.

OVER-TEMPERATURE PROTECTION

When the LMZ10505 senses a junction temperature greater than 145°C (typ.), both switching MOSFETs are turned off and the part enters a standby state. Upon sensing a junction temperature below 135°C (typ.), the part will re-initiate the soft-start sequence and begin switching once again.

LMZ10505 Application Circuit Schematic and BOMs

This section provides several application solutions with an associated bill of materials. The compensation for each solution was optimized to work over the full input range. Many applications have a fixed input voltage rail. It is possible to modify the compensation to obtain a faster transient response for a given input voltage operating point.

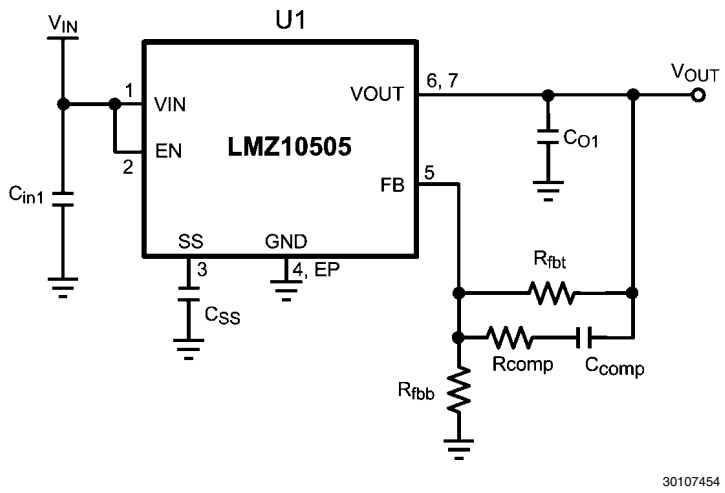


FIGURE 2.

TABLE 3. Bill of Materials, V_{IN} = 3.3V to 5V, V_{OUT} = 2.5V, $I_{OUT\ (MAX)}$ = 5A, Optimized for Electrolytic Input and Output Capacitance

Designator	Description	Case Size	Manufacturer	Manufacturer P/N	Quantity
U1	SIMPLE SWITCHER ®	TO-PMOD-7	National Semiconductor	LMZ10505TZ-ADJ	1
C_{in1}	150 µF, 6.3V, 18 mΩ	C2, 6.0 x 3.2 x 1.8 mm	Sanyo	6TPE150MIC2	1
C_{O1}	330 µF, 6.3V, 18 mΩ	D3L, 7.3 x 4.3 x 2.8 mm	Sanyo	6TPE330MIL	1
R_{fbt}	100 kΩ	0603	Vishay Dale	CRCW0603100KFKEA	1
R_{fbb}	47.5 kΩ	0603	Vishay Dale	CRCW060347K5FKEA	1
R_{comp}	15 kΩ	0603	Vishay Dale	CRCW060315K0FKEA	1
C_{comp}	330 pF, ±5%, C0G, 50V	0603	TDK	C1608C0G1H331J	1
C_{SS}	10 nF, ±10%, X7R, 16V	0603	Murata	GRM188R71C103KA01	1

TABLE 4. Bill of Materials, V_{IN} = 3.3V, V_{OUT} = 0.8V, $I_{OUT\ (MAX)}$ = 5A, Optimized for Solution Size and Transient Response

Designator	Description	Case Size	Manufacturer	Manufacturer P/N	Quantity
U1	SIMPLE SWITCHER ®	TO-PMOD-7	National Semiconductor	LMZ10505TZ-ADJ	1
C_{in1}, C_{O1}	47 µF, X5R, 6.3V	1206	TDK	C3216X5R0J476M	2
R_{fbt}	110 kΩ	0402	Vishay Dale	CRCW0402100KFKED	1
R_{comp}	1.0 kΩ	0402	Vishay Dale	CRCW04021K00FKED	1
C_{comp}	27 pF, ±5%, C0G, 50V	0402	Murata	GRM1555C1H270JZ01	1
C_{SS}	10 nF, ±10%, X7R, 16V	0402	Murata	GRM155R71C103KA01	1

In the case where the output voltage is 0.8V, it is recommended to remove R_{fbb} and keep R_{fbt}, R_{comp}, and C_{comp} for a type III compensation.

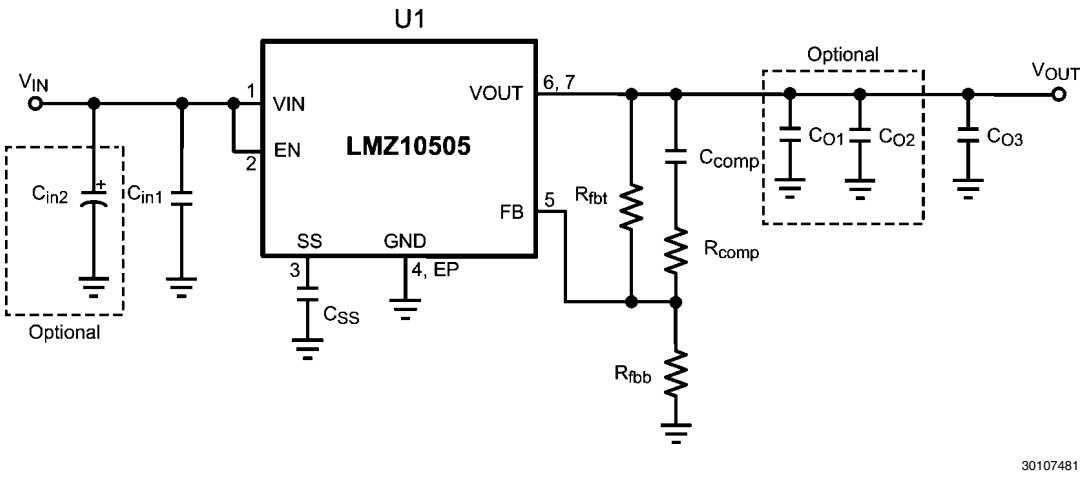


FIGURE 3.

TABLE 5. Bill of Materials, V_{IN} = 3.3V to 5V, V_{OUT} = 2.5V, $I_{OUT\ (MAX)}$ = 5A, Optimized for Low Input and Output Ripple Voltage and Fast Transient Response

Designator	Description	Case Size	Manufacturer	Manufacturer P/N	Quantity
U1	SIMPLE SWITCHER®	TO-PMOD-7	National Semiconductor	LMZ10505TZ-ADJ	1
C_{in1}	22 µF, X5R, 10V	1210	AVX	1210ZD226MAT	2
C_{in2}	220 µF, 10V, AL-Elec	E	Panasonic	EEE1AA221AP	1*
C_{O1}	4.7 µF, X5R, 10V	0805	AVX	0805ZD475MAT	1*
C_{O2}	22 µF, X5R, 6.3V	1206	AVX	12066D226MAT	1*
C_{O3}	100 µF, X5R, 6.3V	1812	AVX	18126D107MAT	1
R_{fbt}	75 kΩ	0402	Vishay Dale	CRCW040275K0FKED	1
R_{fbb}	34.8 kΩ	0402	Vishay Dale	CRCW040234K8FKED	1
R_{comp}	1.0 kΩ	0402	Vishay Dale	CRCW04021K00FKED	1
C_{comp}	100 pF, ±5%, C0G, 50V	0402	Murata	GRM1555C1H101JZ01	1
C_{SS}	10 nF, ±10%, X7R, 16V	0402	Murata	GRM155R71C103KA01	1

* Optional components, include for low input and output voltage ripple.

TABLE 6. Output Voltage Setting (R_{fbt} = 75 kΩ)

V_{OUT}	R_{fbb}
2.5 V	34.8 kΩ
1.8 V	59 kΩ
1.5 V	84.5 kΩ
1.2 V	150 kΩ
0.9 V	590 kΩ

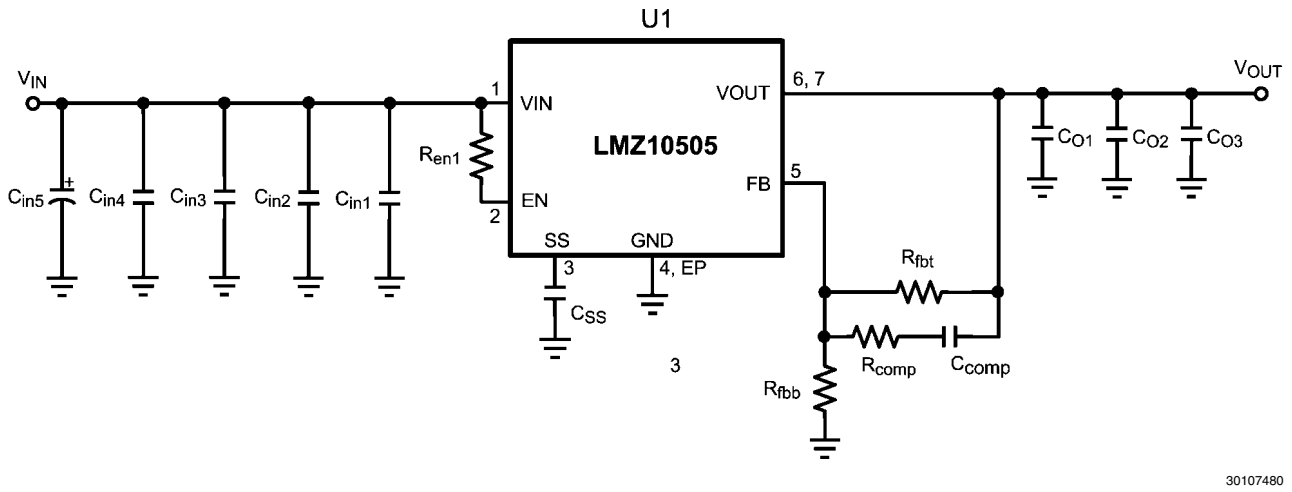


FIGURE 4.

TABLE 7. Bill of Materials, V_{IN} = 3.3V to 5V, V_{OUT} = 2.5V, $I_{OUT\ (MAX)}$ = 5A

Designator	Description	Case Size	Manufacturer	Manufacturer P/N	Quantity
U1	SIMPLE SWITCHER®	TO-PMOD-7	National Semiconductor	LMZ10505TZ-ADJ	1
C_{in1}	1 µF, X7R, 16V	0805	TDK	C2012X7R1C105K	1
C_{in2}, C_{O1}	4.7 µF, X5R, 6.3V	0805	TDK	C2012X5R0J475K	2
C_{in3}, C_{O2}	22 µF, X5R, 16V	1210	TDK	C3225X5R1C226M	2
C_{in4}	47 µF, X5R, 6.3V	1210	TDK	C3225X5R0J476M	1
C_{in5}	220 µF, 10V, AL-Elec	E	Panasonic	EEE1AA221AP	1
C_{O3}	100 µF, X5R, 6.3V	1812	TDK	C4532X5R0J107M	1
R_{fbt}	75 kΩ	0805	Vishay Dale	CRCW080575K0FKEA	1
R_{fbb}	34.8 kΩ	0805	Vishay Dale	CRCW080534K8FKEA	1
R_{comp}	1.1 kΩ	0805	Vishay Dale	CRCW08051K10FKEA	1
C_{comp}	180 pF, ±5%, C0G, 50V	0603	TDK	C1608C0G1H181J	1
R_{en1}	100 kΩ	0805	Vishay Dale	CRCW0805100KFKEA	1
C_{SS}	10 nF, ±5%, C0G, 50V	0805	TDK	C2012C0G1H103J	1

TABLE 8. Output Voltage Setting (R_{fbt} = 75 kΩ)

V_{OUT}	R_{fbb}
2.5 V	34.8 kΩ
1.8 V	59 kΩ
1.5 V	84.5 kΩ
1.2 V	150 kΩ
0.9 V	590 kΩ

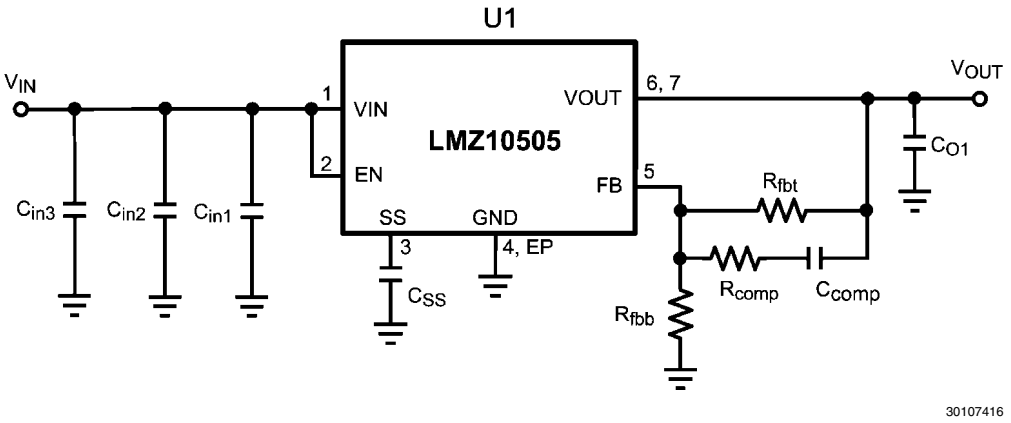


FIGURE 5.

TABLE 9. Bill of Materials, V_{IN} = 5V, V_{OUT} = 2.5V, $I_{OUT\ (MAX)}$ = 5A, Complies with EN55022 Class B Radiated Emissions

Designator	Description	Case Size	Manufacturer	Manufacturer P/N	Quantity
U1	SIMPLE SWITCHER®	TO-PMOD-7	National Semiconductor	LMZ10505TZ-ADJ	1
C_{in1}	1 µF, X7R, 16V	0805	TDK	C2012X7R1C105K	1
C_{in2}	4.7 µF, X5R, 6.3V	0805	TDK	C2012X5R0J475K	1
C_{in3}	47 µF, X5R, 6.3V	1210	TDK	C3225X5R0J476M	1
C_{O1}	100 µF, X5R, 6.3V	1812	TDK	C4532X5R0J107M	1
R_{fbt}	75 kΩ	0805	Vishay Dale	CRCW080575K0FKEA	1
R_{fbb}	34.8 kΩ	0805	Vishay Dale	CRCW080534K8FKEA	1
R_{comp}	1.1 kΩ	0805	Vishay Dale	CRCW08051K10FKEA	1
C_{comp}	180 pF, ±5%, C0G, 50V	0603	TDK	C1608C0G1H181J	1
C_{SS}	10 nF, ±5%, C0G, 50V	0805	TDK	C2012C0G1H103J	1

TABLE 10. Output Voltage Setting (R_{fbt} = 75 kΩ)

V_{OUT}	R_{fbb}
3.3 V	23.7 kΩ
2.5 V	34.8 kΩ
1.8 V	59 kΩ
1.5 V	84.5 kΩ
1.2 V	150 kΩ
0.9 V	590 kΩ

PCB Layout Diagrams

The PCB design is available in the LMZ10505 product folder at www.national.com.

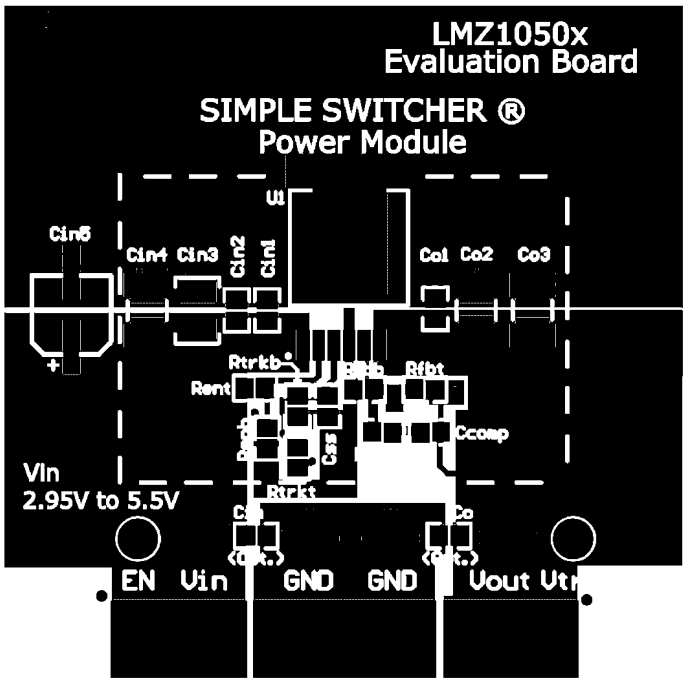


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FIGURE 6. Top Copper

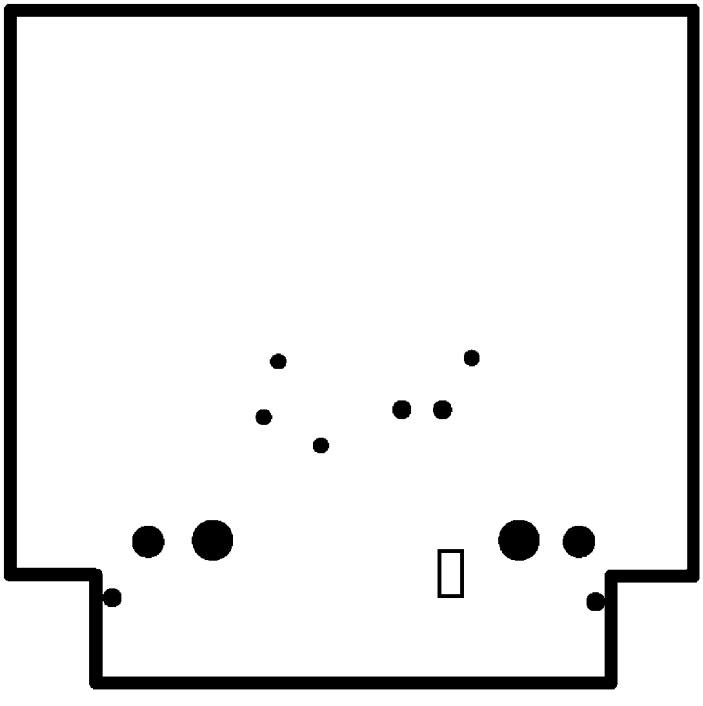

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FIGURE 7. Internal Layer 1 (Ground)

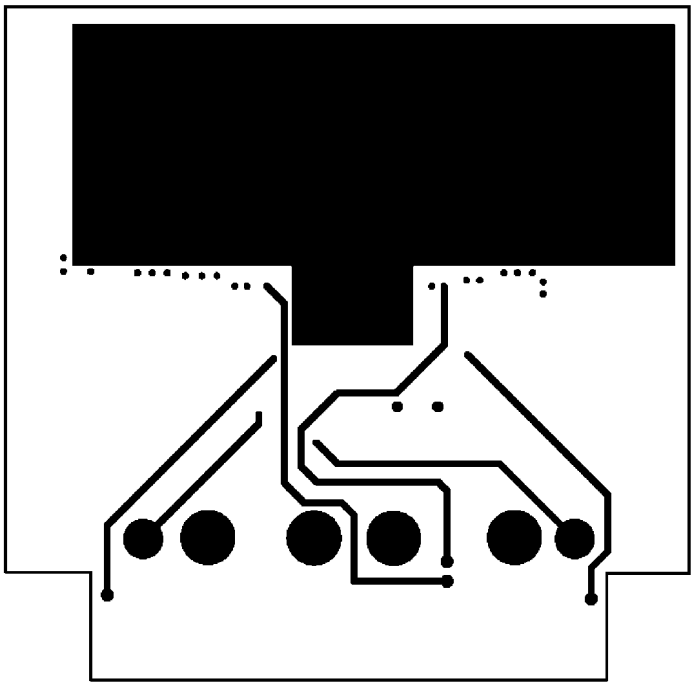

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FIGURE 8. Internal Layer 2 (Ground and Signal Traces)

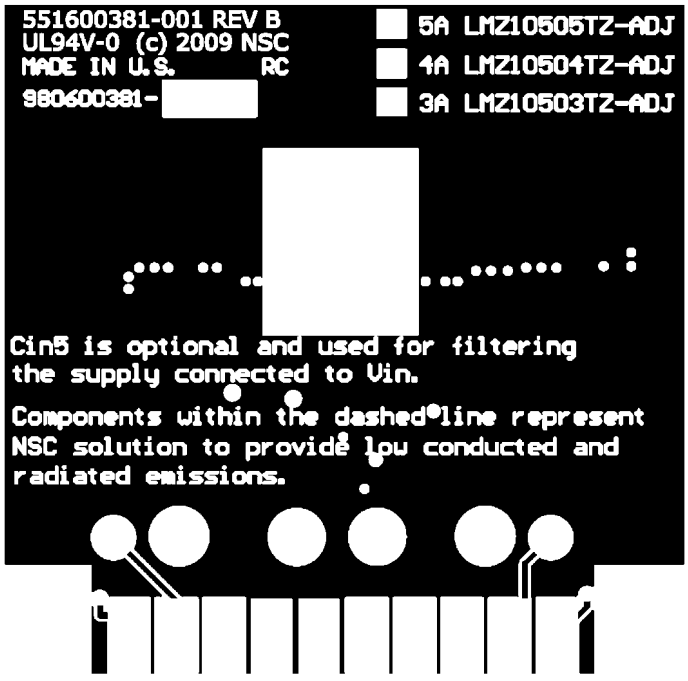

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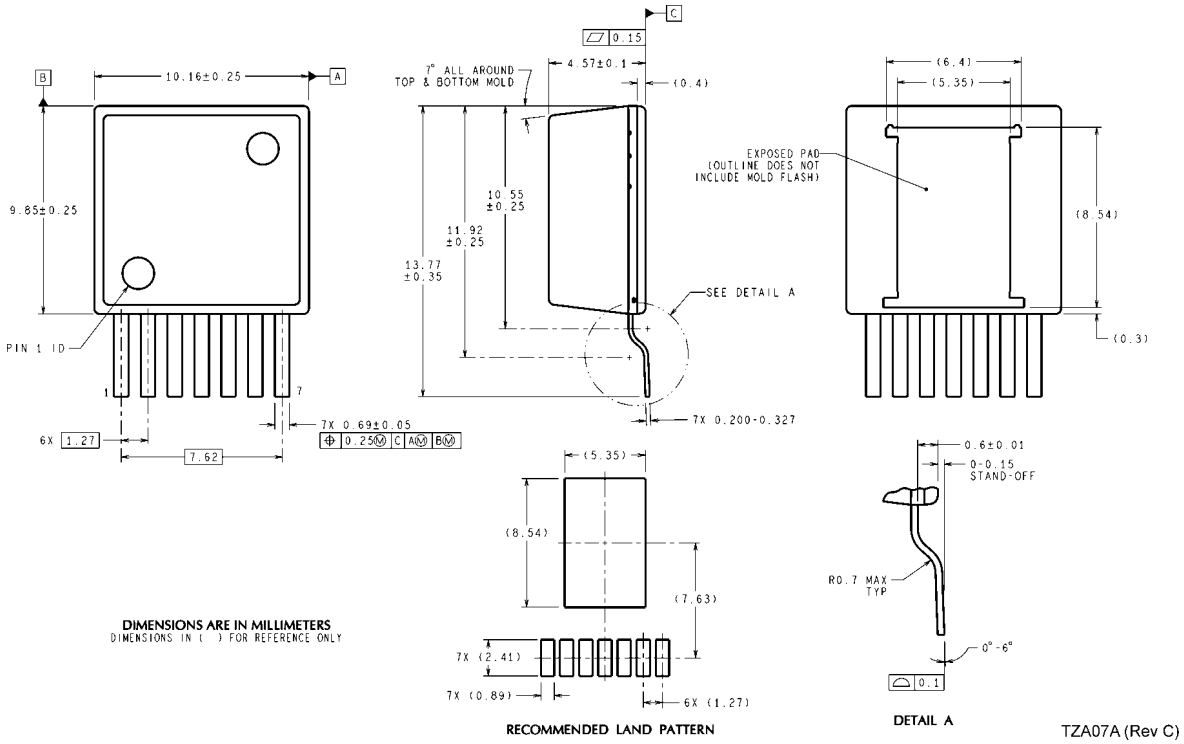
FIGURE 9. Bottom Copper

Physical Dimensions inches (millimeters) unless otherwise noted



TO-PMOD-7 Pin Package
NS Package Number TZA07A

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