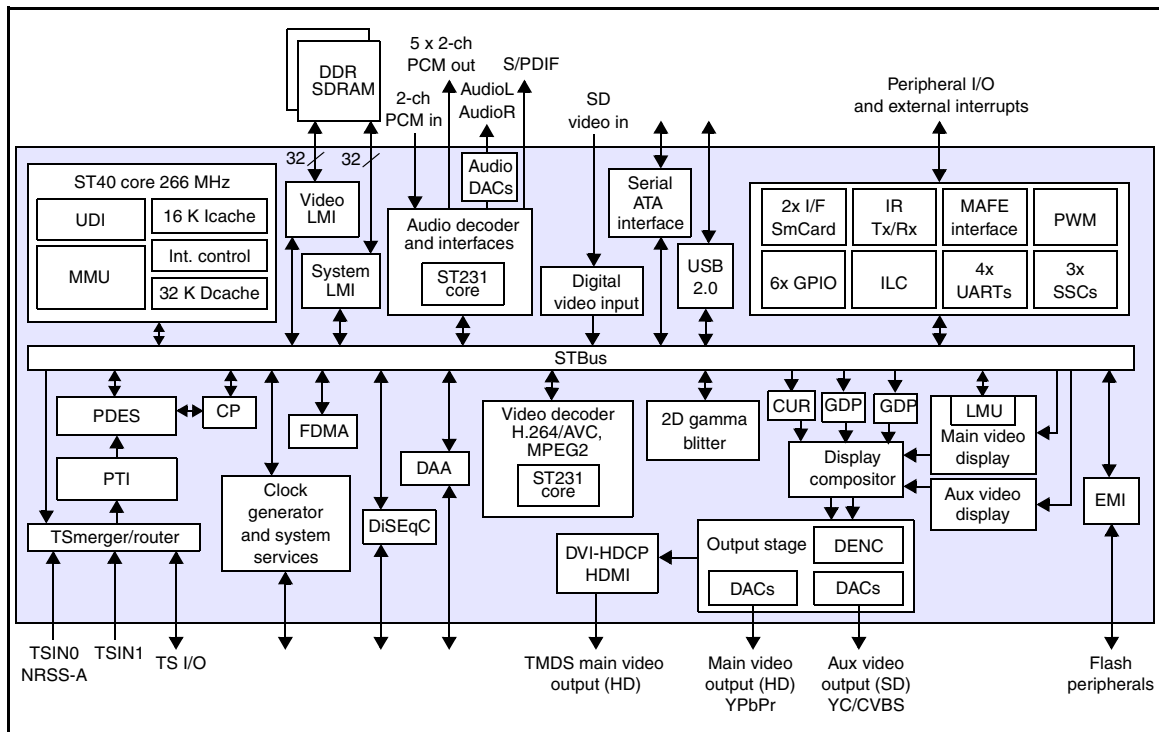


## Low cost HDTV set-top box decoder for H.264/AVC and MPEG-2

Data Brief

### Features

- The STi7100 is a single-chip, high-definition STB decoder including:
  - ST40 CPU core, 266 MHz
  - dual ST231 CPU cores for audio and video decoding, both 400 MHz
  - transport filtering and descrambling
  - video decoder: H.264/AVC and MPEG-2
  - graphics engine and dual display: high-definition (HD) and standard definition (SD)
  - audio decoder
- The STi7100 also features the following embedded interfaces:
  - USB 2.0
  - DVI/HDMI output
  - digital audio and video auxiliary input
  - modem
  - serial ATA



# 1 Description

The STi7100 is a new generation, high-definition set-top box decoder chip, and provides very high performance for low-cost HD systems. With enhanced performances over the STi7710, it includes an H.264/AVC decoder for new low-bitrate applications, as well as dual-decode MPEG-2 capability.

Based on the Omega2 (STBus) architecture, this system on chip is a full back-end processing solution for digital terrestrial, satellite and cable high-definition set-top boxes compliant with ATSC, DVB, DIRECTV, DCII, OpenCable and ARIB BS4 specifications.

The STi7100 demultiplexes, decrypts and decodes a single HD or SD video stream with associated multichannel audio. Video is output to two independently formatted displays: a full resolution display intended for a TV monitor, and a downsampled display intended for a VCR, or alternatively a second SD TV. Connection to a TV or display panel can be via an analog component interface or a copy protected DVI/HDMI interface. Composite outputs are provided for connection to the VCR with Macrovision protection. Audio is output with optional PCM mixing to an S/PDIF interface, PCM interface or via integrated stereo audio DACs.

Digitized analog programs can also be input to the STi7100 for reformatting and display.

The STi7100 includes a graphics rendering and display capability with a 2D graphics accelerator, two graphics planes and a cursor plane. A dual display compositor provides mixing of graphics and video with independent composition for each of the TV and VCR outputs.

The STi7100 includes a stream merger to allow five different transport streams from different sources to be merged and processed concurrently. Applications include DVR time shifted viewing of a terrestrial program while acquiring an EPG/data stream from a satellite or cable front end.

The flexible descrambling engine is compatible with required standards including DVB, DES, AES and Multi2.

The STi7100 embeds a 266 MHz ST40 CPU for applications and device control. A dual DDR1 SDRAM memory interface is used for higher performance, to allow the video decoder the required memory bandwidth for HD H.264 decoding and sufficient bandwidth for the CPU and the rest of the system. A second memory bus is also provided for flash memory storing resident software and for connection of peripherals.

A hard-disk drive (HDD) can be connected either to the serial ATA interface or as an expansion drive via the USB 2.0 port. The USB port can also be used to connect to a DOCSIS 2.0 CM gateway for interactive cable applications.

The STi7100 is supported by STMicroelectronics' STAPI software, and is compatible with several other related devices such as the STi7109.

Figure 1. Low-cost satellite HD set-top box

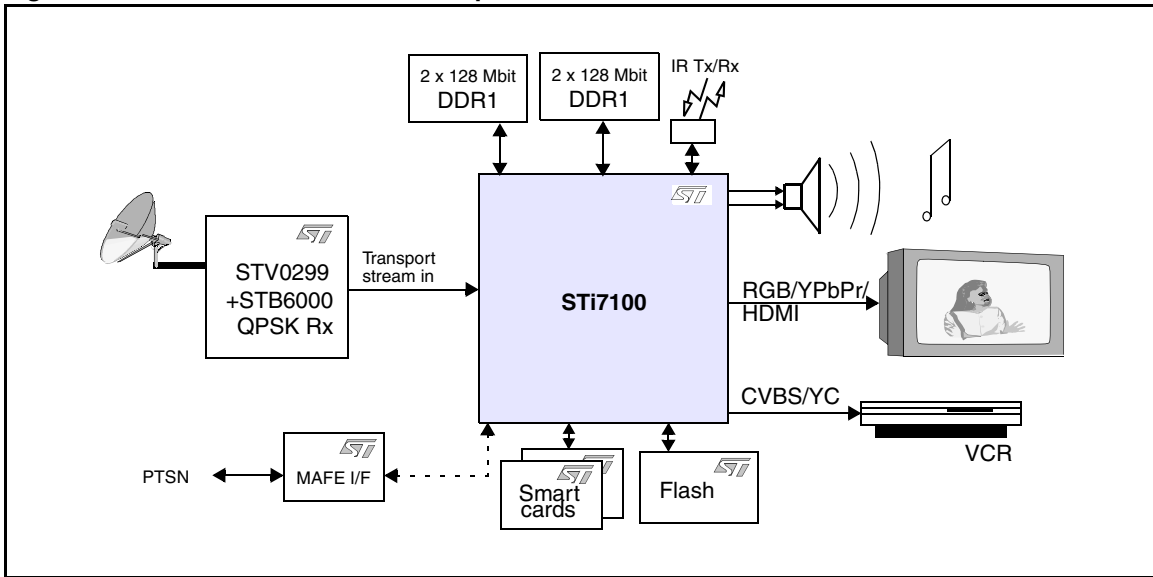


Figure 2. Low-cost cable HD set-top box with return channel

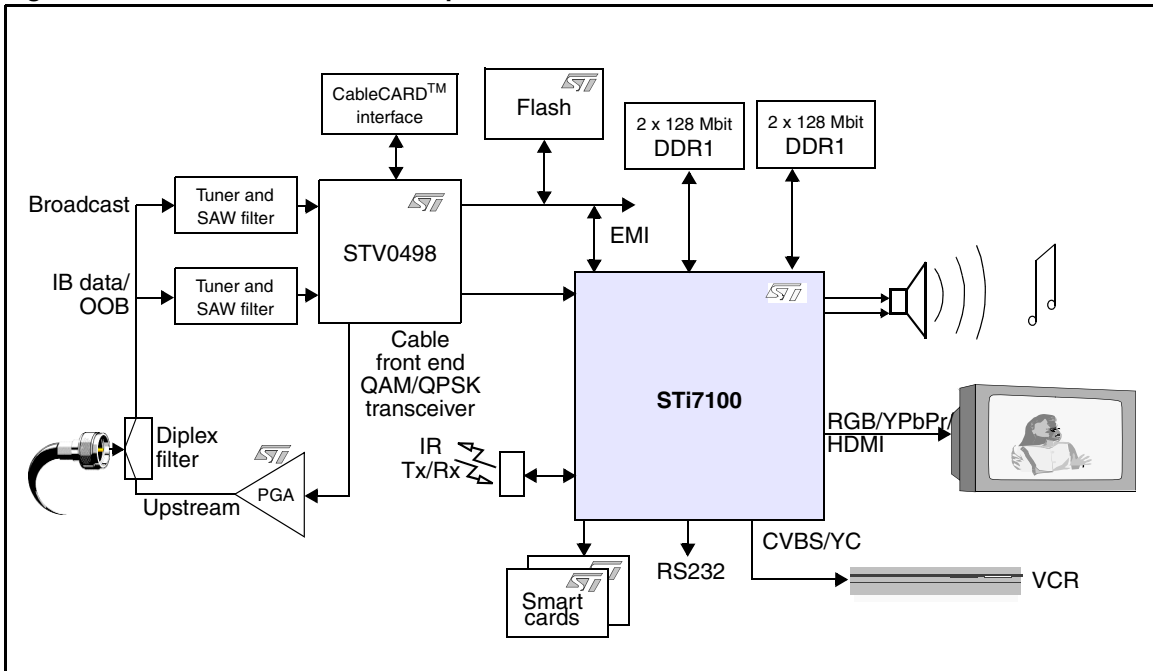


Figure 3. Low-cost dual satellite and terrestrial HD set-top box with HDD

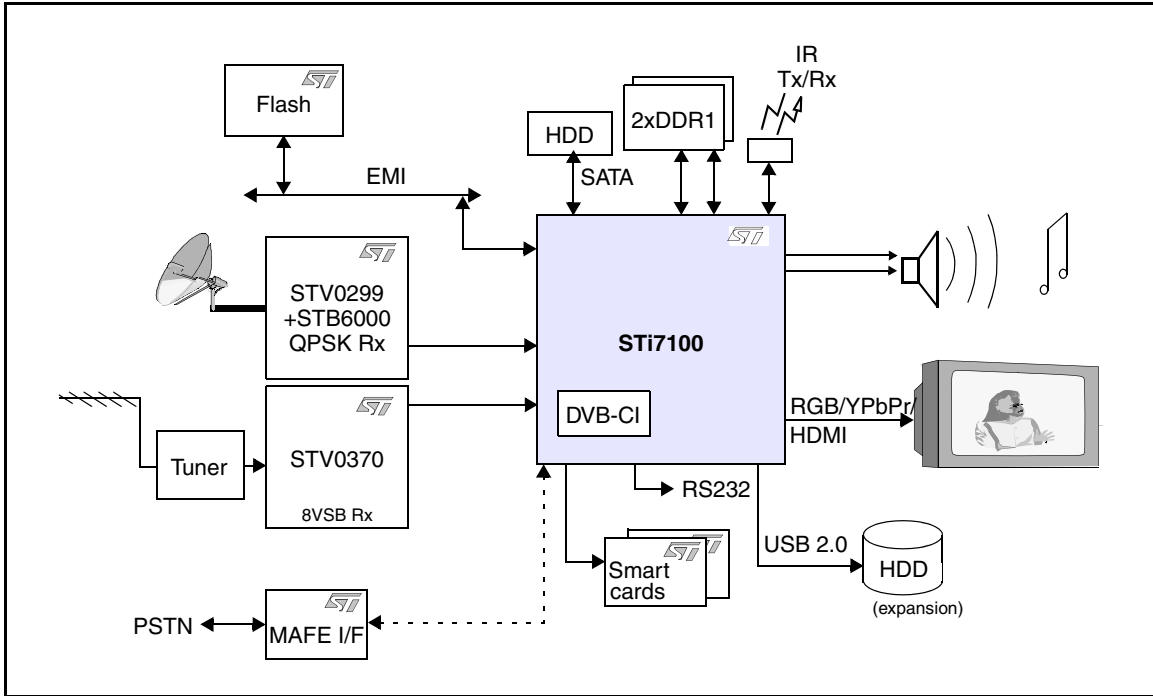
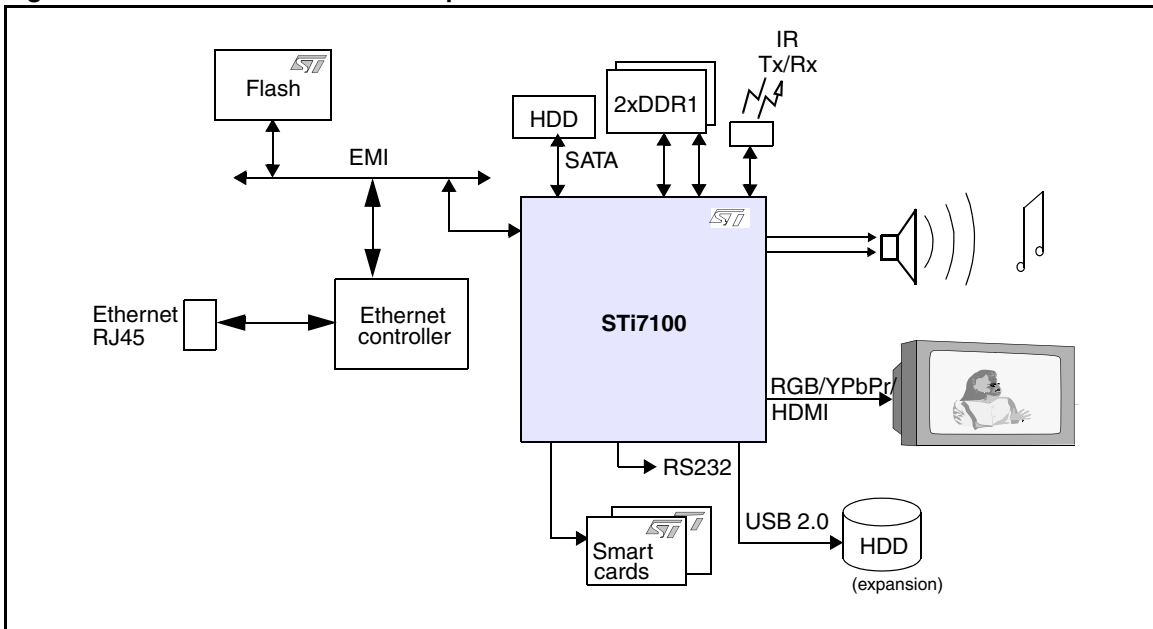


Figure 4. Low-cost HD IP-TV set-top box with HDD



## 1.1 Detailed features list

### 1.1.1 Processor subsystem

- ST40 32-bit superscalar RISC CPU
  - 266 MHz, 2-way set associative 16-Kbyte ICache, 32-Kbyte DCache, MMU
  - 5-stage pipeline, delayed branch support
  - floating point unit, matrix operation support
  - debug port, interrupt controller

### 1.1.2 Transport subsystem

- TS merger/router
  - 2 serial/parallel inputs
  - 1 bidirectional interface
  - merging of 3 transport streams
  - transport stream from memory support
  - NRSS-A module interface
  - TS routing for DVB-CI and CableCARD™ modules
- Programmable transport interface (PTI)
  - transport stream demux: DVB, DIRECTV®, ATSC, ARIB, OpenCable, DCII
  - integrated DES, AES, DVB, ICAM and Multi2 descramblers
  - NDS random access scrambled stream protocol (RASP) compliant
  - NDS ICAM CA
  - support for VGS, Passage and DVS042 residue handling

### 1.1.3 Video/graphics subsystem

- MPEG-4 AVC high profile level 4.1/ MPEG-2 MP@HL video decoder
  - hardware/firmware mixed architecture
  - advanced error concealment and trick mode support
  - dual MPEG-2 MP@HL decode
- SD (ITU-R BT 601/656) D1 digital video input
- Displays
  - HD display, multiformat capable (1080I, 720P, 480P/576P, 480I/576I)
    - Analog HD output RGB or YPbPr
    - HDMI encoded output
  - SD display
    - Analog SD output: YPbPr or YC and CVBS

- Gamma 2D/3D graphics processor
  - dual source blitter engine
  - alpha blending and logical operations
  - color space and format conversion
  - fast color fill
  - arbitrary resizing with high quality filters
  - acceleration of direct drawing by CPU
  - Gamma compositor and video processor
  - 5 channels mixer for HD output
  - independent 2-channel mixer for SD output
  - 2 graphic display planes
  - high-quality video scaler
  - picture up-conversion hardware
  - linear resizing and format conversions
  - horizontal and vertical filtering
- Copy protection
  - HDMI 1.0/HDCP 1.1 copy protection hardware
  - Macrovision™ copy protection for 480I, 480P, 576I, 576P outputs

#### 1.1.4 Audio subsystem

- Digital audio decoder
  - compatible with all popular audio standards
  - PCM mixing with internal or external source and sample rate conversion
  - independent multichannel PCM output, S/PDIF output and analog output
  - 6 to 2 channel downmixing
  - PCM audio input
- Stereo 24-bit audio DAC for analog output
- IEC958/IEC1937 digital audio output interface (S/PDIF)

#### 1.1.5 Interfaces

- External memory interface (EMI)
  - 16-bit interface supporting ROM, Flash, SFlash, SRAM, peripherals
  - access in 5 banks
  - master/slave support for interconnecting two STi7100 devices
- Dual local memory interface (LMI)
  - dual interface for 32-bit DDR1 200-MHz (DDR400) memories, supports 64, 128, 256 and 512 Mbit devices
- USB 2.0 host interface
- Serial ATA hard-disk drive support
  - record and playback with trick modes
  - pause and time shifting
  - watch and record

- On-chip peripherals
  - 4 ASCs (UARTs) with Tx and Rx FIFOS, two of which can be used in smartcard interfaces
  - 2 smartcard interfaces and clock generators (improved to reduce external circuitry)
  - 3 SSCs for I<sup>2</sup>C/SPI master slaves interfaces
  - serial communications interface (SCIF)
  - 2 PWM outputs
  - PWM capture/compare functions
  - teletext serializer and DMA module
  - 6 banks of general purpose I/O, 3.3 V tolerant
  - SiLabs line-side (DAA) interface
  - Modem analog front end (MAFE/DAA) interface
  - infrared transmitter/receiver supporting RC5, RC6 and RECS80 codes
  - UHF remote receiver input interface
  - interrupt level controller and external interrupts, 3.3 V tolerant
  - low power/RTC/watchdog controller
  - integrated VCXO
  - DiSEqC™ 2.0 interface
- Flexible multichannel DMA

### 1.1.6 Services and package

- JTAG/TAP interface
- ST40 and ST231 toolset support
- 35 x 35 PGBA package, 580+100 balls

## 2 Revision history

Table 1. Document revision history

Date	Revision	Changes
19-Dec-2006	2	Rewritten to include latest information and corrected product code.
10-Dec-2004	1	Initial release.



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