

# Thyristors logic level

## BT258U series

### GENERAL DESCRIPTION

Passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

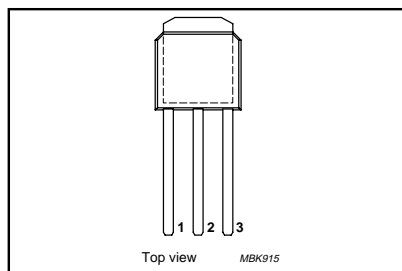
### QUICK REFERENCE DATA

| SYMBOL                   | PARAMETER                            | MAX.               | MAX.               | MAX.               | UNIT |
|--------------------------|--------------------------------------|--------------------|--------------------|--------------------|------|
| $V_{DRM}$ ,<br>$V_{RRM}$ | Repetitive peak off-state voltages   | <b>500R</b><br>500 | <b>600R</b><br>600 | <b>800R</b><br>800 | V    |
| $I_{T(AV)}$              | Average on-state current             | 5                  | 5                  | 5                  | A    |
| $I_{T(RMS)}$             | RMS on-state current                 | 8                  | 8                  | 8                  | A    |
| $I_{TSM}$                | Non-repetitive peak on-state current | 75                 | 75                 | 75                 | A    |

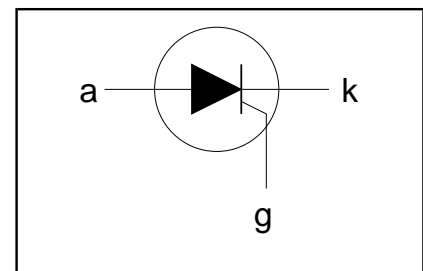
### PINNING - SOT533

| PIN NUMBER | DESCRIPTION |
|------------|-------------|
| 1          | cathode     |
| 2          | anode       |
| 3          | gate        |
| tab        | anode       |

### PIN CONFIGURATION



### SYMBOL



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL                | PARAMETER  | CONDITIONS  | MIN. | MAX.                      |                           |              | UNIT             |
|-----------------------|--|---|------|---------------------------|---------------------------|--------------|------------------|
|                       |  |   |      | -500R<br>500 <sup>1</sup> | -600R<br>600 <sup>1</sup> | -800R<br>800 |                  |
| $V_{DRM}$ , $V_{RRM}$ | Repetitive peak off-state voltages                           |   | -    |                           |                           |              | V                |
| $I_{T(AV)}$           | Average on-state current                                     | half sine wave; $T_{mb} \leq 111$ °C                        | -    | 5                         |                           |              | A                |
| $I_{T(RMS)}$          | RMS on-state current   | all conduction angles                                       | -    | 8                         |                           |              | A                |
| $I_{TSM}$             | Non-repetitive peak on-state current                         | half sine wave; $T_j = 25$ °C prior to surge<br>$t = 10$ ms | -    | 75                        |                           |              | A                |
| $I^2t$                | $I^2t$ for fusing  | $t = 8.3$ ms  | -    | 82                        |                           |              | A <sup>2</sup>   |
| $dl_T/dt$             | Repetitive rate of rise of on-state current after triggering | $t = 10$ ms   | -    | 28                        |                           |              | A <sup>2</sup> s |
| $I_{GM}$              | Peak gate current  | $I_{TM} = 10$ A; $I_G = 50$ mA;                             | -    | 50                        |                           |              | A/ $\mu$ s       |
| $V_{GM}$              | Peak gate voltage  | $dl_G/dt = 50$ mA/ $\mu$ s                                  | -    | 2                         |                           |              | A                |
| $V_{RGM}$             | Peak reverse gate voltage                                    |   | -    | 5                         |                           |              | V                |
| $P_{GM}$              | Peak gate power  |   | -    | 5                         |                           |              | W                |
| $P_{G(AV)}$           | Average gate power   | over any 20 ms period                                       | -    | 0.5                       |                           |              | W                |
| $T_{stg}$             | Storage temperature  |   | -40  | 150                       |                           |              | °C               |
| $T_j$                 | Operating junction temperature                               |   | -    | 125 <sup>2</sup>          |                           |              | °C               |

<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu$ s.

<sup>2</sup> Note: Operation above 110 °C may require the use of a gate to cathode resistor of 1k $\Omega$  or less.

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**THERMAL RESISTANCES**

| SYMBOL         | PARAMETER                                    | CONDITIONS  | MIN. | TYP. | MAX. | UNIT |
|----------------|--|-------------|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | in free air | -    | -    | 2.0  | K/W  |
| $R_{th\ j-a}$  | Thermal resistance junction to ambient       |             | -    | 70   | -    | K/W  |

**STATIC CHARACTERISTICS** $T_j = 25\text{ °C}$  unless otherwise stated

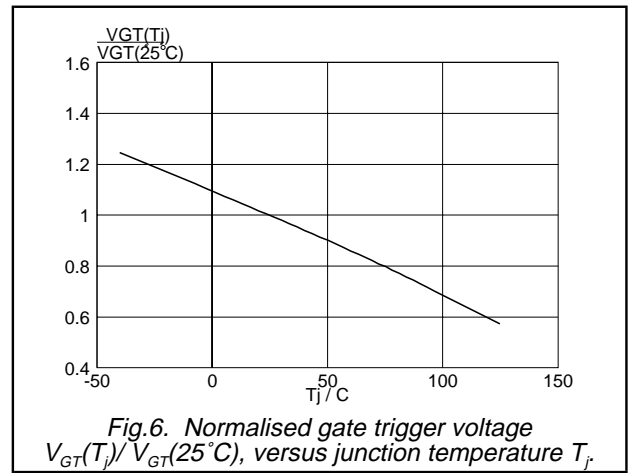
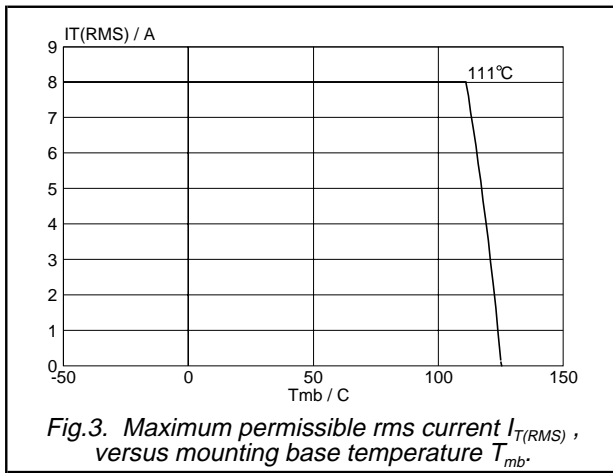
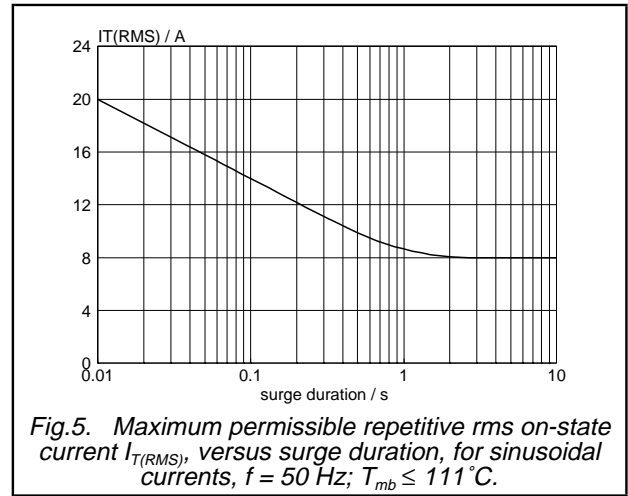
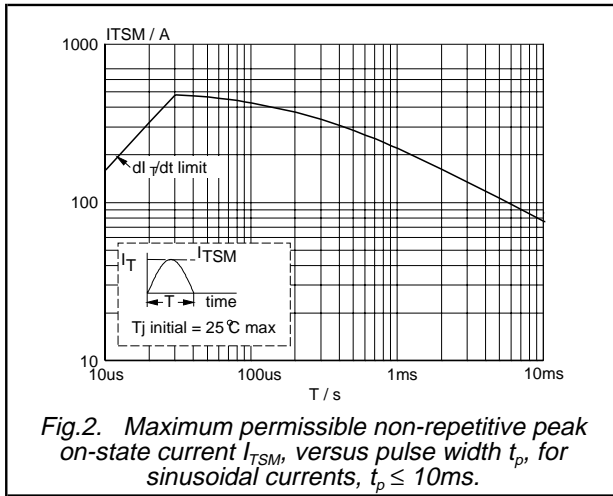
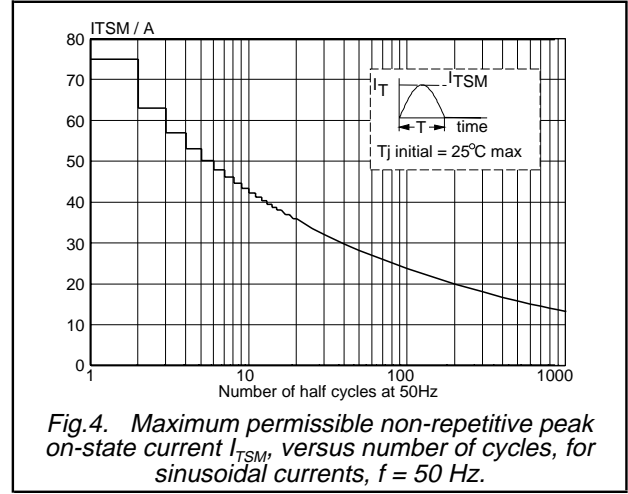
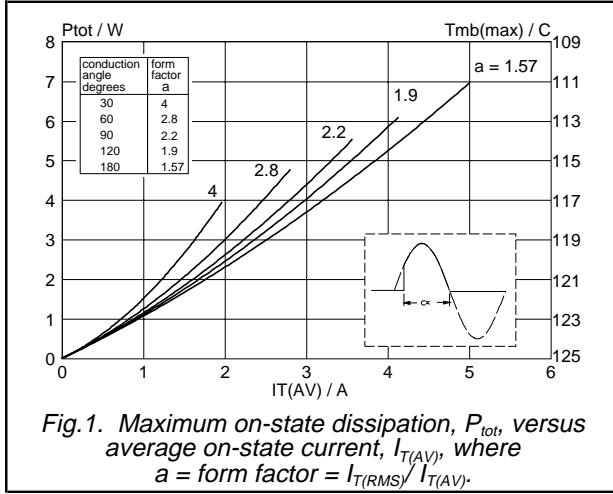
| SYMBOL     | PARAMETER                 | CONDITIONS  | MIN. | TYP. | MAX. | UNIT          |
|------------|---------------------------|---|------|------|------|---------------|
| $I_{GT}$   | Gate trigger current      | $V_D = 12\text{ V}; I_T = 0.1\text{ A}$                       | -    | 50   | 200  | $\mu\text{A}$ |
| $I_L$      | Latching current          | $V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$                    | -    | 0.4  | 10   | mA            |
| $I_H$      | Holding current           | $V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$                    | -    | 0.3  | 6    | mA            |
| $V_T$      | On-state voltage          | $I_T = 16\text{ A}$   | -    | 1.3  | 1.5  | V             |
| $V_{GT}$   | Gate trigger voltage      | $V_D = 12\text{ V}; I_T = 0.1\text{ A}$                       | -    | 0.4  | 1.5  | V             |
| $I_D, I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}; I_T = 0.1\text{ A}; T_j = 110\text{ °C}$ | 0.1  | 0.2  | -    | V             |
|            |                           | $V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125\text{ °C}$ | -    | 0.1  | 0.5  | mA            |

**DYNAMIC CHARACTERISTICS** $T_j = 25\text{ °C}$  unless otherwise stated

| SYMBOL    | PARAMETER                                  | CONDITIONS   | MIN. | TYP. | MAX. | UNIT             |
|-----------|--|--|------|------|------|------------------|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$<br>exponential waveform; $R_{GK} = 100\ \Omega$   | 50   | 100  | -    | V/ $\mu\text{s}$ |
| $t_{gt}$  | Gate controlled turn-on time               | $I_{TM} = 10\text{ A}; V_D = V_{DRM(max)}; I_G = 5\text{ mA};$<br>$dI_G/dt = 0.2\text{ A}/\mu\text{s}$   | -    | 2    | -    | $\mu\text{s}$    |
| $t_q$     | Circuit commutated turn-off time           | $V_D = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$<br>$I_{TM} = 12\text{ A}; V_R = 24\text{ V}; dI_{TM}/dt = 10\text{ A}/\mu\text{s};$<br>$dV_D/dt = 2\text{ V}/\mu\text{s}; R_{GK} = 1\text{ k}\Omega$ | -    | 100  | -    | $\mu\text{s}$    |

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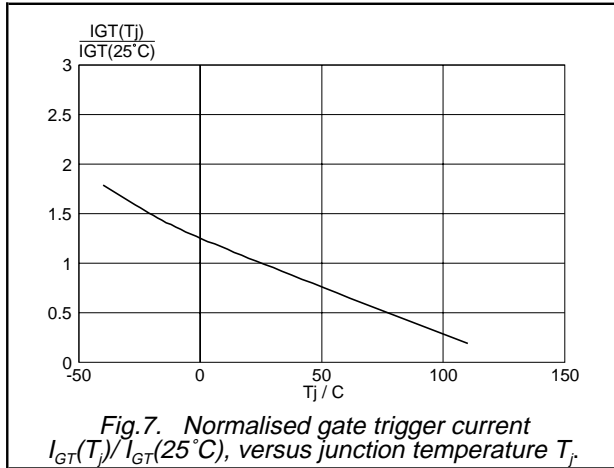


Fig. 7. Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

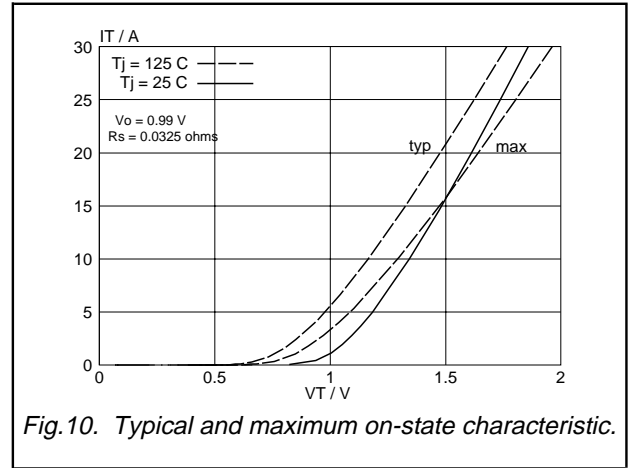


Fig. 10. Typical and maximum on-state characteristic.

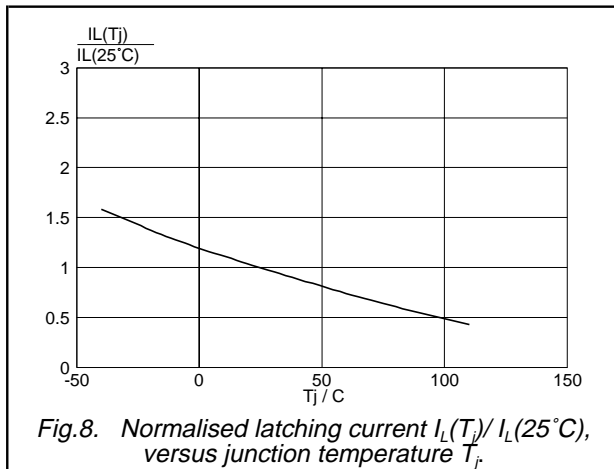


Fig. 8. Normalised latching current  $I_L(T_j)/I_L(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

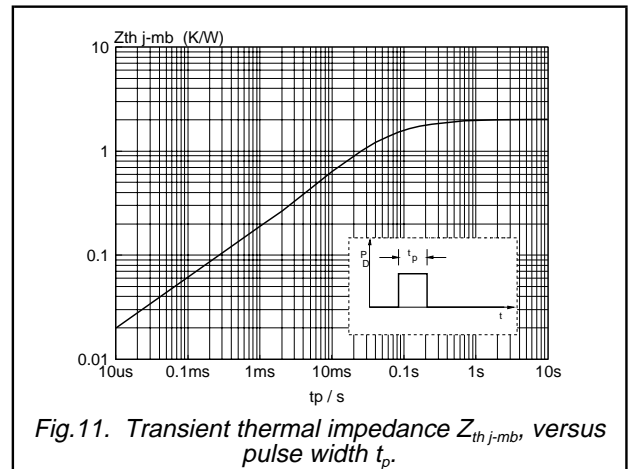


Fig. 11. Transient thermal impedance  $Z_{th \text{ j-mb}}$ , versus pulse width  $t_p$ .

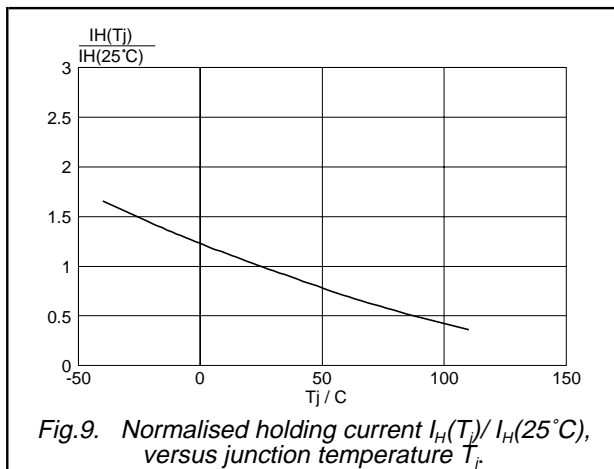


Fig. 9. Normalised holding current  $I_H(T_j)/I_H(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

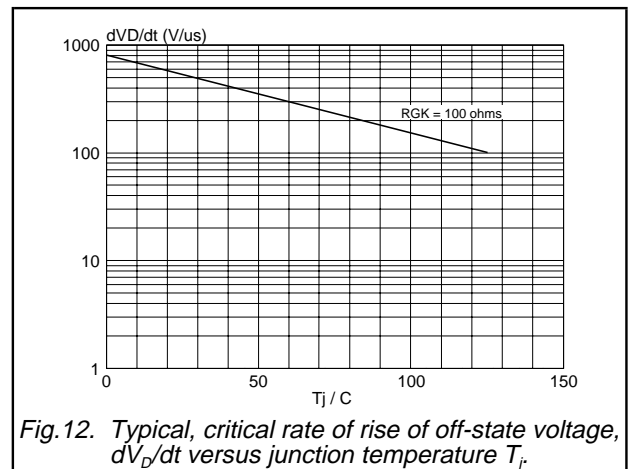


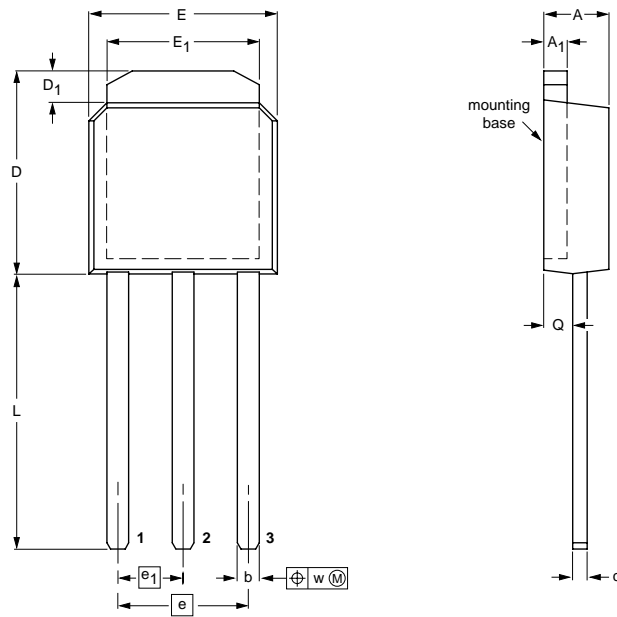
Fig. 12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  versus junction temperature  $T_j$ .

**MECHANICAL DATA**

Dimensions in mm Net Mass: 1.3 g

Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line)

SOT533



DIMENSIONS (mm are the original dimensions)

| UNIT | A            | A <sub>1</sub> | b            | c            | D            | D <sub>1</sub> | E            | E <sub>1</sub> | e    | e <sub>1</sub> | L          | Q            |
|------|--------------|----------------|--------------|--------------|--------------|----------------|--------------|----------------|------|----------------|------------|--------------|
| mm   | 2.38<br>2.22 | 0.89<br>0.71   | 0.89<br>0.71 | 0.56<br>0.46 | 7.28<br>6.94 | 1.06<br>0.96   | 6.73<br>6.47 | 5.36<br>5.26   | 4.57 | 2.285          | 9.8<br>9.4 | 1.00<br>1.10 |

| OUTLINE VERSION | REFERENCES |        |      |  | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|------------|
|                 | IEC        | JEDEC  | EIAJ |  |                     |            |
| SOT533          |            | TO-251 |      |  |                     | 99-02-18   |

Fig.13. SOT533 (TO251). pin 2 connected to mounting base.

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**BT258U series****DEFINITIONS**

|  |   |
|--|---|
| <b>Data sheet status</b>   |   |
| Objective specification  | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification  | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification  | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>   |   |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>   |   |
| Where application information is given, it is advisory and does not form part of the specification.  |   |
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