MCRF202

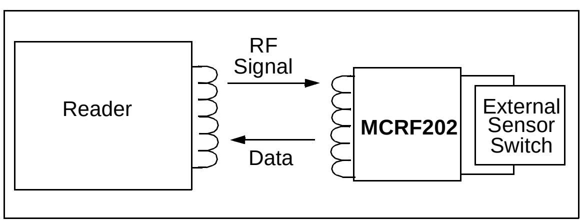
125 kHz Passive RFID Device with Sensor Input

Features

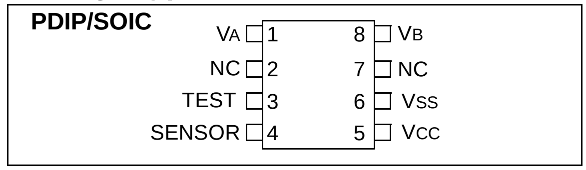
- External sensor input
- Data polarity changes with sensor input condition
- Read-only data transmission
- 96- or 128-bits of factory programming user memory (also supports 48- and 64-bit protocols)
- Operates up to 400 kHz carrier frequency
- Low-power operation
- Modulation options:
  - ASK, FSK, PSK
- Data Encoding options:
  - NRZ Direct, Differential Biphase Manchester Biphase
- Die, Wafer, PDIP or SOIC package option
- Factory programming and device serialization

Applications

- Insect control
- Industrial tagging



Package Type



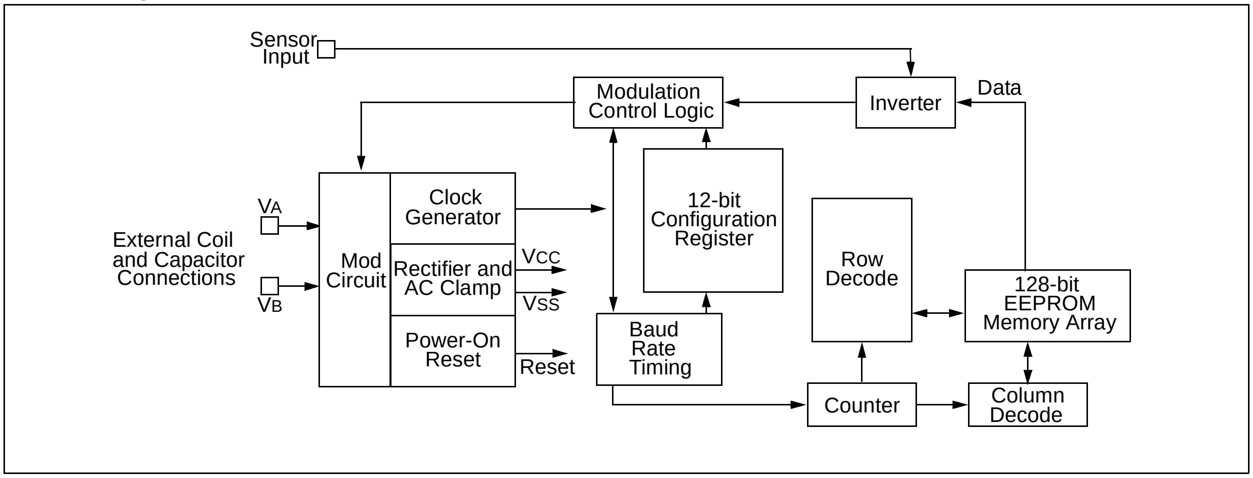
Description

The MCRF202 is a passive Radio Frequency Identification (RFID) device that provides an RF interface for reading the contents of a user memory array. This device is specially designed to detect the logic state of an external sensor, and alters its data transmissions, based on the condition of the sensor input. The device outputs a normal bit data stream if the sensor input has a logic '1' state, but outputs an inverted data stream for a logic '0' state. In this way, the reader can monitor the state (condition) of the external sensor input by detecting whether the data from the device is a normal or inverted data stream.

The device is powered by rectifying the incoming RF carrier signal that is transmitted from the reader. When the device develops sufficient DC voltage, it transmits the contents of its memory array by modulating the incoming RF carrier signal. The reader is able to detect the modulation and decodes the data being transmitted. Code length, modulation option, encoding option, and bit rate are set at the factory to fit the needs of particular applications.

The MCRF202 is available in die, wafer, PDIP and SOIC packages. The encoding, modulation, bit rate options, and data fields are specified by the customer and programmed by Microchip Technology Inc. prior to shipment. See Technical Bulletin TB023 for more information on factory serialization (SQTP™).

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings(†)

Storage temperature ....- 65°C to +150°C

Ambient temperature with power applied...-40°C to +125°C

Maximum current into coil pads ....50 mA

† **NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: AC AND DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Industrial (I): T_A = -40°C to +85°C					
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Clock frequency	F_{CLK}	100	—	400	kHz	
Data retention		200	—	—	Years	25°C
Coil current (Dynamic)	I_{CD}	—	50	—	µA	
Operating current with no V_{CC} load	I_{DD}	—	5	—	µA	V_{CC} = 2V No load to V_{CC} pad
Operating current with V_{CC} load	I_{DL}	—	10	—	µA	V_{CC} = 2V V_{CC} load through switch to sensor
Turn-on-voltage (Dynamic) for modulation	V_AV_B V_{CC}	10 2	— —	— —	V_{PP} V_{DC}	
Input Capacitance	C_{IN}	—	2	—	pF	Between V_A and V_B
SENSOR pull-down	R_S	400	800	1200	kΩ	
SENSOR trigger threshold	V_S	0.5	1.0	1.5	V	

2.0 FUNCTIONAL DESCRIPTION

The device contains three major building blocks. They are RF front-end and sensor input, configuration and control logic, and memory sections. The Block Diagram is shown on page 1.

2.1 RF Front-End and Sensor Input

The RF front-end of the device includes circuits for rectification of the carrier, VDD (operating voltage), and high-voltage clamping to prevent excessive voltage from being applied to the device. This section also generates a system clock from the incoming carrier signal and modulates the carrier signal to transmit data to the reader.

2.1.1 RECTIFIER – AC CLAMP

The AC voltage generated by the external tuned LC circuit is full wave rectified. This unregulated voltage is used as the maximum DC supply voltage for the rest of the device and for the VCC supply to the external sensor or switch. Any excessive voltage on the tuned circuit is clamped by the internal circuitry to a safe level to prevent damage to the IC.

2.1.2 MODULATION CIRCUIT

The MCRF202 sends the encoded data to the reader by AM-modulating the coil voltage across the tuned LC circuit. A modulation transistor is placed between the antenna coil pads (VA and VB). The transistor turns on and off based on the modulation signal. As a result, the amplitude of the antenna coil voltage varies with the modulation signal. See Figure 2-1 for details.

2.1.3 VCC REGULATOR

The device generates a DC supply voltage from the unregulated coil voltage. The Vcc pin can be used to power a separate low-current device (read range will be affected).

2.1.4 CLOCK GENERATOR

This circuit generates a clock based on the carrier frequency from the reader. This clock is used to derive all timing in the MCRF202, including the baud rate and modulation rate.

2.1.5 POWER-ON RESET

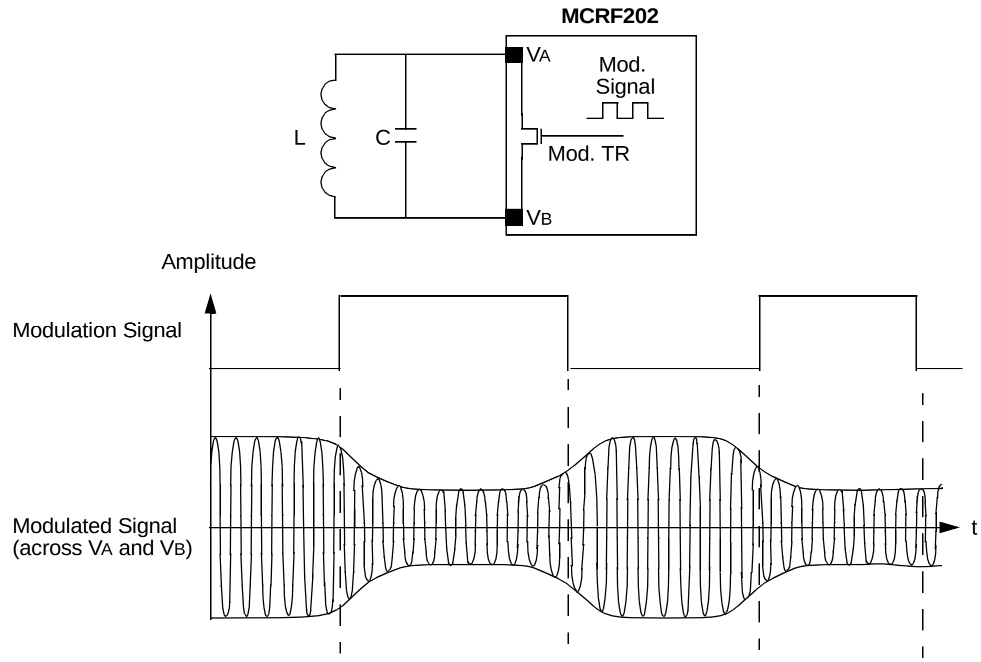
This circuit generates a Power-on Reset when the tag first enters the interrogator field. The Reset releases when sufficient power has developed on the VDD regulator to allow correct operation.

2.1.6 SENSOR INPUT AND DATA INVERTER

The SENSOR input responds to logic high or logic low voltages to drive the internal inverter on or off. A logic high results in normal tag operation; a logic low at SENSOR input activates an inverter, which inverts the entire data stream prior to modulation.

The SENSOR input has an internal pull-down resistor of 800 kΩ (typical). See Figure 2-4 for application details.

FIGURE 2-1: MODULATION SIGNAL AND MODULATED SIGNAL



2.2 Configuration Register and Control Logic

The configuration register determines the operational parameters of the device. It directly controls logic blocks which generate the baud rate, memory size, encoded data, modulation protocol, etc. CB11 is always a zero. Once the array is successfully programmed at the factory, the lock bit CB12 is set. When the lock bit is set, programming and erasing the device becomes permanently disabled. Table 2-1 contains a description of the control register bit functions.

2.2.1 BAUD RATE TIMING OPTION

The chip will access data at a baud rate determined by bits CB2, CB3, and CB4 of the configuration register. For example, MOD32 (CB2 = 0, CB3 = 1, CB4 = 1) has 32 RF cycles per bit. This gives the data rate of 4 kHz for the RF carrier frequency of 128 kHz.

2.2.2 DATA ENCODING OPTION

This logic acts upon the serial data being read from the EEPROM. The logic encodes the data according to the configuration bits CB6 and CB7. CB6 and CB7 determine the data encoding method. The available choices are:

- Non-return to zero-level (NRZ_L)
- Biphase_S (Differential)
- Biphase_L (Manchester)
- Inverted Manchester

2.2.3 MODULATION OPTION

CB8 and CB9 determine the modulation protocol of the encoded data. The available choices are:

- ASK
- FSK
- PSK_1
- PSK_2

When ASK (direct) option is chosen, the encoded data is fed into the modulation transistor without change.

When FSK option is chosen, the encoded data is represented by:

a) Sets of 10 RF carrier cycles (first 5 cycles → higher amplitude, the last 5 cycles → lower amplitude) for logic “high” level.

b) Sets of 8 RF carrier cycles (first 4 cycles → higher amplitude, the last 4 cycles → lower amplitude) for logic “low” level.

For example, FSK signal for MOD40 is represented:

a) 4 sets of 10 RF carrier cycles for data ‘1’.

b) 5 sets of 8 RF carrier cycles for data ‘0’.

Refer to Figure 2-2 for the FSK signal with MOD40 option.

The PSK_1 represents change in the phase of the modulation signal at the change of the encoded data. For example, the phase changes when the encoded data is changed from ‘1’ to ‘0’, or from ‘0’ to ‘1’.

The PSK_2 represents change in the phase at the change on ‘1’. For example, the phase changes when the encoded data is changed from ‘0’ to ‘1’, or from ‘1’ to ‘1’.

FIGURE 2-2: ENCODED DATA AND FSK OUTPUT SIGNAL FOR MOD40 OPTION

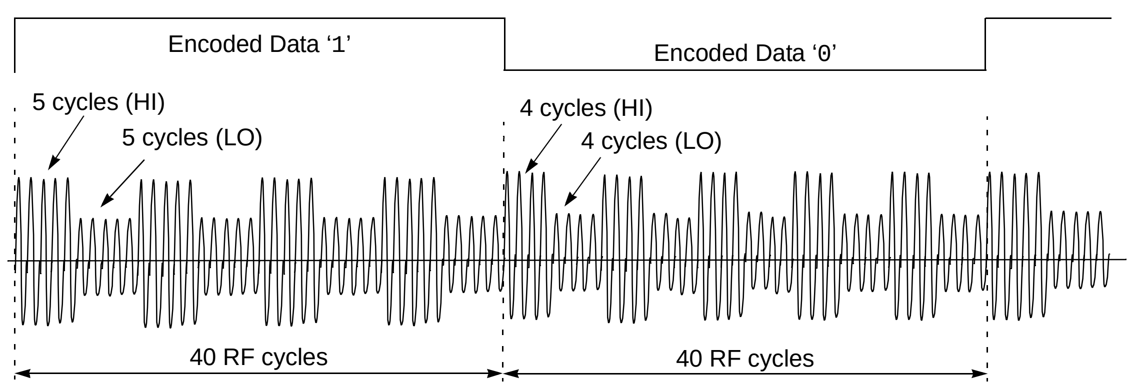
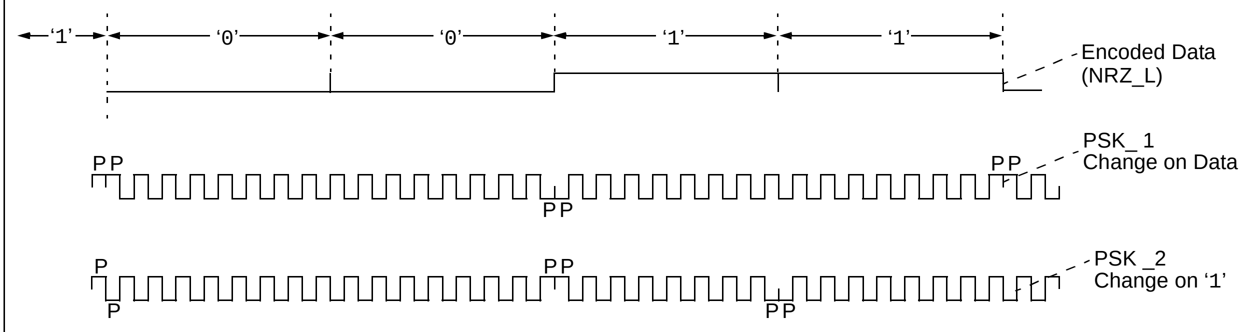


FIGURE 2-3: PSK DATA MODULATION



2.2.4 MEMORY ARRAY LOCK BIT (CB12)

The CB12 bit must be a ‘1’ for a factory programmed device.

2.3 Memory Section

The device has 128 bits of one-time programmable (OTP) memory. The user can choose 96 or 128 bits by selecting the CB1 bit in the configuration register. See Table 2-1 for more details.

2.3.1 COLUMN AND ROW DECODER LOGIC AND BIT COUNTER

The column and row decoders address the EEPROM array at the clock rate and generate a serial data stream for modulation. This data stream can be up to 128 bits in length. The size of the data stream is user programmable with CB1 and can be set to 96 or 128 bits. Data lengths of 48 and 64 bits are available by programming the data twice in the array, end-to-end.

The column and row decoders route the proper voltage to the array for programming and reading. In the programming modes, each individual bit is addressed serially from bit 1 to bit 128.

2.4 Examples of Configuration Settings

EXAMPLE 2-1: “88D” CONFIGURATION

The “88D” (hex) configuration is interpreted as follows:

```
            CB12                CB1
             |                   |
“88D” → 1000-1000-1101
```

Referring to Table 2-1, the “88D” configuration represents:

Modulation = PSK_1
PSK rate = rf/2
Data encoding = NRZ_L (direct)
Baud rate = rf/32 = MOD32
Memory size: 128 bits
Programmed device

EXAMPLE 2-2: “80A” CONFIGURATION

The “80A” (hex) configuration is interpreted as follows:

```
            CB12                CB1
             |                   |
“80A” → 1000-0000-1010
```

The MSB corresponds to CB12 and the LSB corresponds to CB1 of the configuration register. Therefore, we have:

CB12=1	CB11=0	CB10=0	CB9=0
CB8=0	CB7=0	CB6=0	CB5=0
CB4=1	CB3=0	CB2=1	CB1=0

Referring to Table 2-1, the “80A” configuration represents:

Programmed device, FSK protocol, NRZ_L (direct) encoding, MOD50 (baud rate = rf/50), 96 bits.

TABLE 2-1: CONFIGURATION REGISTER

CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1

ARRAY SIZE

CB1 = 1 128-bit user array
CB1 = 0 96-bit user array

TIMING

CB2	CB3	CB4	Rate
0	0	0	MOD128
0	0	1	MOD100
0	1	0	MOD80
0	1	1	MOD32
1	0	0	MOD64
1	0	1	MOD50
1	1	0	MOD40
1	1	1	MOD16

NOT USED

CB5 = 0

DATA ENCODING

CB6 = 0; CB7 = 0 NRZ_L (Direct)
CB6 = 0; CB7 = 1 Biphase_S (Differential)
CB6 = 1; CB7 = 0 Biphase_L (Manchester)
CB6 = 1; CB7 = 1 (Inverted Manchester)

MODULATION OPTIONS

CB8 = 0; CB9 = 0 FSK 0 = Fc/8, 1 = Fc/10
CB8 = 0; CB9 = 1 Direct
CB8 = 1; CB9 = 0 PSK_1
(phase change on change of data)
CB8 = 1; CB9 = 1 PSK_2
(phase change at beginning of a one)

PSK RATE OPTION

CB10 = 1 clk/4 carrier
CB10 = 0 clk/2 carrier

(NOT USED)

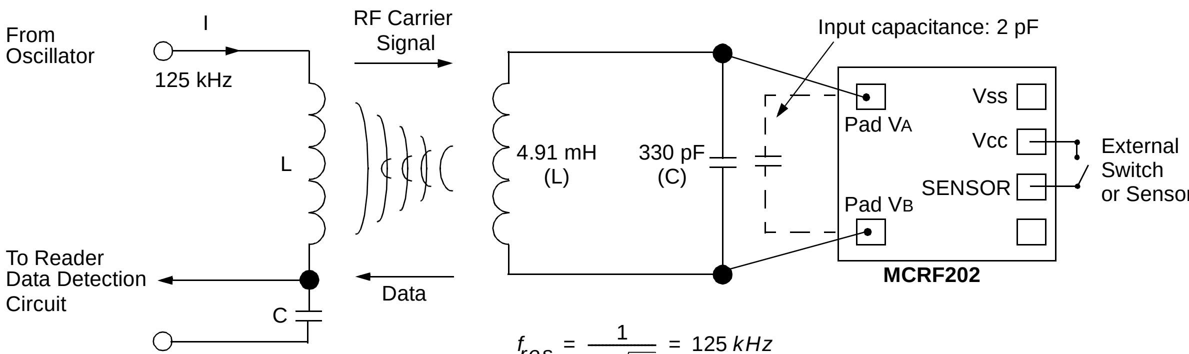
CB11 = 0

ARRAY LOCK BIT

CB12 = 1

FIGURE 2-4: TYPICAL APPLICATION CIRCUITS

Using MCRF202 with an external passive switch or sensor



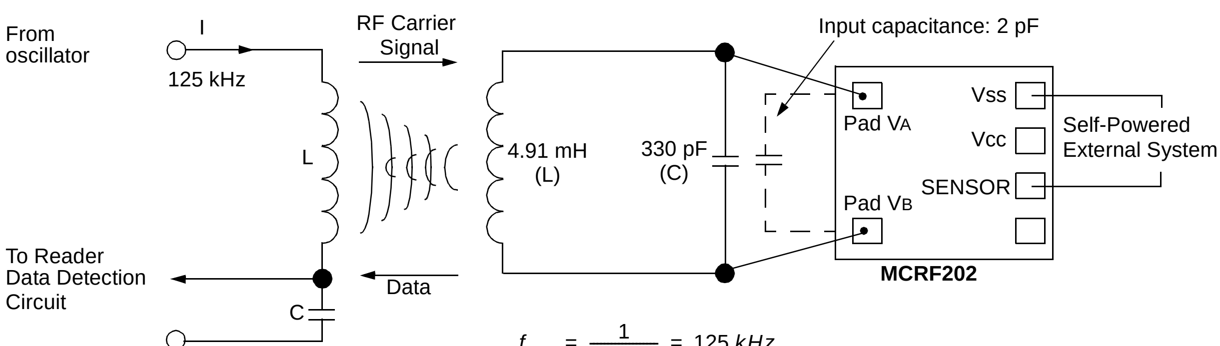
$$f_{res} = \frac{1}{2\pi\sqrt{LC}} = 125\ kHz$$

Device Output

External Switch CLOSED (Logic “1” in SENSOR Input): Normal Data Stream

External Switch OPEN (Logic “0” in SENSOR Input): Inverted Data Stream

Using MCRF202 with an external, self-powered system



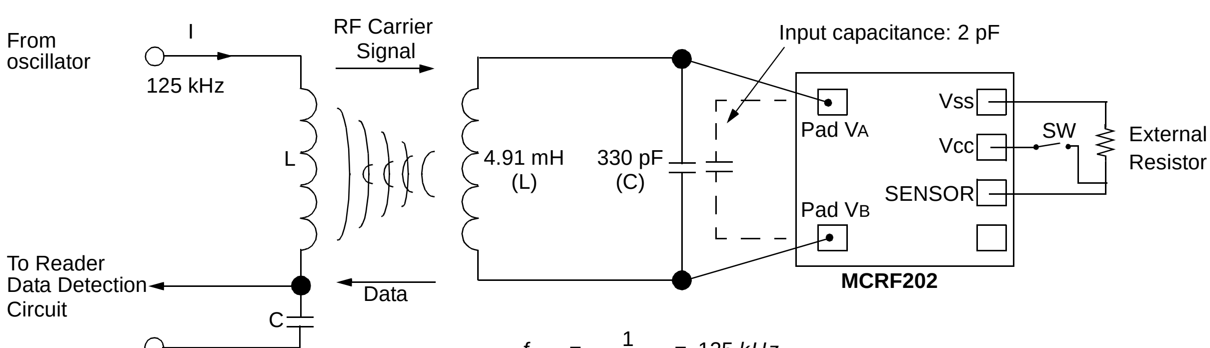
$$f_{res} = \frac{1}{2\pi\sqrt{LC}} = 125\ kHz$$

Device Output

Logic “1” in SENSOR Input: Normal Data Stream

Logic “0” in SENSOR Input: Inverted Data Stream

Using MCRF202 with a low-resistance pull-down



$$f_{res} = \frac{1}{2\pi\sqrt{LC}} = 125\ kHz$$

Device Output

External Switch CLOSED (Logic “1” in SENSOR Input): Normal Data Stream

External Switch OPEN (Logic “0” in SENSOR Input): Inverted Data Stream

3.0 MECHANICAL SPECIFICATIONS FOR DIE AND WAFER

FIGURE 3-1: DIE PLOT

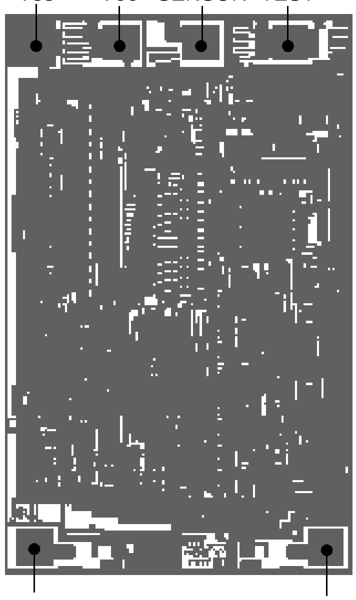


TABLE 3-1: PAD COORDINATES (μM)

Pad Name	Passivation Openings		Pad Center X	Pad Center Y
	Pad Width	Pad Height		
VA	90.0	90.0	427.50	-734.17
VB	90.0	90.0	-408.60	-734.17
VSS	105.3	112.5	-417.60	722.47
VCC	90.0	90.0	-164.70	723.82
SENSOR	90.0	90.0	69.30	723.82
TEST	90.0	90.0	325.35	723.82

Note 1: All coordinates are referenced from the center of the die.

2: Die size: 1.1215 mm x 1.7384 mm.

TABLE 3-2: PAD FUNCTION TABLE

Name	Function
VA, VB	Coil and capacitor connections
VSS	Device ground
VCC	DC supply out from device
SENSOR	Sensor input
TEST	Do Not Connect, Test pin

TABLE 3-3: DIE MECHANICAL DIMENSIONS

Specifications	Min	Typ	Max	Unit	Comments
Bond pad opening	— —	3.5 x 3.5 89 x 89	— —	mil µm	**Note 1**, **Note 2**
Die backgrind thickness	— —	7 177.8	— —	mil µm	Sawed 6” wafer on frame (option = WF) **Note 3**
	— —	11 279.4	— —	mil µm	Unsawed wafer (option = W) **Note 3**
Die backgrind thickness tolerance	— —	— —	±1 ±25.4	mil µm	
Die passivation thickness (multilayer)	—	0.9050	—	µm	**Note 4**
Die Size: Die size X*Y before saw (step size) Die size X*Y after saw	 — —	 44.15 x 68.44 42.58 x 66.87	 — —	 mil mil	 — —

Note 1: The bond pad size is that of the passivation opening. The metal overlaps the bond pad passivation by at least 0.1 mil.

2: Metal Pad Composition is 98.5% Aluminum with 1% Si and 0.5% Cu.

3: As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow.

4: The Die Passivation thickness can vary by device depending on the mask set used:

- Layer 1: Oxide (undopped oxide 0.135 µm)
- Layer 2: PSG (dopped oxide, 0.43 µm)
- Layer 3: Oxynitride (top layer, 0.34 µm)

5: The conversion rate is 25.4 µm/mil.

Notice: Extreme care is urged in the handling and assembly of die products since they are susceptible to mechanical and electrostatic damage.

TABLE 3-4: WAFER MECHANICAL SPECIFICATIONS

Specifications	Min	Typ	Max	Unit	Comments
Wafer Diameter	—	8	—	inch	150 mm
Die separation line width	—	80	—	µm	
Dice per wafer	—	14,000	—	die	
Batch size	—	24	—	wafer	

4.0 FAILED DIE IDENTIFICATION

Every die on the wafer is electrically tested according to the data sheet specifications and visually inspected to detect any mechanical damage such as mechanical cracks and scratches.

Any failed die in the test or visual inspection is identified by black colored inking. Therefore, any die covered with black ink should not be used.

The ink dot specification:

- Ink dot size: minimum 20 µm x 20 µm
- Position: central third of die
- Color: black

5.0 WAFER DELIVERY DOCUMENTATION

Each wafer container is marked with the following information:

- Microchip Technology Inc. MP Code
- Lot Number
- Total number of wafer in the container
- Total number of good dice in the container
- Average die per wafer (DPW)
- Scribe number of wafer with number of good dice.

6.0 NOTICE ON DIE AND WAFER HANDLING

The device is very susceptible to Electrostatic Discharge (ESD). ESD can cause critical damage to the device. Special attention is needed during the handling process.

Any ultraviolet (UV) light can erase the memory cell contents of an unpackaged device. Fluorescent lights and sun light can also erase the memory cell although it takes more time than UV lamps. Therefore, keep any unpackaged devices out of UV light and also avoid direct exposure from strong fluorescent lights and sun light.

Certain integrated circuit (IC) manufacturing, chip-on-board (COB) and tag assembly operations may use UV light. Operations such as backgrind, de-tape, certain cleaning operations, epoxy or glue cure should be done without exposing the die surface to UV light.

Using x-ray for die inspection will not harm the die, nor erase memory cell contents.

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

8-Lead PDIP (300 mil)

XXXXXXXX
XXXXXNNN
YYWW

Example:

MCRF202
XXXXXNNN
0025

8-Lead SOIC (150 mil)

XXXXXXX
XXXYYWW
NNN

Example:

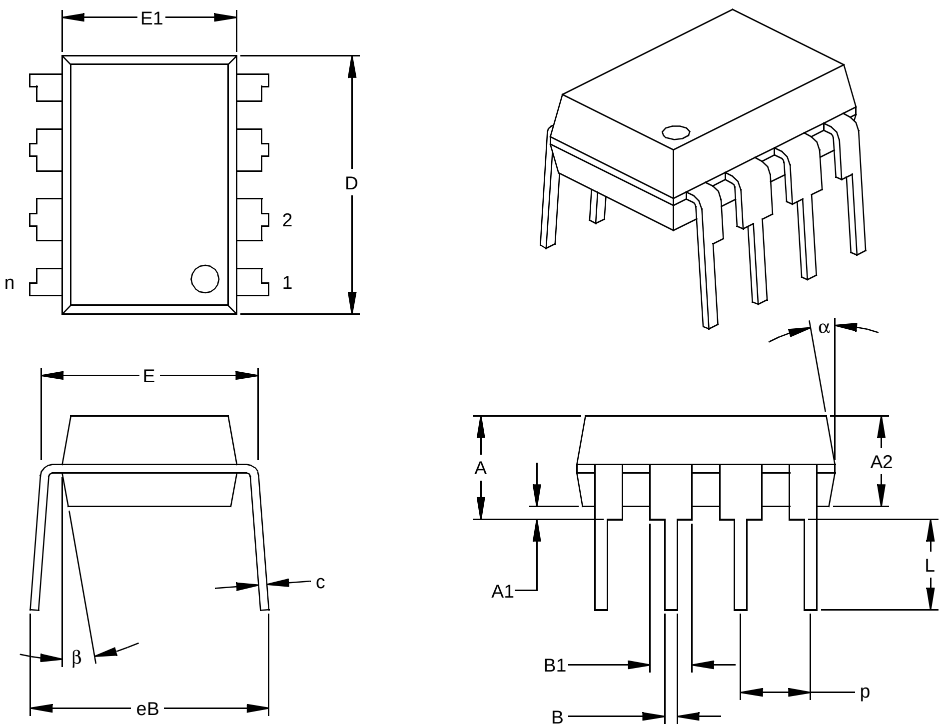
MCRF202
XXX0025
NNN

Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

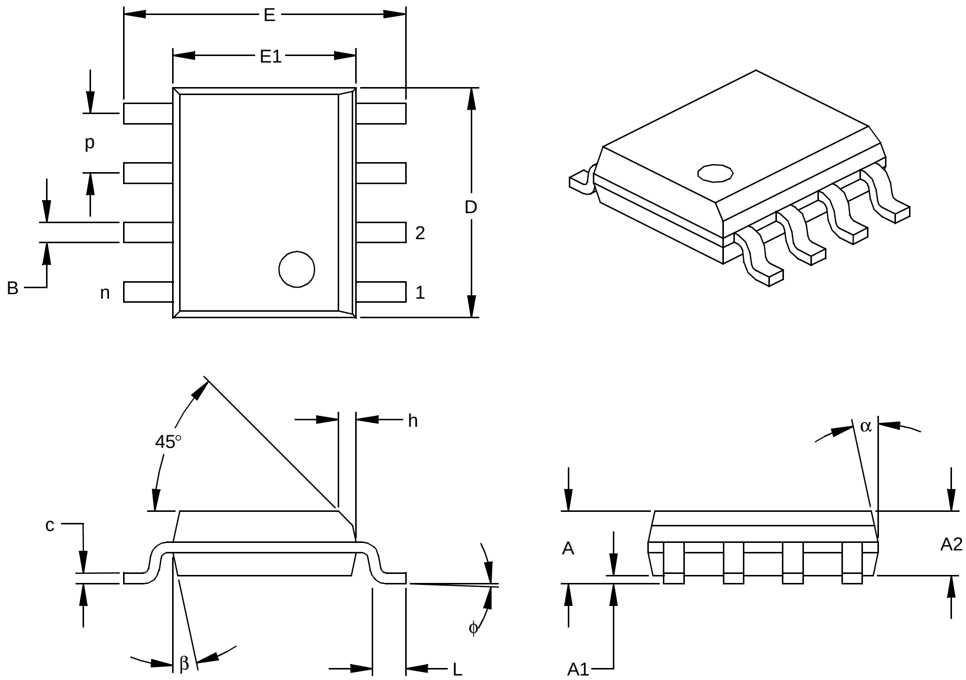


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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Application (optional):

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Device: MCRF202   Literature Number: DS21308E

Questions:

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____

____

2. How does this document meet your hardware and software development needs?

____

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3. Do you find the organization of this document easy to follow? If not, why?

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5. What deletions from the document could be made without affecting the overall usefulness?

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6. Is there any incorrect or misleading information (what and where)?

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7. How would you improve this document?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XXX	XXX
Device	Temperature Range	Package	Configuration

Device:	MCRF202	=	125 kHz MicroID tag with Sensor input, 96/128-bit
Temperature Range:	I	=	-40°C to +85°C
Package:	WF	=	Sawed wafer on frame (7 mil backgrind)
	W	=	Wafer (11 mil backgrind)
	S	=	Dice in waffle pack (11 mil backgrind)
	WFB	=	Sawed, Bumped wafer on frame (11 mil backgrind)
	WB	=	Bumped wafer (11 mil backgrind)
	SB	=	Bumped die in waffle pack (11 mil backgrind)
	SN	=	Plastic SOIC (150 mil body) 8-lead
	P	=	Plastic DIP (300 mil body) 8-lead
Configuration:	SQTP Customer Identifier. Assigned during the SQTP (factory programming) approval process. Usually QXX where XX is an integer used to track customer data files.		

Examples:

a) MCRF202-I/WQ99 = 125 kHz, industrial temperature, wafer package, factory programmed, sensor input, "Q99" sample customer code.

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003 . The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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