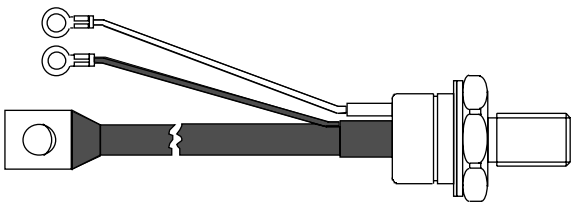
Phase Control Thyristors (Stud Version), 110 A



TO-209AC (TO-94)

FEATURES

- Center gate
- International standard case TO-209AC (TO-94)
- Compression bonded encapsulation for heavy duty operations such as severe thermal cycling
- Hermetic glass-metal case with ceramic insulator (Glass-metal seal over 1200 V)
- Lead (Pb)-free
- Designed and qualified for industrial level

RoHS COMPLIANT

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY	
$I_{T(AV)}$	110 A

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		110	A
	T_C	90	°C
$I_{T(RMS)}$		175	A
I_{TSM}	50 Hz	2700	
	60 Hz	2830	
I^2t	50 Hz	36.4	kA^2s
	60 Hz	33.2	
V_{DRM}/V_{RRM}		400 to 1600	V
t_q	Typical	100	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST110S	04	400	500	20
	08	800	900	
	12	1200	1300	
	16	1600	1700	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			110	A
					90	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 85 °C case temperature			175	A
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	2700	
		t = 8.3 ms			2830	
		t = 10 ms	100 % V_{RRM} reapplied		2270	
		t = 8.3 ms			2380	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		36.4	kA^2s
		t = 8.3 ms			33.2	
		t = 10 ms	100 % V_{RRM} reapplied		25.8	
		t = 8.3 ms			23.5	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			364	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.90	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.92	
Low level value of on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.79	mΩ
High level value of on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.81	
Maximum on-state voltage	V_{TM}	I_{pk} = 350 A, $T_J = T_J$ maximum, t_p = 10 ms sine pulse			1.52	V
Maximum holding current	I_H	T_J = 25 °C, anode supply 12 V resistive load			600	mA
Typical latching current	I_L				1000	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ µs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	500	A/µs
Typical delay time	t_d	Gate current 1 A, dI_g/dt = 1 A/µs V_d = 0.67 % V_{DRM}, T_J = 25 °C	2.0	µs
Typical turn-off time	t_q	I_{TM} = 100 A, $T_J = T_J$ maximum, dI/dt = 10 A/µs, V_R = 50 V, dV/dt = 20 V/µs, gate 0 V 100 Ω, t_p = 500 µs	100	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/µs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	20	mA

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		5		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		1		
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		2.0		A
Maximum peak positive gate voltage	+ V_{GM}			20		V
Maximum peak negative gate voltage	- V_{GM}			5.0		
DC gate current required to trigger	I_{GT}	T_J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 6 V anode to cathode applied	180	-	mA
		T_J = 25 °C		90	150	
		T_J = 125 °C		40	-	
DC gate voltage required to trigger	V_{GT}	T_J = - 40 °C		2.9	-	V
		T_J = 25 °C		1.8	3.0	
		T_J = 125 °C		1.2	-	
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.195	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.08	
Mounting torque, ± 10 %		Non-lubricated threads	15.5 (137)	Nm (lbf · in)
		Lubricated threads	14 (120)	
Approximate weight			130	g
Case style		See dimensions - link at the end of datasheet	TO-209AC (TO-94)	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.035	0.025	$T_J = T_J$ maximum	K/W
120°	0.041	0.042		
90°	0.052	0.056		
60°	0.076	0.079		
30°	0.126	0.127		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

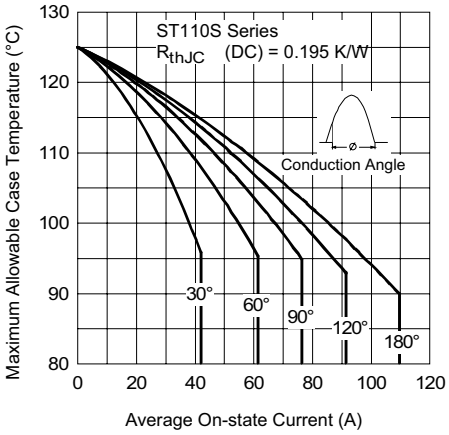


Fig. 1 - Current Ratings Characteristics

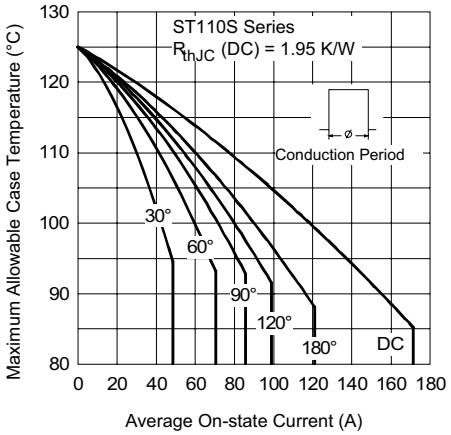


Fig. 2 - Current Ratings Characteristics

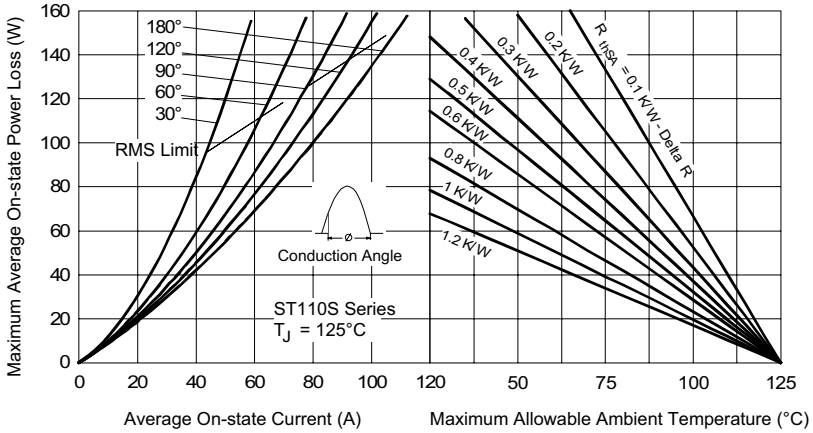


Fig. 3 - On-State Power Loss Characteristics

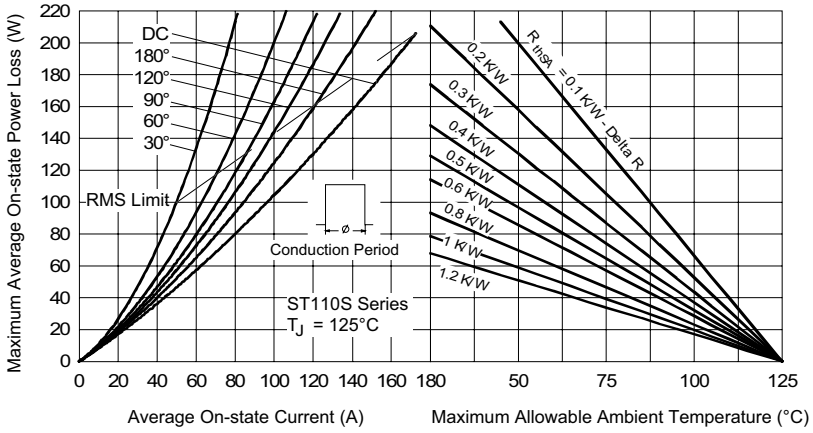


Fig. 4 - On-State Power Loss Characteristics

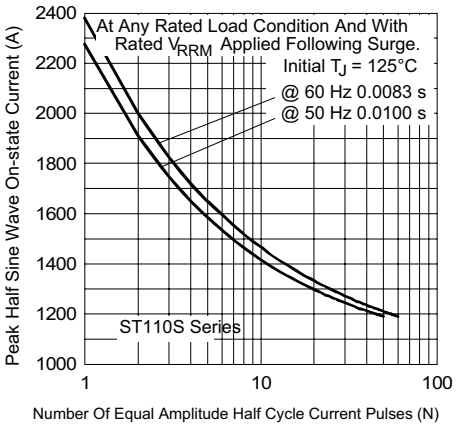


Fig. 5 - Maximum Non-Repetitive Surge Current

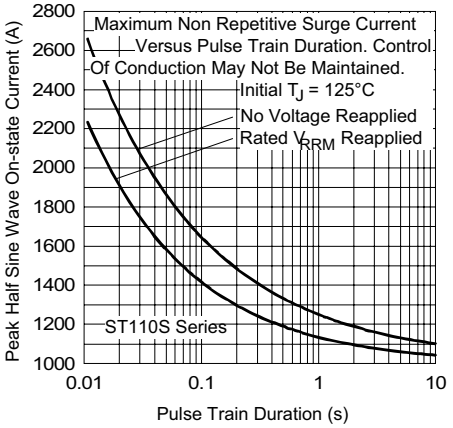


Fig. 6 - Maximum Non-Repetitive Surge Current

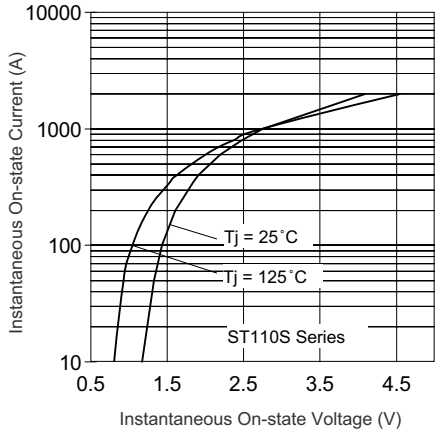


Fig. 7 - On-State Voltage Drop Characteristics

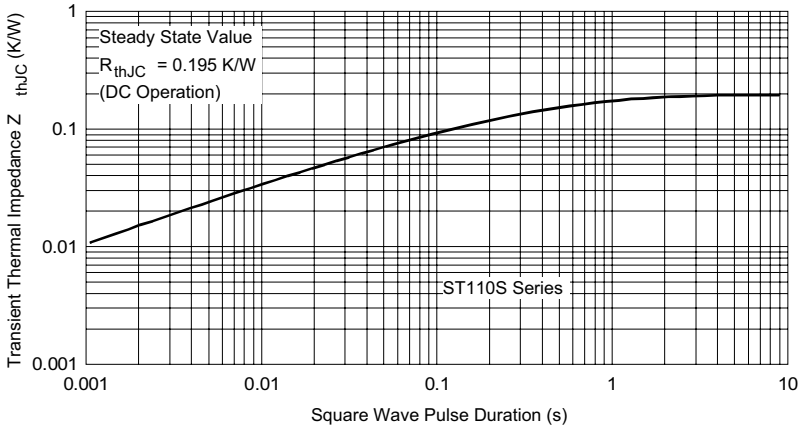


Fig. 8 - Thermal Impedance Z_{thJC} Characteristic

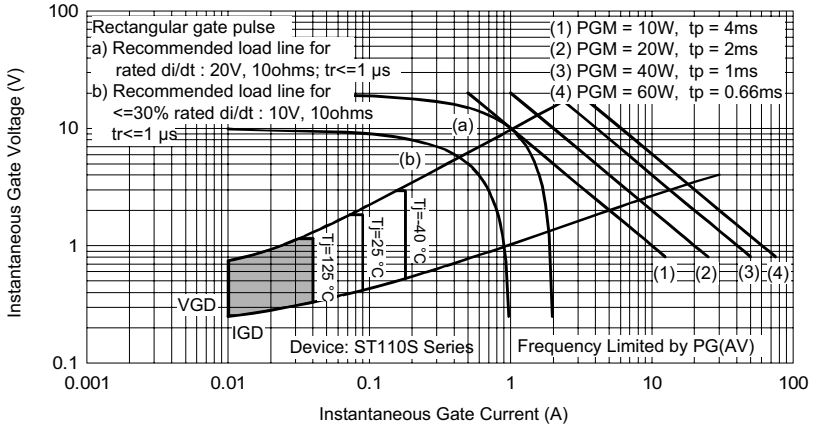


Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

ST	11	0	S	16	P	0	V	PbF
1	2	3	4	5	6	7	8	9

- **1** - Thyristor
- **2** - Essential part marking
- **3** - 0 = Converter grade
- **4** - S = Compression bonding stud
- **5** - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- **6** - P = Stud base 1/2"-20UNF- 2 A threads
- **7** - 0 = Eyelet terminals (gate and auxiliary cathode leads)
  1 = Fast-on terminals (gate and auxiliary cathode leads)
- **8** - • V = Glass-metal seal (only up to 1200 V)
  • None = Ceramic housing (over 1200 V)
- **9** - Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95078

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.