Lattice Semiconductor

MACH4-96/96-15

High-Performance EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- **144 Pins in PQFP**
- **96 Macrocells**
- **15 ns t_{PD} Commercial, 18 ns t_{PD} Industrial**
- **47.6 MHz f_{CNT}**
- **102 Inputs with pull-up resistors**
- **96 I/Os; 4 dedicated inputs/clocks; 2 dedicated inputs**
- **96 Flip-flops**
- **Up to 20 product terms per macrocell, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **3 MACH111SP-size blocks**
- **SpeedLocking™ for guaranteed fixed timing**
- **JTAG, 5-V, in-system programmable**
- **JTAG (IEEE 1149.1) boundary scan testing capability**
- **Input and output switch matrices for high routability**

PLEASE NOTE: The MACH4-96/96 (M4-96/96) reflects a new nomenclature for the MACH® 4 Family. This device is currently dual-marked with the MACH355 ordering part number. The dual-mark scheme will facilitate design and manufacturing flows until we have completely phased in the new M4-96/96 nomenclature. Please use the MACH355 data sheet (PID# 17467) as a reference.

GENERAL DESCRIPTION

The MACH4-96/96 (M4-96/96) is a member of Vantis' high-performance EE CMOS MACH 4 family. This device has approximately three times the macrocell capability of the popular MACH111SP, with significant additional density and functional features.

The M4-96/96 consists of six PAL® blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

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The M4-96/96 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per macrocell can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The M4-96 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer using software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Vantis offers software design support for MACH devices through its own development system and device fitters integrated into third-party CAE tools. Platform support extends across PCs, Sun and HP workstations under advanced operating systems such as Windows 3.1, Windows 95 and NT, SunOS and Solaris, and HPUX.

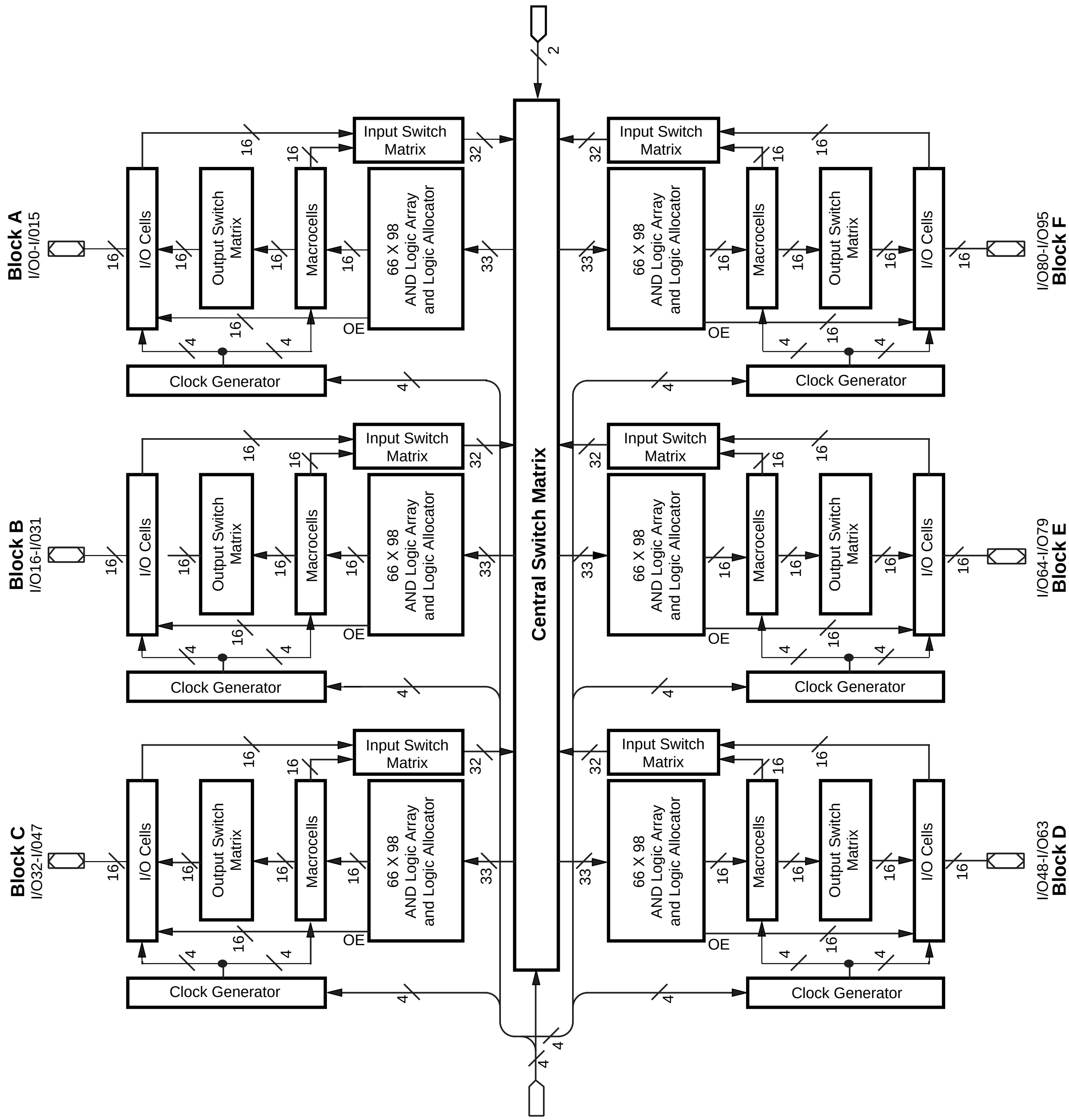
MACHXL® software is a complete development system for the PC, supporting Vantis' MACH devices. It supports design entry with Boolean and behavioral syntax, state machine syntax and truth tables. Functional simulation and static timing analysis are also included in this easy-to-use system. This development system includes high-performance device fitters for all MACH devices.

The same fitter technology included in MACHXL software is seamlessly incorporated into third-party tools from leading CAE vendors such as Synario, Viewlogic, Mentor Graphics, Cadence and MINC. Interface kits and MACHXL configurations are also available to support design entry and verification with other leading vendors such as Synopsys, Exemplar, OrCAD, Synplicity and Model Technology. These MACHXL configurations and interfaces accept EDIF 2.0.0 netlists, generate JEDEC files for MACH devices, and create industry-standard SDF, VITAL-compliant VHDL and Verilog output files for design simulation.

Vantis offers in-system programming support for MACH devices through its MACHPRO® software enabling MACH device programmability through JTAG compliant ports and easy-to-use PC interface. Additionally, MACHPRO generated vectors work seamlessly with HP3070, GenRad and Teradyne testers to program MACH devices or test them for connectivity.

All MACH devices are supported by industry standard programmers available from a number of vendors. These programmer vendors include Advin Systems, BP Microsystems, Data I/O Corporation, Hi-Lo Systems, SMS GmbH, Stag House, and System General.

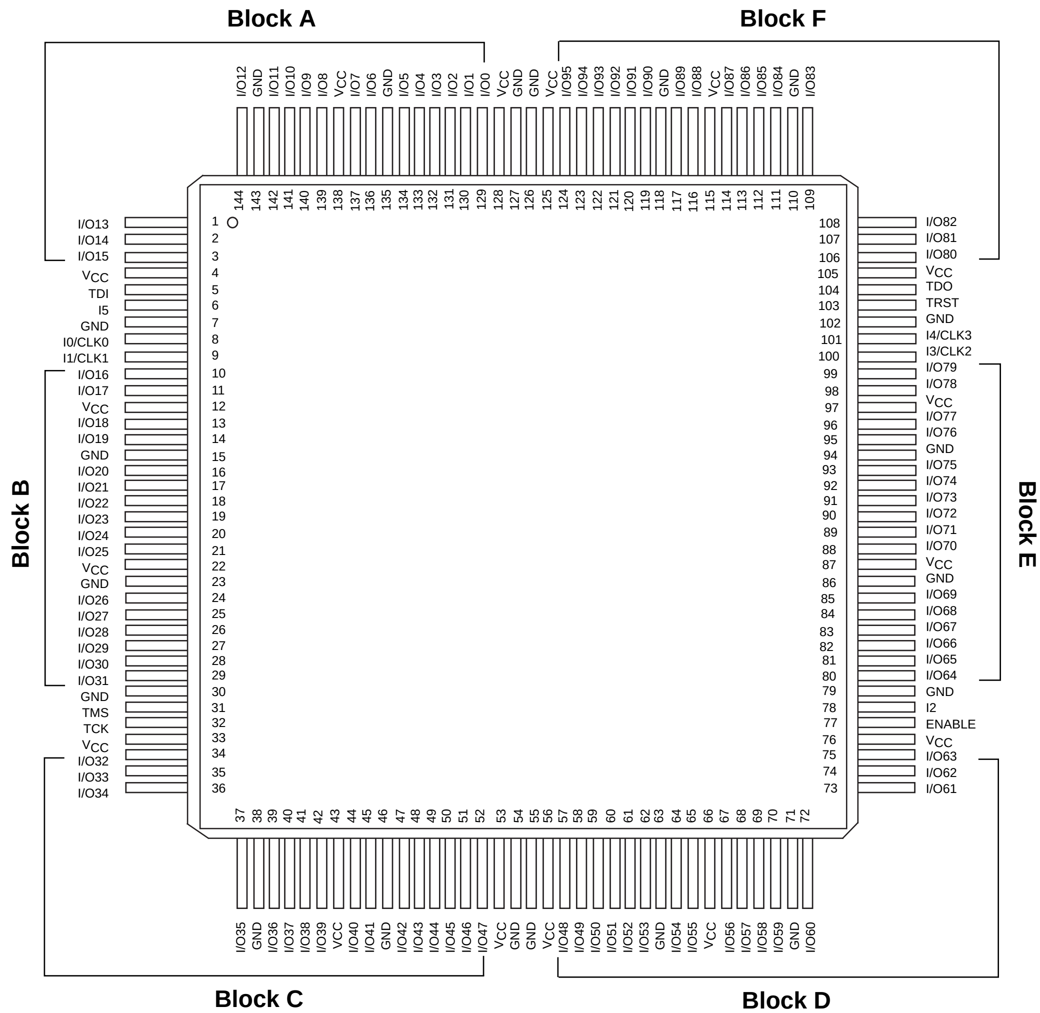
BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View

144-Pin PQFP



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TMS = Test Mode Select

TCK = Test Clock

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

ORDERING INFORMATION

Commercial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4 -96 /96 -15 Y C

FAMILY TYPE
M4 = MACH 4 Family (5-V V_{CC})

DEVICE NUMBER
96 = 96 Macrocells

I/O
/96 =144-pin Package

SPEED
-15 = 15 ns t_{PD}

PACKAGE TYPE
Y = 144-Pin Plastic Quad Pack (PQR144)

OPERATING CONDITIONS
C = Commercial (0°C to +70°C)

Valid Combinations	
MACH4-96/96-15	YC

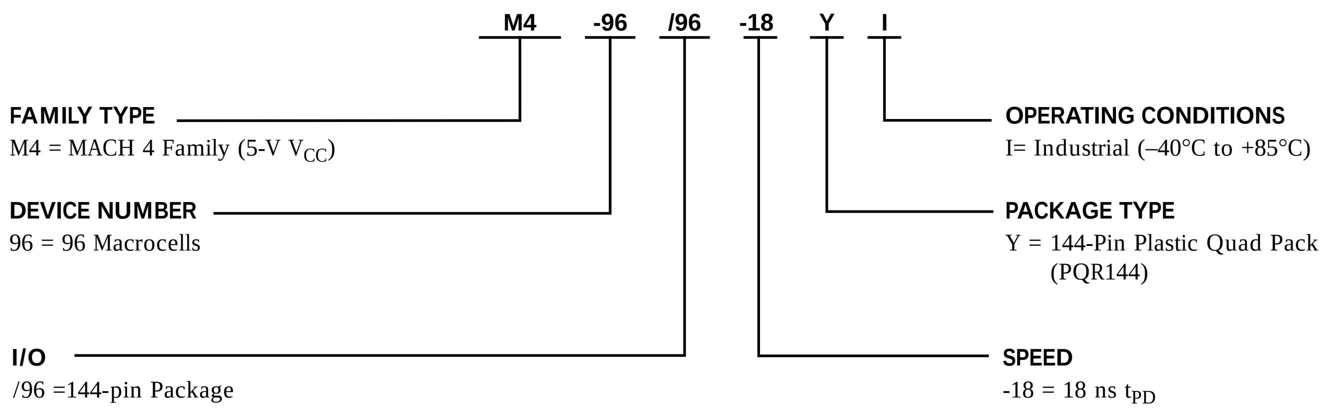
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH4-96/96-18	YI

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The M4-96/96 consists of six PAL blocks connected by a central switch matrix. There are 96 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the M4-96/96 (Figure 7) contains a clock generator, a 98-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 16 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent “PALCE33V16”.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

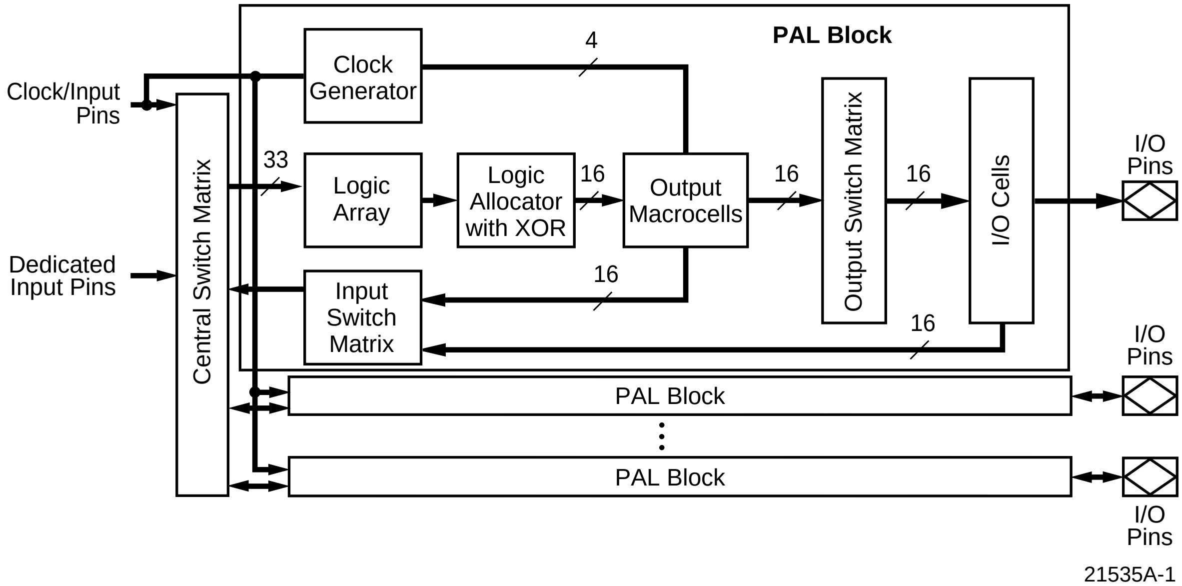


Figure 1.   MACH4-96/96 Block Diagram and PAL Block Structure

The Central Switch Matrix and Input Switch Matrix

The M4-96/96 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals and 16 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device. The input switch matrix (Figure 2) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

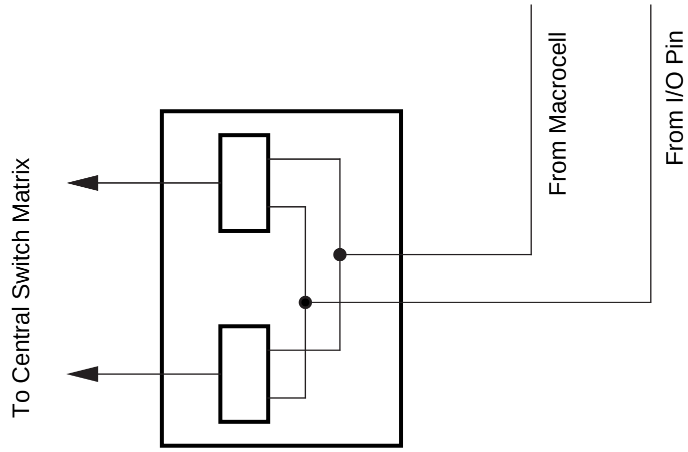


Figure 2. MACH4-96/96 Input Switch Matrix

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

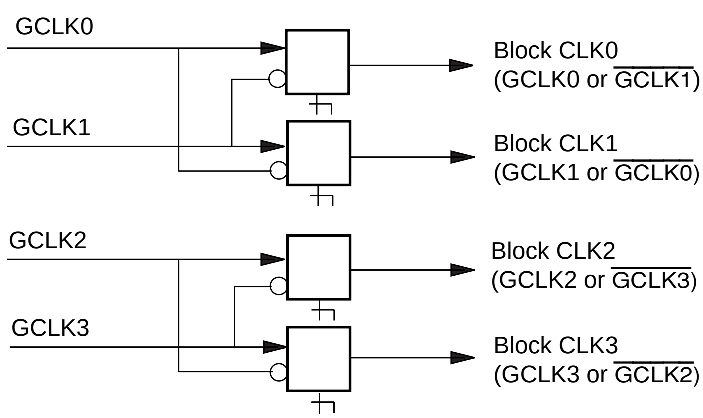


Figure 3. PAL Block Clock Generator

Synchronous and Asynchronous Operation

The MACH 4 family can perform synchronous or asynchronous logic. Each individual cell can be programmed as synchronous or asynchronous, allowing unlimited “mixing and matching” of the two logic styles. The selection of synchronous or asynchronous mode affects the logic allocator and the macrocell, since product terms used for logic in the synchronous mode are used for control functions in the asynchronous mode.

The Product-Term Array

The M4-96/96 product-term array consists of 80 product terms for logic use, 16 product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the M4-96/96 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms in synchronous mode, or 18 product terms in asynchronous mode. When product terms are routed away from a macrocell, it is possible to redirect all 5 product terms away, which precludes the use of the macrocell for logic generation. It is possible to route only 4 product terms; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. Emulating all flip-flop types with a D-type flip-flop is also made possible. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 7 for cluster and macrocell numbers.

Table 1. Output Switch Matrix Combinations

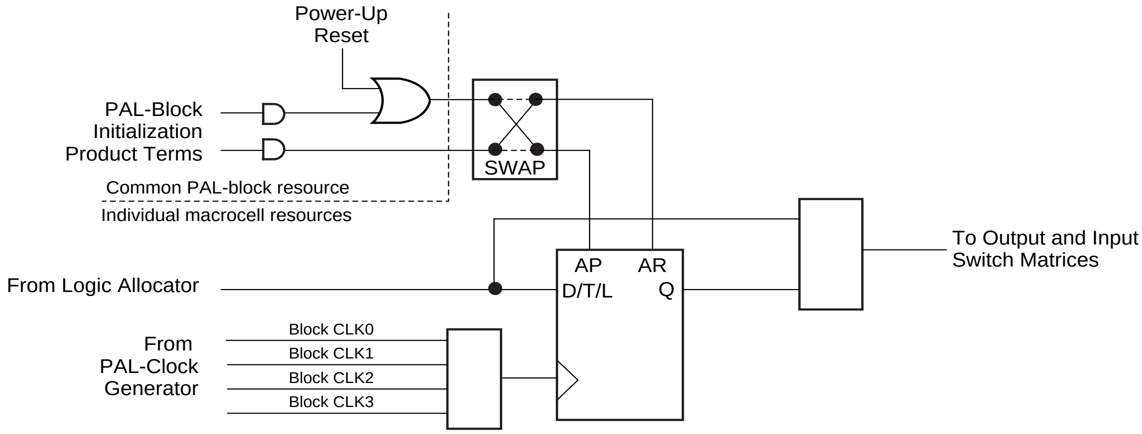
Macrocell	Routable to I/O Pins
M0, M1 M2, M3 M4, M5 M6, M7	I/O0, I/O1,I/O2,I/O3,I/O4,I/O5, I/O6,I/O7
M8, M9 M10, M11 M12, M13 M14, M15	I/O8,I/O9,I/O10,I/O11,I/O12, I/O13,I /O14,I/O15
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M1, M2, M3, M4, M5, M6, M7, M0
I/O2	M2, M3, M4, M5, M6, M7, M0, M1
I/O3	M3, M4, M5, M6, M7, M0, M1, M2
I/O4	M4, M5, M6, M7 M0, M1, M2, M3
I/O5	M5, M6, M7, M0, M1, M2, M3, M4
I/O6	M6, M7, M0, M1, M2, M3, M4, M5
I/O7	M7, M0, M1, M2, M3, M4, M5, M6
I/O8	M8, M9, M10, M11, M12, M13, M14, M15
I/O9	M9, M10, M11, M12, M13, M14, M15, M8
I/O10	M10, M11, M12, M13, M14, M15, M8, M9
I/O11	M11, M12, M13, M14, M15, M8, M9, M10
I/O12	M12, M13, M14, M15, M8, M9, M10, M11
I/O13	M13, M14, M15, M8, M9, M10, M11, M12
I/O14	M14, M15, M8, M9, M10, M11, M12, M13
I/O15	M15, M8, M9, M10, M11, M12, M13, M14

The Macrocell and Output Switch Matrix

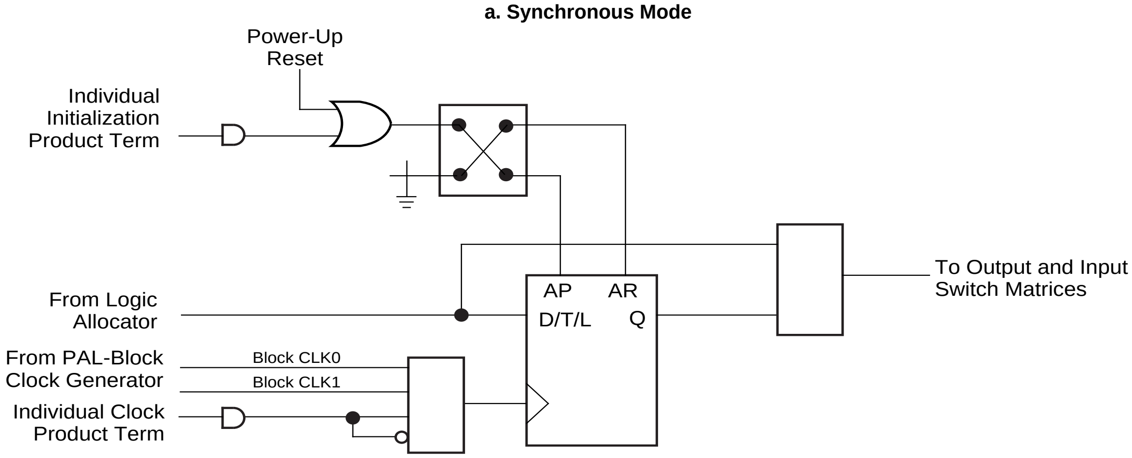
Each M4-96/96 PAL block has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 1. Please refer to Figure 7 for macrocell and I/O pin numbers.The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode (Figure 4). In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.



a. Synchronous Mode



b. Asynchronous Mode

21535A-4

Figure 4. Macrocell

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout, and allows design changes that will not affect pinout.

In the MACH 4 devices, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 5. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells.

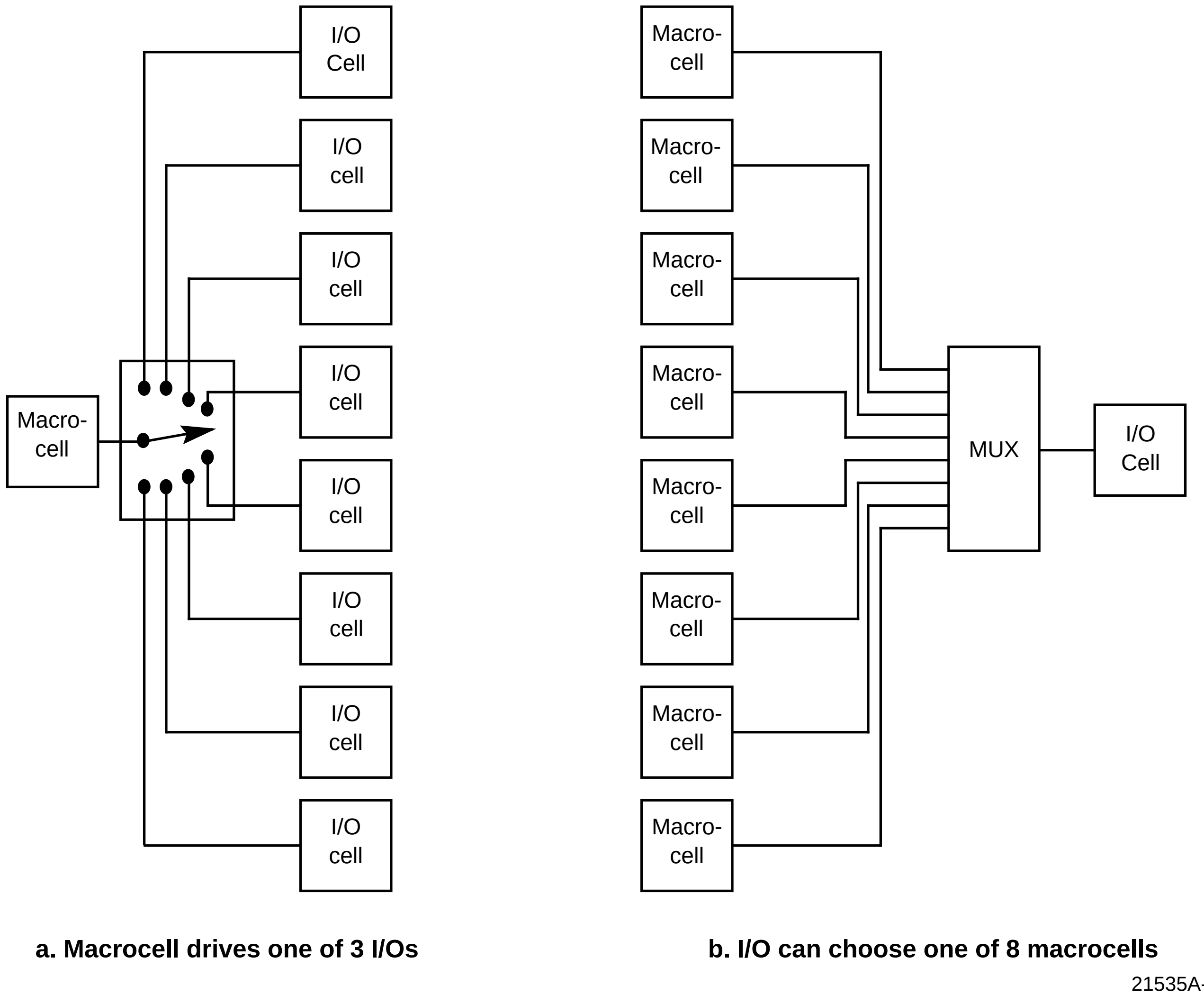


Figure 5. MACH4-96/96 Output Switch Matrix

The I/O Cell

The I/O cell (Figure 6) in the M4-96/96 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The direct I/O signal is available to the input switch matrix, and can be used if desired.

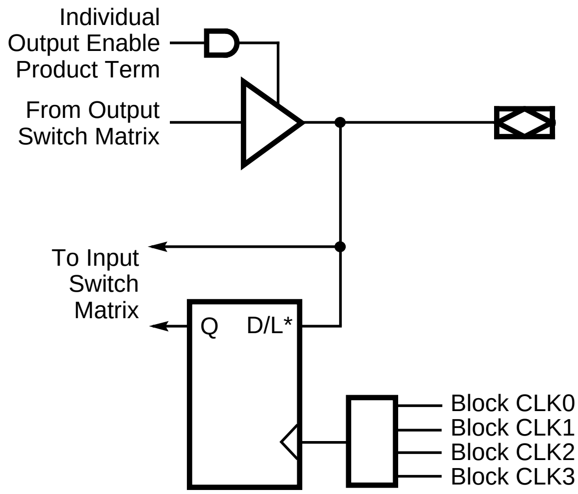


Figure 6. I/O Cell

SpeedLocking for Guaranteed Fixed Timing

The MACH 4 architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate *without* incurring additional timing delays. Using this architectural strength, the M4-96/96 provides the industry's highest-speed and *only* fixed timing at 5-V supply voltages. This SpeedLocking feature delivers guaranteed fixed speed independent of logic path, routing resources, or design refits.

5-V In-System Programming

Another benefit of the JTAG circuitry is the ability to use the JTAG port for 5-V programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port. There is an optional ENABLE pin which can be used to inhibit programming for additional security. These devices can be programmed in any JTAG chain.

JTAG Boundary Scan Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1-1990. The JTAG standard defines input and output pins, logic control functions, and instructions. Vantis has incorporated this standard into the M4-96/96 device.

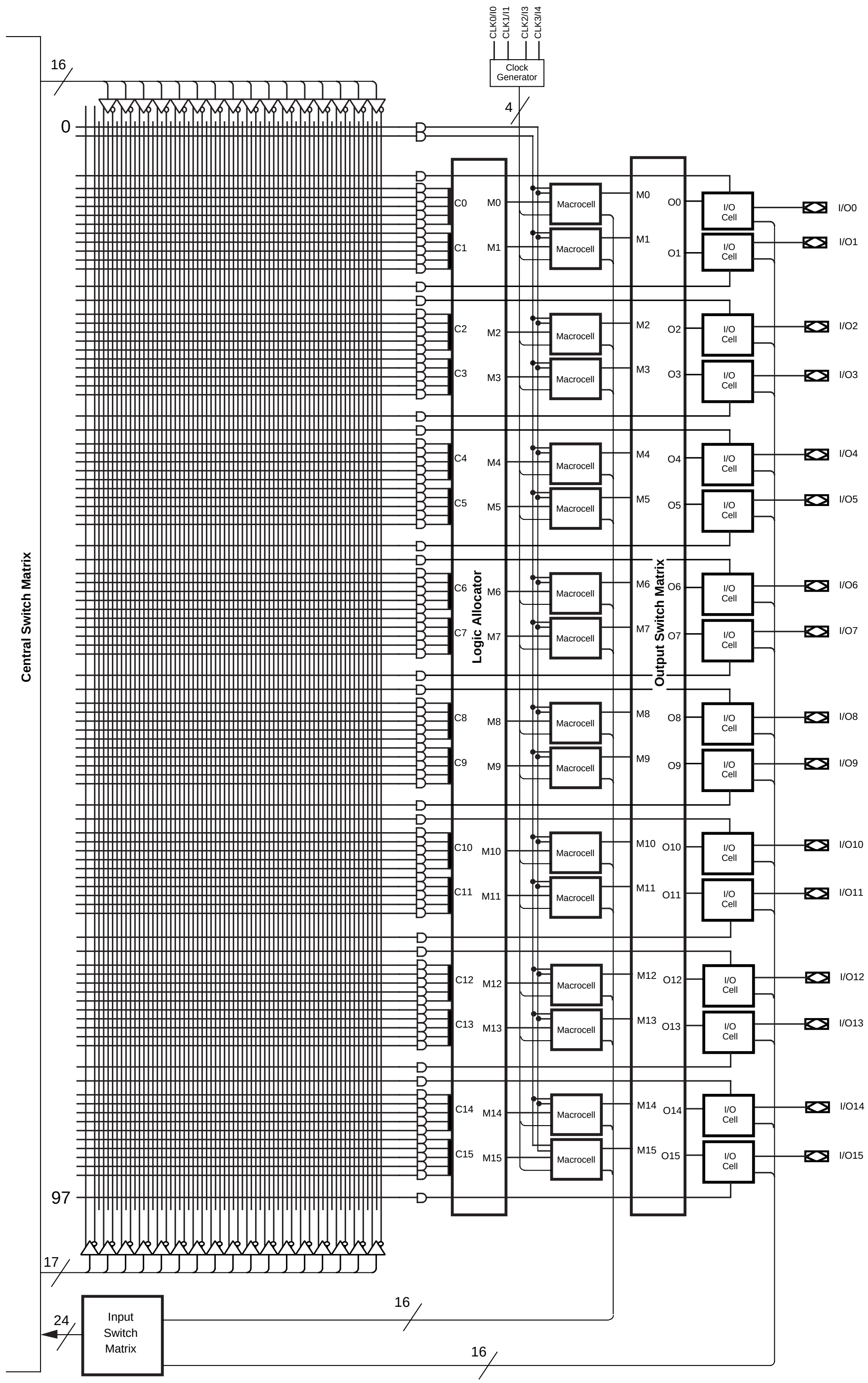


Figure 7. M4-96/96 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . -55°C to +125°C

Device Junction Temperature . . . . +150°C

Supply Voltage with
Respect to Ground . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . -0.5 V to V_{CC} +0.5 V

DC Output or
I/O Pin Voltage . . . . -0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . 2001 V

Latchup Current
(T_A = 0°C to +70°C) . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	-30		-160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		225		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the “Typical Dynamic I_{CC} Characteristics” Chart towards the end of this data sheet.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15 Min	-15 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		ns
				T-type	9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	ns
t_{WLA}	Product Term, Clock Width			LOW	9		ns
t_{WHA}				HIGH	9		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA}+t_{CO})$	D-type	38.5		MHz
				T-type	37		MHz
		Internal Feedback $f_{(CNTA)}$		D-type	47.6		MHz
				T-type	45.4		MHz
		No Feedback (Note 4)	$1/(t_{WLA}+t_{WHA})$		55.6		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		ns
				T-type	11		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	ns
t_{WLS}	Global Clock Width			LOW	6		ns
t_{WHS}				HIGH	6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		MHz
				T-type	47.6		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		MHz
				T-type	62.5		MHz
		No Feedback (Note4)	$1/(t_{WLS} + t_{WHS})$		83.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (Continued)

Parameter Symbol	Parameter Description	-15 Min	-15 Max	Unit
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)	9		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate	10		ns
t_{HLS}	Latch Data Hold Time Using Global Gate	0		ns
t_{GOS}	Gate to Output (Note 2)		11	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)	6		ns
t_{PDL}	Input, I/O or Feedback to Output through Transparent Output Latch		17	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		20	ns
t_{ARW}	Asynchronous Reset Width (Note 3)	15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)	15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20	ns
t_{APW}	Asynchronous Preset Width (Note 3)	15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)	15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2	2	15	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . -55°C to +125°C

Device Junction Temperature . . . . +150°C

Supply Voltage with
Respect to Ground . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . -0.5 V to V_{CC} +0.5 V

DC Output or
I/O Pin Voltage. . . . . -0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . 2001 V

Latchup Current
(T_A = –40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Temperature (T_A) Operating
in Free Air. . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground. . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	-30		-160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		225		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	$V_{CC} = 5.0$ V, $T_A = 25°C$, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V		8	pF

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-18 Min	-18 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	18	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	10		ns
				T-type	11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	20	ns
t_{WLA}	Product Term, Clock Width			LOW	10		ns
t_{WHA}				HIGH	10		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA}+t_{CO})$	D-type	33.3		MHz
				T-type	33.2		MHz
		Internal Feedback $f_{(CNTA)}$		D-type	35.7		MHz
				T-type	34.4		MHz
		No Feedback (Note 4)	$1/(t_{WLA}+t_{WHA})$		50.0		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	12		ns
				T-type	13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		ns
t_{COS}	Global Clock to Output (Note 2)				2	12	ns
t_{WLS}	Global Clock Width			LOW	7		ns
t_{WHS}				HIGH	7		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	41.7		MHz
				T-type	40.0		MHz
		Internal Feedback (f_{CNTS})		D-type	58.8		MHz
				T-type	55.5		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		71.4		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					22	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (Continued)

Parameter Symbol	Parameter Description	-18 Min	-18 Max	Unit
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)	11		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate	12		ns
t_{HLS}	Latch Data Hold Time Using Global Gate	0		ns
t_{GOS}	Gate to Output (Note 2)		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)	7		ns
t_{PDL}	Input, I/O or Feedback to Output through Transparent Output Latch		20	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		22	ns
t_{ARW}	Asynchronous Reset Width (Note 3)	17		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)	17		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		22	ns
t_{APW}	Asynchronous Preset Width (Note 3)	17		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)	17		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)	2	17	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2	2	17	ns

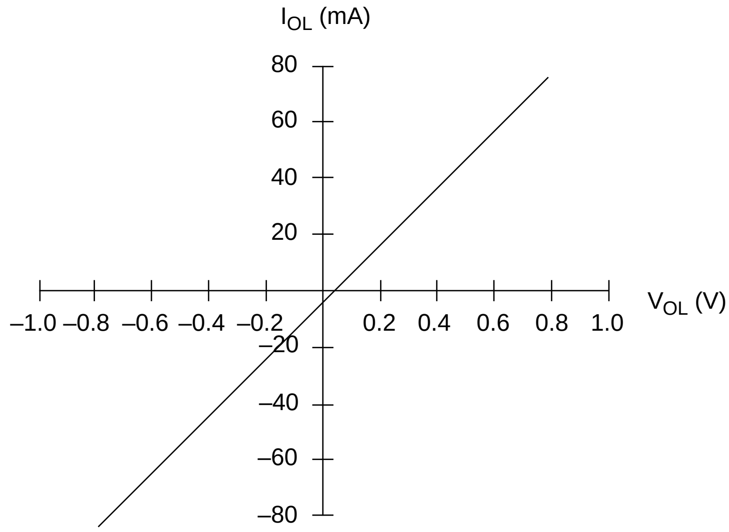
Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

MACH 4 Family

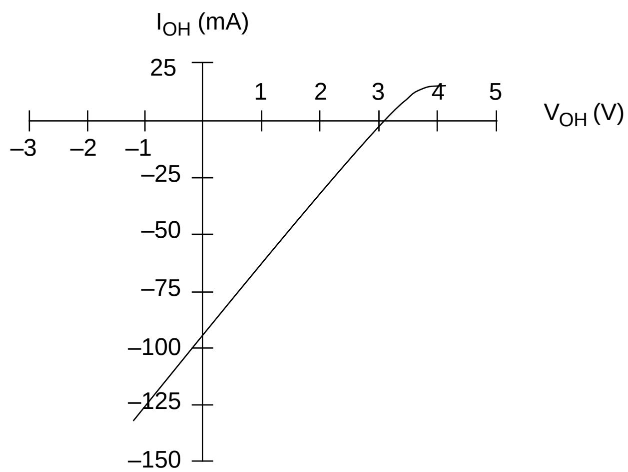
TYPICAL CURRENT vs. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



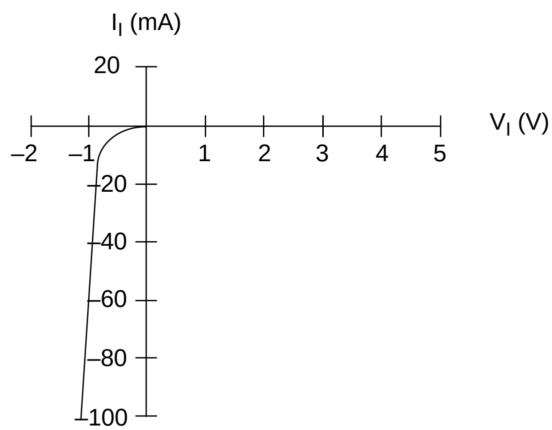
Output, LOW

21535A-7



Output, HIGH

21535A-8

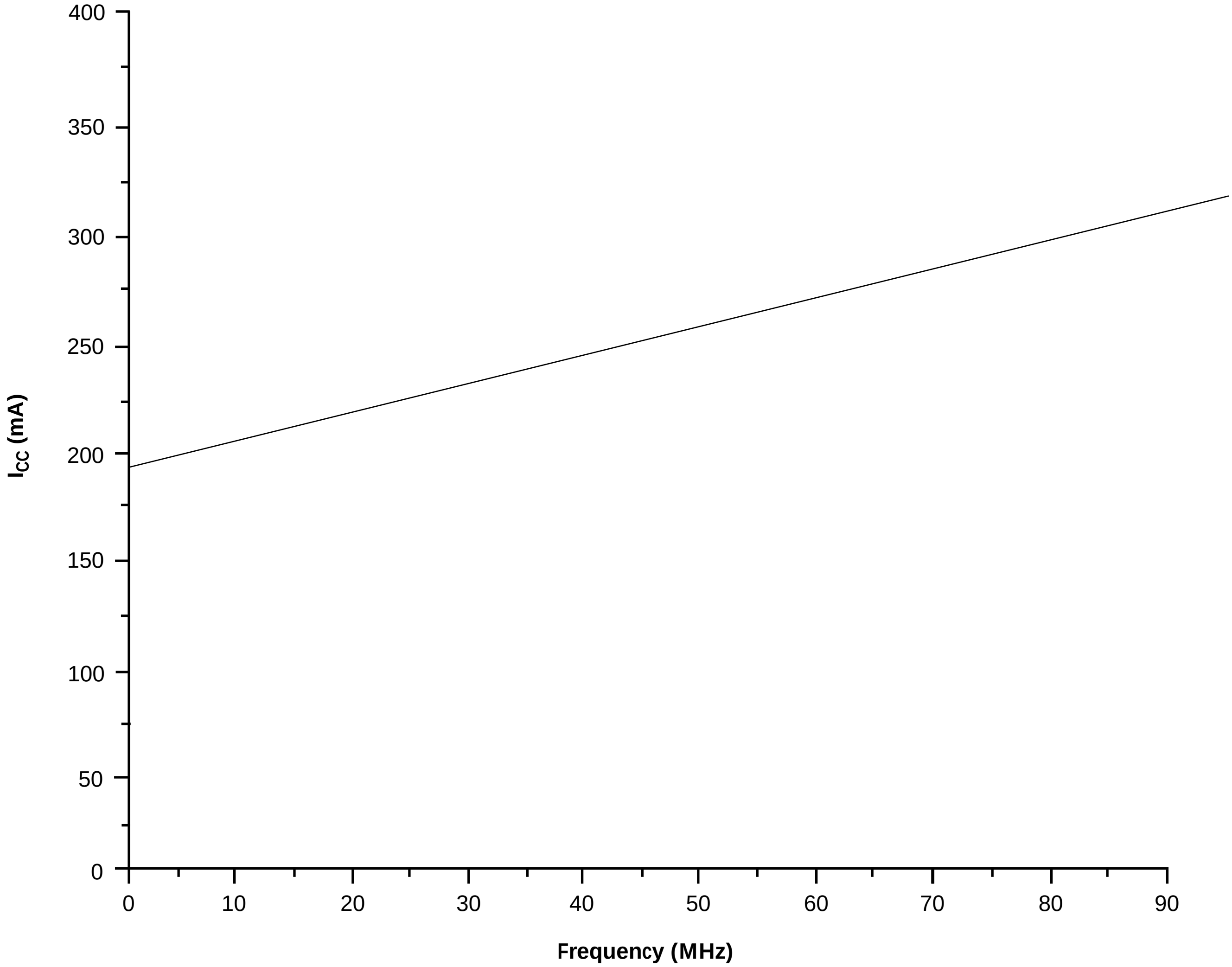


Input

21535A-9

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



21535A-10

The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

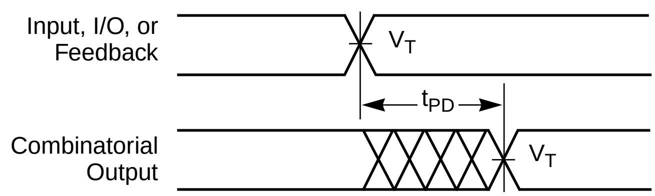
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PQFP	Unit
θ_{jc}	Thermal impedance, junction to case		7	°C /W
θ_{ja}	Thermal impedance, junction to ambient		25	°C /W
θ_{jma}	Thermal impedance, junction to ambient air flow	200 lfpm air	21	°C /W
		400 lfpm air	18	°C /W
		600 lfpm air	16	°C /W
		800 lfpm air	15	°C /W

Plastic θjc Considerations

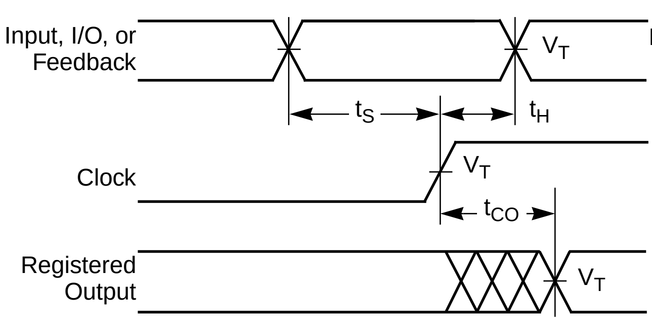
The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

SWITCHING WAVEFORMS



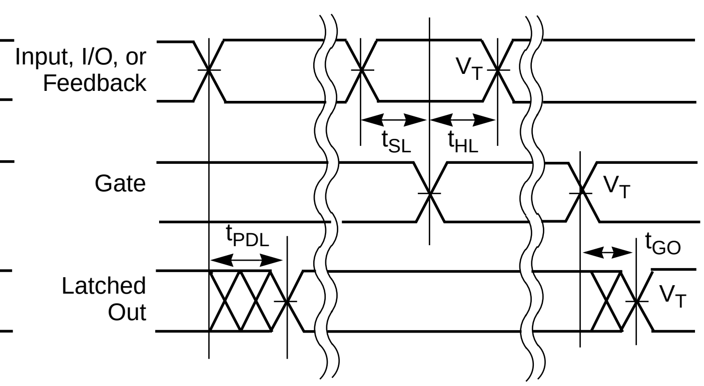
21535A-11

Combinatorial Output



21535A-12

Registered Output



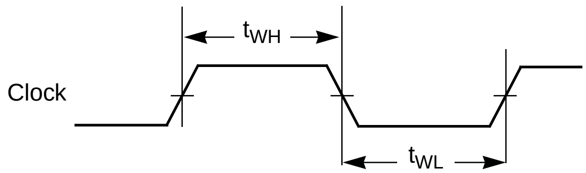
21535A-13

Latched Output

Notes:

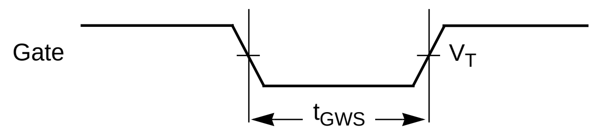
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



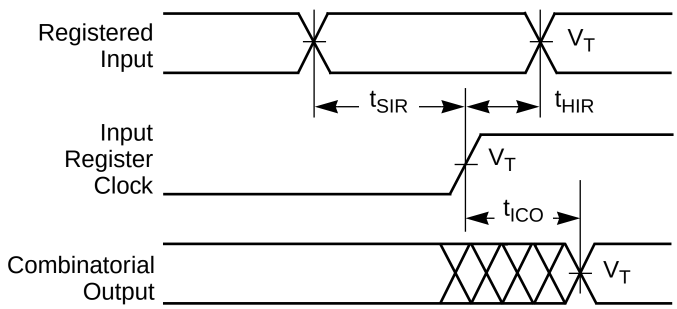
21535A-14

Clock Width



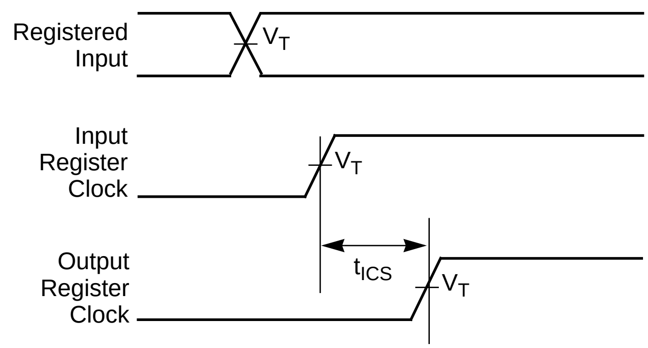
21535A-15

Gate Width



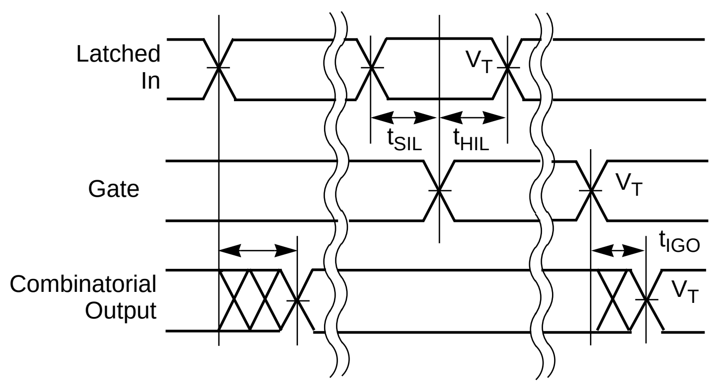
21535A-16

Registered Input



21535A-17

Input Register to Output Register Setup



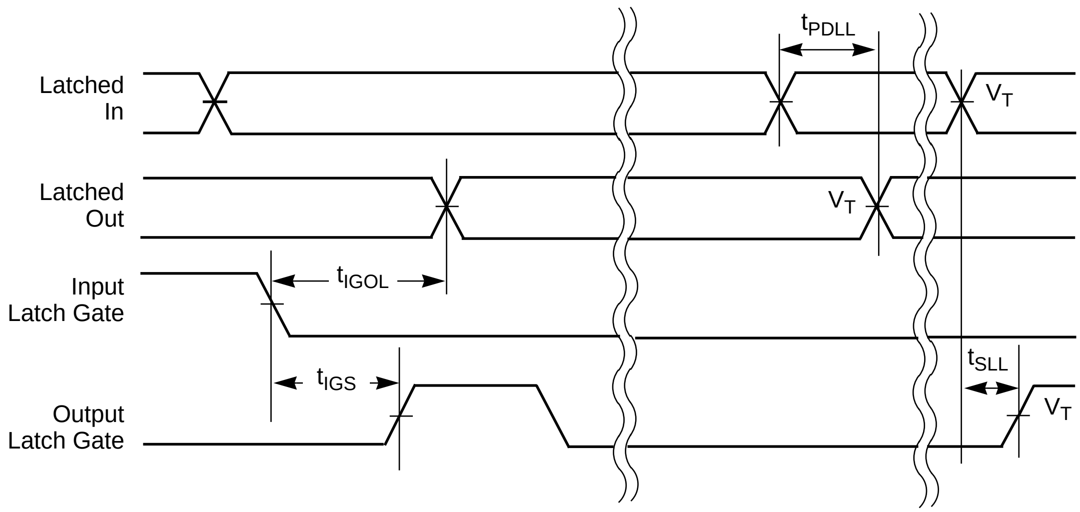
21535A-18

Latched Input

Notes:

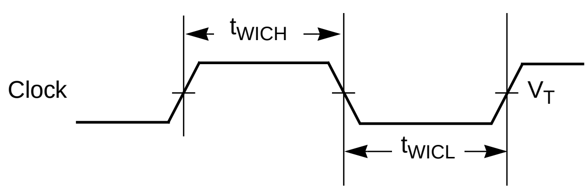
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



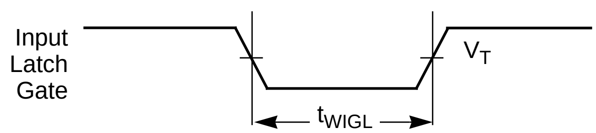
21535A-19

Latched Input and Output



21535A-20

Input Register Clock Width



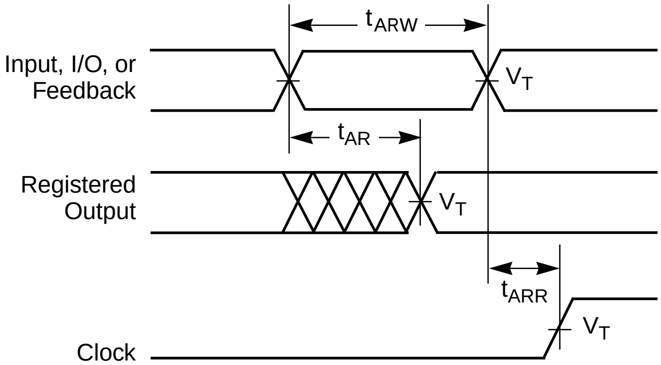
21535A-21

Input Latch Gate Width

Notes:

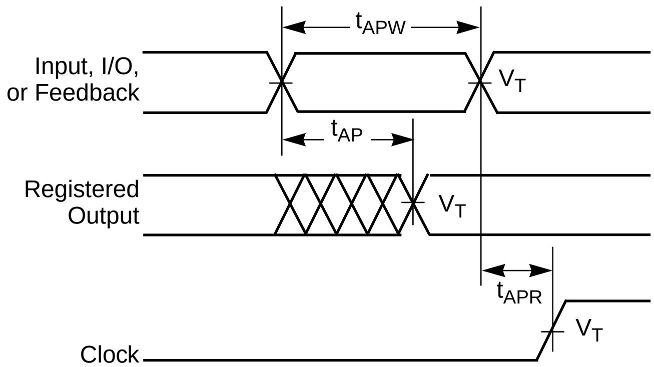
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



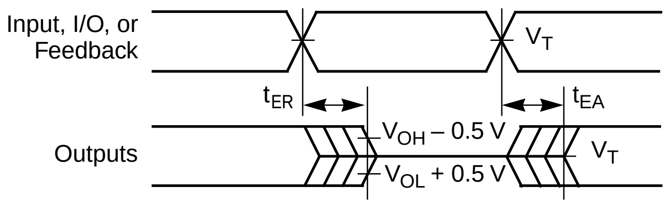
21535A-22

Asynchronous Reset



21535A-23

Asynchronous Preset



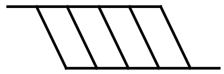
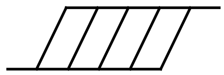
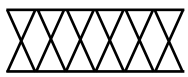
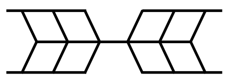
21535A-24

Output Disable/Enable

Notes:

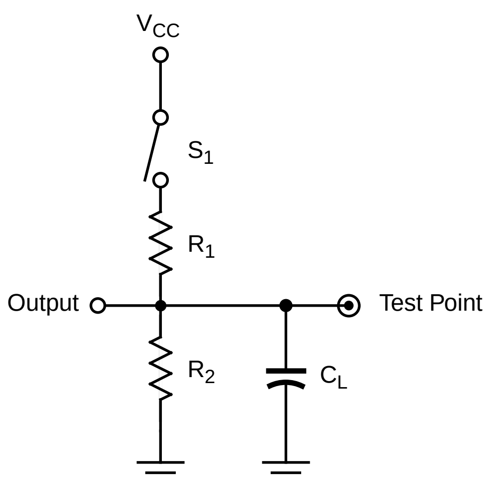
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance “Off” State

KS000010-PAL

SWITCHING TEST CIRCUIT



21535A-25

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

* *Switching several outputs simultaneously should be avoided for accurate measurement.*

f_{MAX} PARAMETERS

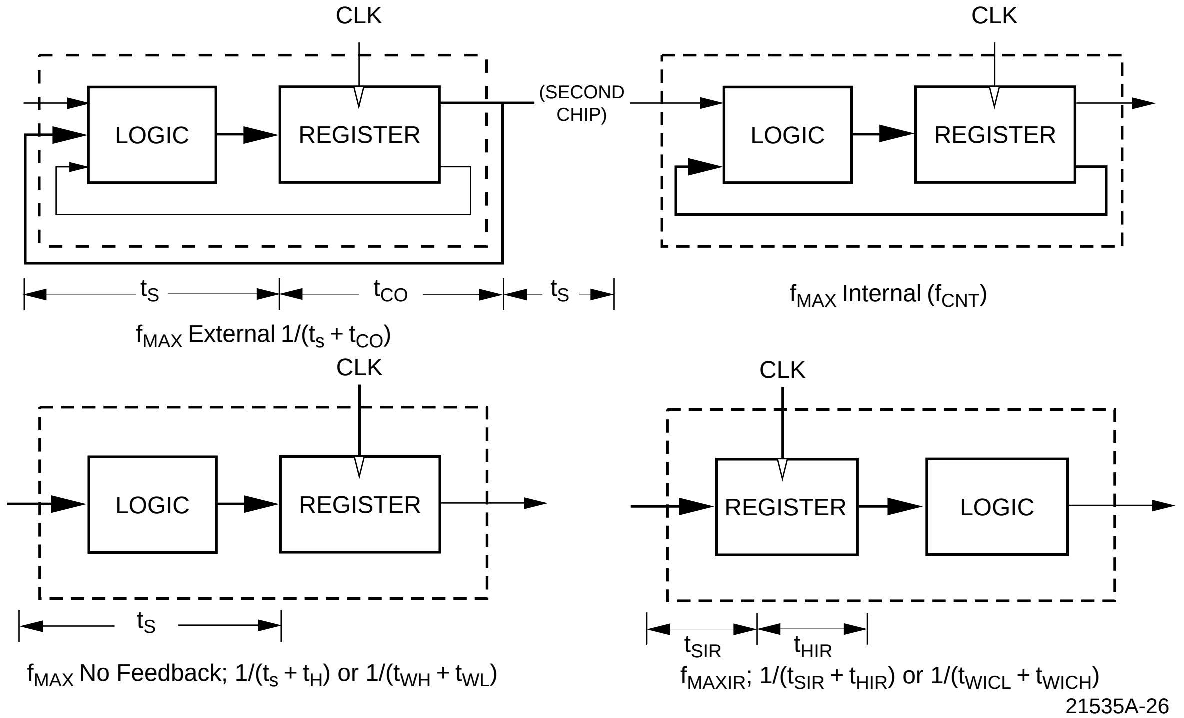
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are used in the same path, the overall frequency will be limited by t_{ICS}. All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



ENDURANCE CHARACTERISTICS

The MACH families are manufactured using Vantis' advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Endurance Characteristics

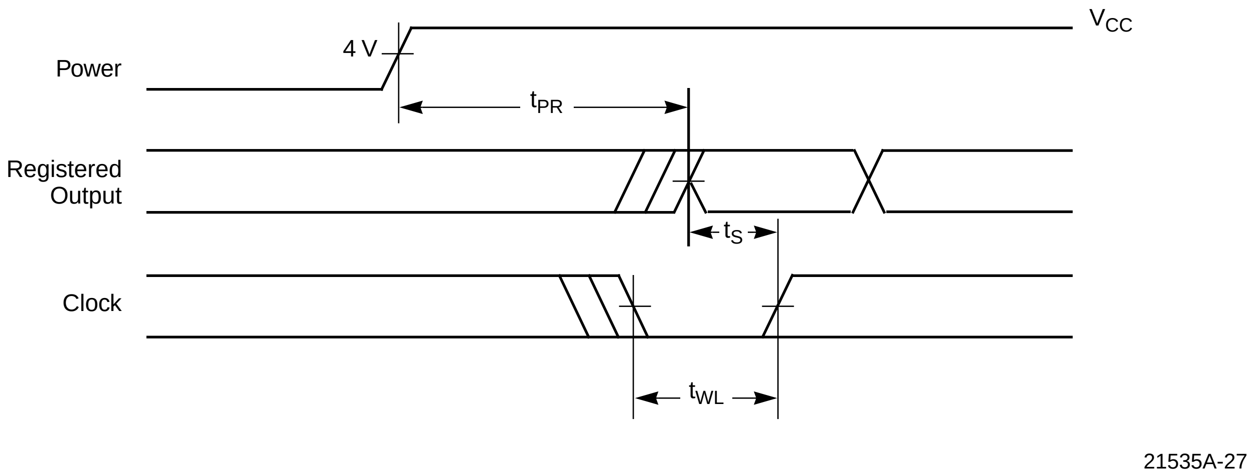
Parameter Symbol	Parameter Description		Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHXL Software Vantis-ABEL Software Vantis-Synario Software
Aldec, Inc. 3 Sunset Way, Suite F Henderson, NV 89014 (702) 456-1222 or (800) 487-8743	ACTIVE-CAD
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234 or (800) 746-6223	PIC Designer Concept/Composer Synergy Leapfrog/Verilog-XL
Exemplar Logic, Inc. 815 Atlantic Avenue, Suite 105 Alameda, CA 94501 (510) 337-3700	Leonardo™ Galileo™
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (800) 346-6335	SmartModel® Library
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	Design Architect, PLDSynthesis™ II Autologic II Synthesizer, QuickSim Simulator, QuickHDL Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	MicroSim Design Lab PLogic, PLSyn
MINC Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner-XL™ Software
Model Technology 8905 S.W. Nimbus Avenue, Suite 150 Beaverton, OR 97008 (503) 641-1340	V-System/VHDL
OrCAD, Inc. 9300 S.W. Nimbus Avenue Beaverton, OR 97008 (503) 671-9500 or (800) 671-9505	OrCAD Express
Synario® Design Automation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Synario™ Software

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Synopsys 700 E. Middlefield Rd. Mountain View, CA 94040 (415) 962-5000 or (800) 388-9125	FPGA or Design Compiler (Requires MINC PLDesigner-XL™) VSS Simulator
Synplicity, Inc. 624 East Evelyn Ave. Sunnyvale, CA 94086 (408) 617-6000	Synplify
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
VeriBest, Inc. 6101 Lookout Road, Suite A Boulder, CO 80301 (800) 837-4237	VeriBest PLD
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 873-8439 or (508) 480-0881	Viewdraw, ViewPLD, Viewsynthesis Speedwave Simulator, ViewSim Simulator, VCS Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 881-8821	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 940 86 (408) 243-7000 or (800) 627-2456 BBS (408) 737-9200 Fax (408) 736-2503	Pilot-U40 Pilot-U84 MVP
BP Microsystems 1000 N. Post Oak Rd., Suite 225 Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600 BBS (713) 688-9283 Fax (713) 688-0920	BP1200 BP1400 BP2100 BP2200
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 426-1045 or (206) 881-6444 BBS (206) 882-3211 Fax (206) 882-1043	UniSite™ Model 2900 Model 3900 AutoSite
Hi-Lo Systems 4F, No. 2, Sec. 5, Ming Shoh E. Road Taipei, Taiwan (886) 2-764-0215 Fax (886) 2-756-6403 or Tribal Microsystems / Hi-Lo Systems 44388 South Grimmer Blvd. Fremont, CA 94538 (510) 623-8859 BBS (510) 623-0430 Fax (510) 623-9925	ALL-07 FLEX-700
SMS GmbH Im Grund 15 88239 Wangen Germany (49) 7522-97280 Fax (49) 7522-972850 or SMS USA 544 Weddell Dr. Suite 12 Sunnyvale, CA 94089 (408) 542-0388	Sprint Expert Sprint Optima Multisite
Stag House Silver Court Watchmead, Welwyn Garden City Herfordshire UK AL7 1LT 44-1-707-332148 Fax 44-1-707-371503	Stag Quazar

MANUFACTURER	PROGRAMMER CONFIGURATION
System General 1603A South Main Street Milpitas, CA 95035 (408) 263-6667 BBS (408) 262-6438 Fax (408) 262-9220 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Road, Shin Diau Taipei, Taiwan (886) 2-917-3005 Fax (886) 2-911-1283	Turpro-1 Turpro-1/FX Turpro-1/TX

APPROVED ADAPTER MANUFACTURERS

MANUFACTURER	PROGRAMMER CONFIGURATION
California Integration Coordinators, Inc. 656 Main Street Placerville, CA 95667 (916) 626-6168 Fax (916) 626-7740	MACH/PAL Programming Adapters
Emulation Technology, Inc. 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982-0660 Fax (408) 982-0664	Adapt-A-Socket® Programming Adapters

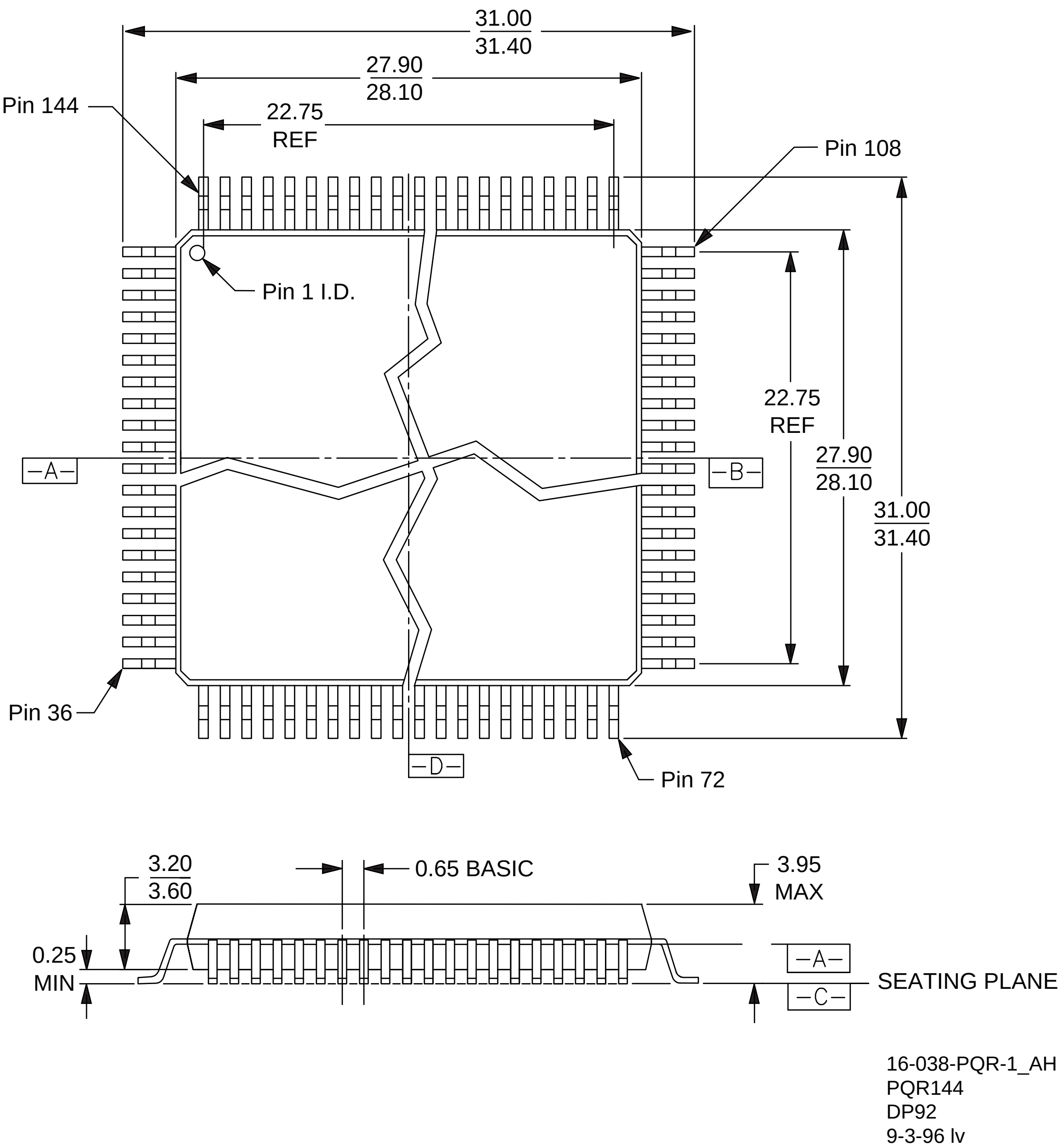
APPROVED ON-BOARD ISP PROGRAMMING TOOLS

MANUFACTURER	PROGRAMMER CONFIGURATION
Corelis, Inc. 12607 Hidden Creek Way, Suite H Cerritos, California 70703 (310) 926-6727	JTAGPROG™
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHPRO®

PHYSICAL DIMENSIONS

PQR144

144-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



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