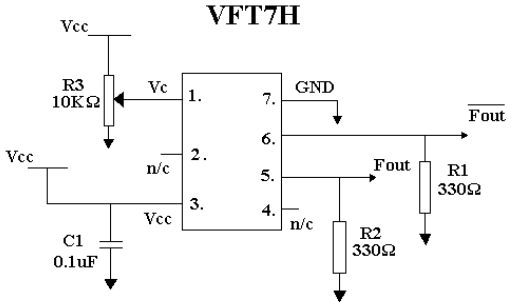
VFT7H Series
TCVCXO
SMD High Frequency

Valpey Fisher Corporation
High Frequency, Low Phase Noise Timing Solutions

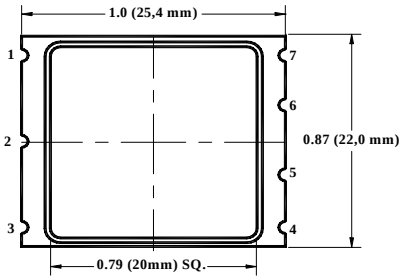
Features

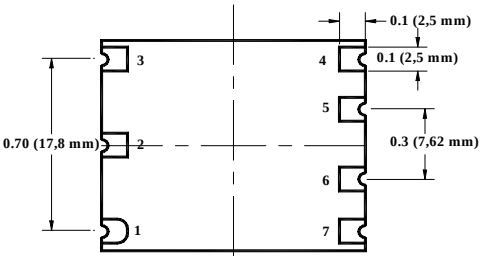
***Not recommended for new designs. Please see VFTX100.**

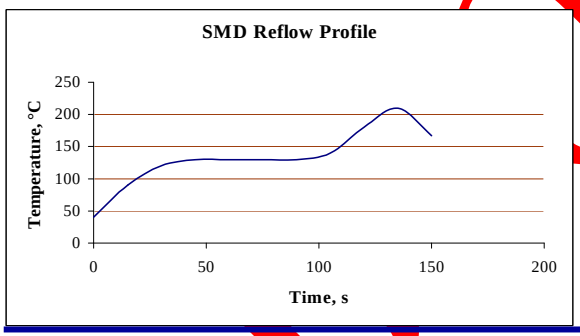
- **Small, Low Profile SMD Package**
- **Very Low Phase Jitter and Phase Noise**
- **Excellent Frequency Stability**
- **Low Aging, Vacuum sealed Crystal**
- **Ultra High Frequency – up to 1 GHz**
- **CMOS, Sine-Wave, or Differential PECL outputs available**



1.) Place R1 & R2 close to the output pads.
2.) C1 is a power supply decoupling capacotor.
3.) R3 is a potentiometer used for fine tuning the output frequency.







How to Order

VFT7H — [ ][ ][ ][ ] — **FREQUENCY, MHz**

Output Type

Code	Specification
C	CMOS
S	Sine-wave
E	PECL

Supply Voltage

Code	Specification
5	5V ±5%
3	3.3V ±5%

Temperature Range

Code	Specification
A	-10°C to 60°C
B	0°C to 70°C
C	-40°C to 85°C

Temp. Frequency Stability

Code	Specification
N	±2.5 ppm
S	±1.0 ppm

Specifications

Parameter	Symb	Condition	Min	Typ	Max	Unit	Note

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VFT7H Series

TCVCXO SMD High Frequency

Absolute Maximum Ratings

Input Break Down Voltage	Vcc		-0.5		5.5	V	
Storage temp.			-40		105	° C	
Contr. Voltage	Vc		-1		9	V	

Electrical

Frequency Range	F	CMOS Sine-wave PECL	30 30 30		160 250 1,000	MHz	
Input Voltage	Vcc		3.135 4.75	3.30 5.0	3.465 5.25	V	
Input Current	Icc	CMOS, Sine PECL			30 100	mA	@ 100 MHz, 3.3V @ 622 MHz, 3.3V
Frequency Stab.	ΔF/F	Overall			±4.6		
Frequency Stability	ΔF/F	vs. Temperature vs. Vcc aging		±0.5 ±0.1 ±1 ±3.5	±1	ppm ppm/V ppm/year ppm	 First Year 10 years
Calibration	ΔF/F	As shipped, 25ºC		±0.5	±1	ppm	
Load		CMOS Sine PECL	15pF/10KOhm AC-coupled 50 Ohm 50 Ohm to Vcc-2V or Thevenin equivalent				
Duty cycle		@50%	45	50	55	%	CMOS, PECL
Rise/Fall time	Tr/Tf	20 to 80 %		2 0.35		ns	CMOS PECL
Logic "1" level	Voh	CMOS	0.9Vcc			V	
Logic "0" level	Vol	CMOS			0.1Vcc	V	
Logic "1" level	Voh	PECL	Vcc-0.96		Vcc-0.81	V	100K available
Logic "0" level	Vol	PECL	Vcc-1.85		Vcc-1.65	V	100K available
Output power		Into 50 Ohm	0	7	10	dBm	Sinewave
Start up time				2	10	ms	
Phase jitter		1□		0.4	1	ps	fj>100 Hz
Subharmonics		PECL CMOS, Sine		-45	-40 none		F>250MHz
SSB Phase Noise		@10 Hz @100 Hz @1 KHz @10 KHz @100 KHz		-80 -110 -140 -150 -160		dBc/Hz	@100 MHz
SSB Phase Noise		@10 Hz @100 Hz @1 KHz @10 KHz @100 KHz		-60 -90 -120 -140 -145		dBc/Hz	@622 MHz
Input Impedance			> 10KOhm				
Control voltage	Vc		0		3.3	V	
Deviation		Vc=0V to 3.3V,25°C	±5	±7		ppm	

Environmental and Mechanical

Operating temp. range	0°C to 70°C , -40°C to 85°C
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Soldering Conditions	230°C for 30s Max
Hermetic Seal	Leak rate less than $5x10^{-8}$ atm.cc/s of helium (crystal only)

Electrical Connections

Pin Out	Pin #1- Voltage Control ; Pin #2 – N/C ; Pin #3 – Vcc; Pin#4– Output, CMOS, Sine or N/C; Pin#5 – PECL Output or N/C; Pin#6 – PECL Complementary Out or N/C; Pin #7– GND

OBSOLETE

Rev 12/08

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