

4789

#### Data Sheet

#### January 2000 File Number

## 1A, 600V Hyperfast Diode

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The RHR1K160 is a hyperfast diode with soft recovery characteristics ( $t_{rr}$  < 25ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

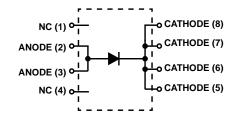
Formerly developmental type TA49185.

### **Ordering Information**

PART NUMBER	PACKAGE	BRAND	
RHR1K160	MS-012AA	RHR1K160	

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RHR1K16096.

# Symbol



# Features

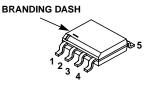
- Operating Temperature......150<sup>o</sup>C
- Thermal Impedance SPICE Model
- Thermal Impedance SABER™ Model
- Avalanche Energy Rated
- Planar Construction
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

## Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

## Packaging

#### JEDEC MS-012AA



UNITS

**RHR1K160** 

#### Absolute Maximum Ratings T<sub>A</sub> = 25°C, Unless Otherwise Specified

Peak Repetitive Reverse Voltage	600	V
Working Peak Reverse VoltageV <sub>RWM</sub>	600	V
DC Blocking VoltageV <sub>R</sub>	600	V
Average Rectified Forward Current	1	А
Repetitive Peak Surge CurrentI <sub>FRM</sub> Square Wave, 20kHz	2	А
Nonrepetitive Peak Surge CurrentI <sub>FSM</sub> Halfwave, 1 Phase, 60Hz	10	А
Maximum Power Dissipation (Note 1) P <sub>D</sub>	2.5	W
Avalanche Energy (See Figures 11 and 12)E <sub>AVL</sub>	5	mJ
Operating and Storage Temperature	-55 to 150	°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	300 260	°C °C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V <sub>F</sub>	I <sub>F</sub> = 1A	-	-	2.1	V
	$I_{F} = 1A, T_{A} = 150^{0}C$	-	-	1.7	V
I <sub>R</sub>	V <sub>R</sub> = 600V	-	-	100	μΑ
	$V_{R} = 600V, T_{A} = 150^{\circ}C$	-	-	500	μA
t <sub>rr</sub>	$I_{\rm F} = 1$ A, $dI_{\rm F}/dt = 200$ A/µs	-	-	25	ns
t <sub>a</sub>	$I_F = 1A$ , $dI_F/dt = 200A/\mu s$	-	10.5	-	ns
t <sub>b</sub>	$I_F = 1A$ , $dI_F/dt = 200A/\mu s$	-	5	-	ns
Q <sub>RR</sub>	$I_F = 1A$ , $dI_F/dt = 200A/\mu s$	-	20	-	nC
CJ	V <sub>R</sub> = 10V, I <sub>F</sub> = 0A	-	10	-	pF
R <sub>θJA</sub>	Pad Area = $0.769 \text{ in}^2$ (Note 1)	-	-	50	°C/W
	Pad Area = 0.054 in <sup>2</sup> (Note 2) (Figure 13)	-	-	177	°C/W
	Pad Area = 0.0115 in <sup>2</sup> (Note 2) (Figure 13)	-	-	217	°C/W

## **Electrical Specifications** $T_A = 25^{\circ}C$ , Unless Otherwise Specified

DEFINITIONS

 $V_F$  = Instantaneous forward voltage (pw = 300µs, D = 2%).

 $I_R$  = Instantaneous reverse current.

 $t_{rr}$  = Reverse recovery time (See Figure 10), summation of  $t_a$  +  $t_b$ .

 $t_a$  = Time to reach peak reverse current (See Figure 10).

 $t_b$  = Time from peak  $I_{RM}$  to projected zero crossing of  $I_{RM}$  based on a straight line from peak  $I_{RM}$  through 25% of  $I_{RM}$  (See Figure 10).

 $Q_{rr}$  = Reverse recovery charge.

C<sub>J</sub> = Junction Capacitance.

 $R_{\theta JA}$  = Thermal resistance junction to ambient.

pw = Pulse width.

D = Duty cycle.

NOTES:

1. Measured using FR-4 copper board at 3.2 seconds.

2. Measured using FR-4 copper board at 1000 seconds.

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# **Typical Performance Curves**

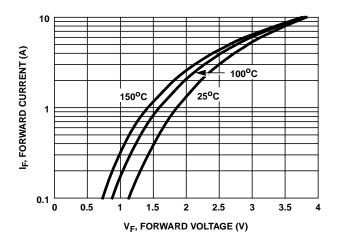


FIGURE 1. FORWARD CURRENT vs FORWARD VOLTAGE

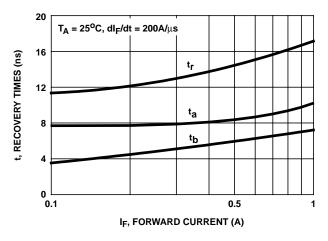
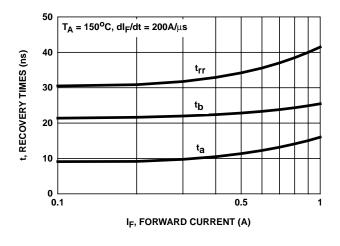


FIGURE 3.  $t_{rr}$ ,  $t_a$  AND  $t_b$  CURVES vs FORWARD CURRENT





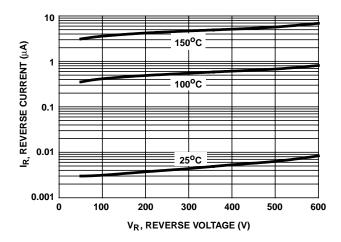


FIGURE 2. REVERSE CURRENT vs REVERSE VOLTAGE

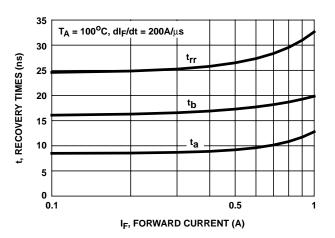


FIGURE 4. trr, ta AND tb CURVES vs FORWARD CURRENT

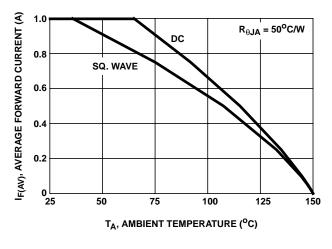
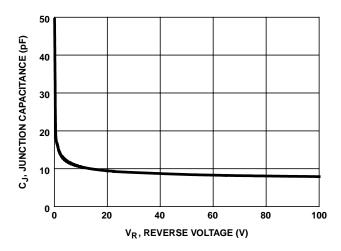


FIGURE 6. CURRENT DERATING CURVE

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### Typical Performance Curves (Continued)





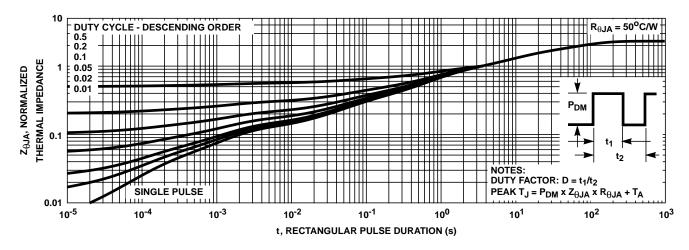


FIGURE 8. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE



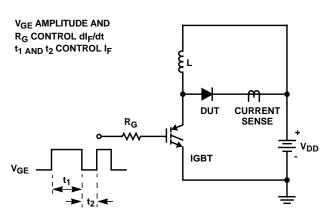


FIGURE 9. trr TEST CIRCUIT

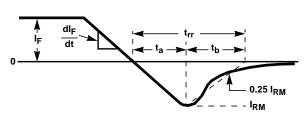


FIGURE 10. trr WAVEFORMS AND DEFINITIONS

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#### Test Circuits and Waveforms (Continued)

$$\begin{split} & L = 20 mH \\ & R < 0.1 \Omega \\ & E_{AVL} = 1/2 LI^2 \left[ V_{R(AVL)} / (V_{R(AVL)} - V_{DD}) \right] \\ & \alpha_1 = IGBT \left( BV_{CES} > DUT \; V_{R(AVL)} \right) \end{split}$$

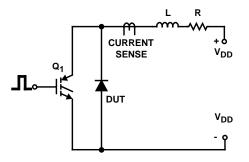


FIGURE 11. AVALANCHE ENERGY TEST CIRCUIT

#### Thermal Resistance vs Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  (<sup>o</sup>C), and thermal resistance  $R_{\theta JA}$  (<sup>o</sup>C/W) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}}$$
(EQ. 1)

In using surface mount devices such as the SO-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of the P<sub>DM</sub> is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- 2. The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- 6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Intersil provides thermal information to assist the designer's preliminary application evaluation. Figure 13 defines the R<sub>0JA</sub> for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 2 oz. copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state

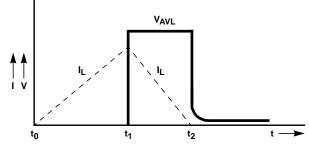
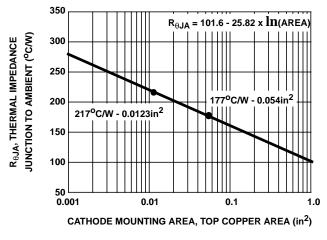


FIGURE 12. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

junction temperature or power dissipation. Pulse applications can be evaluated using the Intersil device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.





Displayed on the curve are  $R_{\theta JA}$  values listed in the Electrical Specifications table. These points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation,  $P_{DM}$ . Thermal resistances corresponding to other component side copper areas can be obtained from Figure 13 or by calculation using Equation 2. The area, in square inches is the top copper area including the cathode pad area.

$$R_{\theta JA} = 101.6 - 25.82 \times ln(Area)$$
 (EQ. 2)

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The transient thermal impedance ( $Z_{\theta JA}$ ) is also effected by various top copper board areas. Figure 14 shows the effect of copper pad area on the single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM4 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

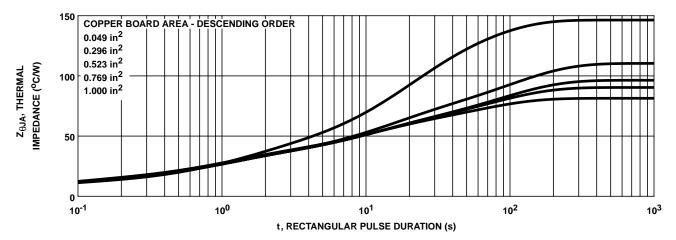


FIGURE 14. TRANSIENT THERMAL IMPEDANCE vs MOUNTING PAD AREA

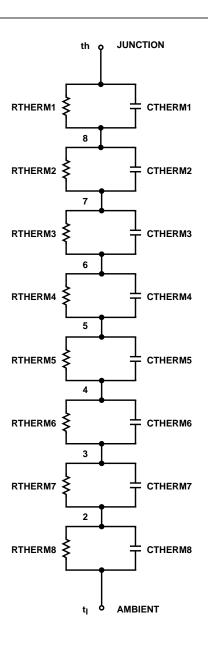
## SPICE Thermal Model

REV August 1998 RHR1K160 Copper Area = 0.769 in<sup>2</sup> CTHERM1 th 8 5e-6 CTHERM2 8 7 2.5e-5 CTHERM3 7 6 1.2e-4 CTHERM4 6 5 4.5e-4 CTHERM5 5 4 9e-3 CTHERM5 4 3 4.5e-2 CTHERM7 3 2 3.5e-1 CTHERM8 2 tl 2

RTHERM1 th 8 4e-2 RTHERM2 8 7 1.6e-1 RTHERM3 7 6 1 RTHERM4 6 5 3.2 RTHERM5 5 4 6 RTHERM6 4 3 19 RTHERM7 3 2 25 RTHERM8 2 tl 36

# SABER Thermal Model

Copper Area =  $0.769 \text{ in}^2$ template thermal\_model th tl thermal\_c th, tl ctherm.ctherm1 th 8 = 5e-6ctherm.ctherm2 8 7 = 2.5e-5 ctherm.ctherm3 7 6 = 1.2e-4 ctherm.ctherm4 6 5 = 4.5e-4ctherm.ctherm5 5 4 = 9e-3 ctherm.ctherm6 4 3 = 4.5e-2 ctherm.ctherm7 3 2 = 3.5e-1 ctherm.ctherm8 2 tl = 2 rtherm.rtherm1 th 8 = 4e-2rtherm.rtherm2 8 7 = 1.6e-1 rtherm.rtherm3 7 6 = 1 rtherm.rtherm4 6 5 = 3.2 rtherm.rtherm554 = 6rtherm.rtherm6 4 3 = 19 rtherm.rtherm7 32 = 25rtherm.rtherm8 2 tl = 36



#### TABLE 1. THERMAL MODELS

COMPONENT	0.049 in <sup>2</sup>	0.296 in <sup>2</sup>	0.523 in <sup>2</sup>	0.769 in <sup>2</sup>	1.0 in <sup>2</sup>
CTHERM6	5e-2	4.5e-2	4.5e-2	4.5e-2	4.5e-2
CTHERM7	2.5e-1	3.5e-1	3.5e-1	3.5e-1	3.5e-1
CTHERM8	1	2	2	2	2
RTHERM5	5	6	6	6	7
RTHERM6	22	19	19	19	19
RTHERM7	60	32	25	25	23
RTHERM8	55	49	42	36	28

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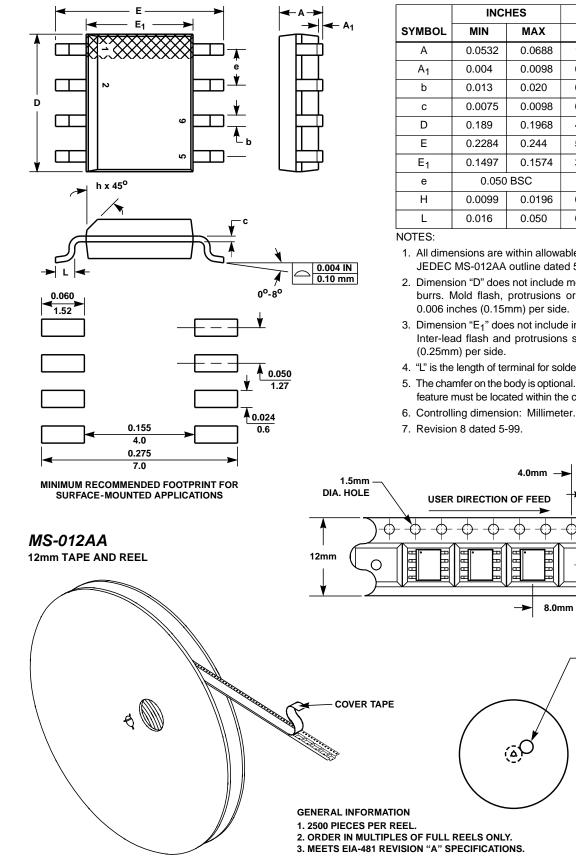
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# **MS-012AA**

8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE



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	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A <sub>1</sub>	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
с	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E <sub>1</sub>	0.1497	0.1574	3.80	4.00	3
е	0.050 BSC		1.27 BSC		-
Н	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

- 1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
- 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
- 3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches
- 4. "L" is the length of terminal for soldering.
- 5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

2.0mm

4

40mm MIN. ACCESS HOLE

330mm

->

1.75mm

ዊ

🗕 18.4mm

13mm

🗲 12.4mm

50mm

6. Controlling dimension: Millimeter.