Features

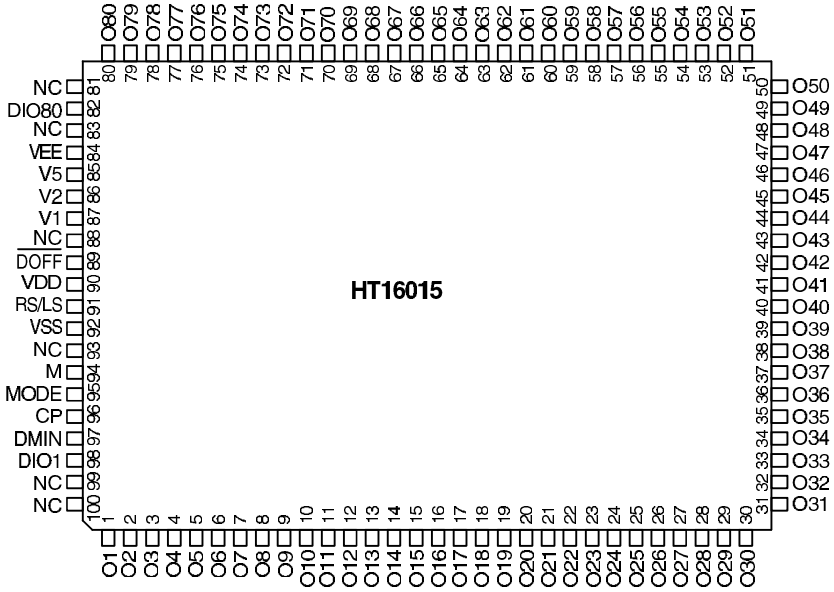
- 80 dot matrix LCD common signal driver
- Power supply for logic circuit from 2.7V to 5.5V
- VLCD Operating voltage: 10V~30V (V_{DD}~V_{EE})
- Application LCD duty selection from 1/64 to 1/256
- Internal 80-bits shift register
- Bias voltage adjustable from external source
- Provide single mode and dual mode applications such as:
  - Single mode
    O1 → O80
    O80 → O1
  - Dual mode
    O1 → O40 and O41 → O80
    O80 → O41 and O40 → O1
- CMOS process
- Pin Compatible with 79430D

General Description

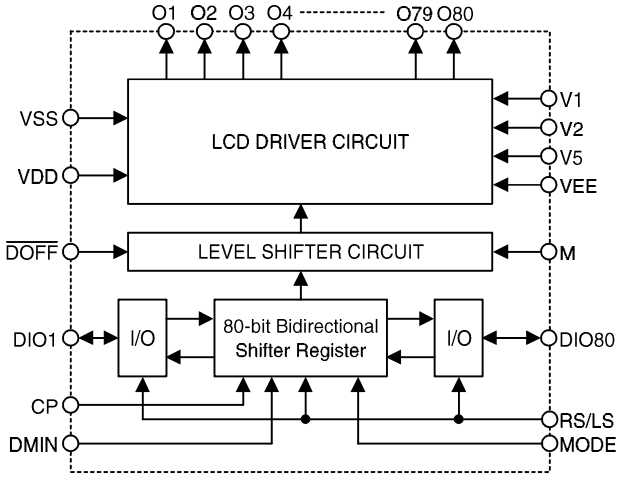
The HT16015 is a dot matrix LCD's common driver LSI implemented in CMOS technology. The HT16015 contains an 80-bit bidirectional shift register, 80-bit level shifter, 80-bit 4-level driver and control circuit.

Therefore the HT16015 can convert serial data recived from LCD controller parallel data and then send out LCD driving waveforms to the LCD panel. The HT16015 is applicable up to 1/256 duty. Furthermore, the bias voltage can be optionally supplied from the external source, and thus the chip can be suitable for driving various LCD panel. With the special function makes the HT1605 more versatile.

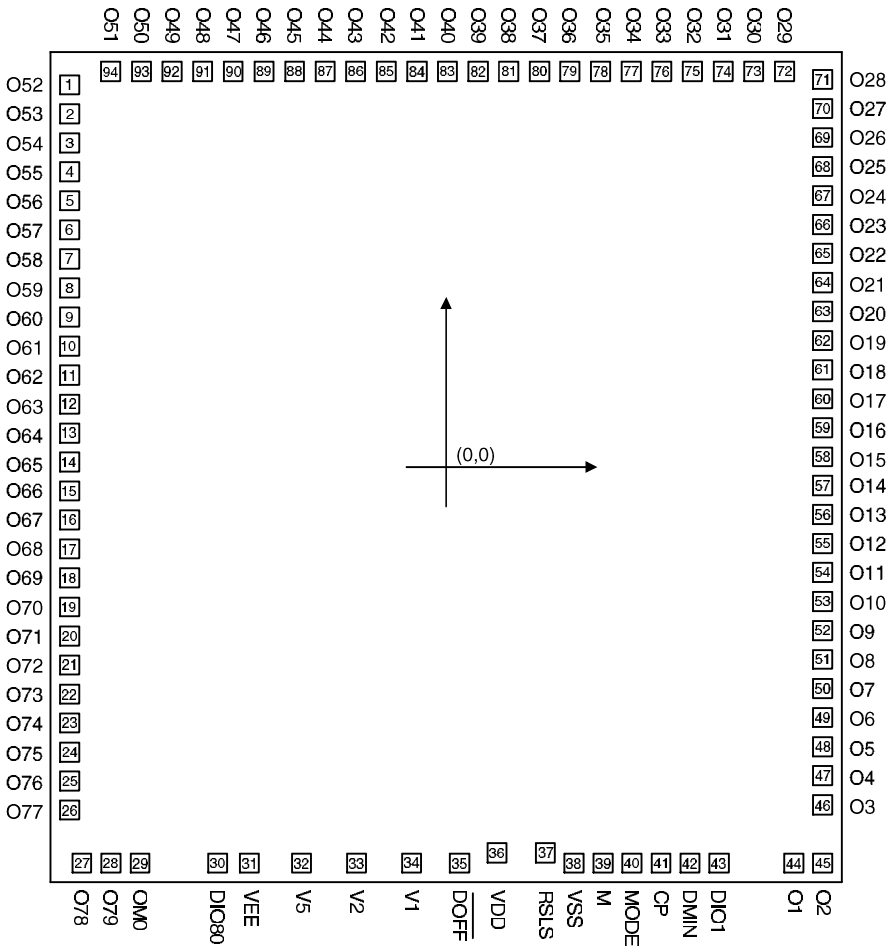
Pin Assignment



Block Diagram



Pad Assignment



Chip size: 3760×4060 $(\mu m)^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1752.00	1779.25	48	1752.00	–1300.25
2	–1752.00	1644.25	49	1752.00	–1165.25
3	–1752.00	1509.25	50	1752.00	–1030.25
4	–1752.00	1374.25	51	1752.00	–895.25
5	–1752.00	1239.25	52	1752.00	–760.25
6	–1752.00	1104.25	53	1752.00	–625.25
7	–1752.00	969.25	54	1752.00	–490.25
8	–1752.00	834.25	55	1752.00	–355.25
9	–1752.00	699.25	56	1752.00	–220.25
10	–1752.00	564.25	57	1752.00	–85.25
11	–1752.00	429.25	58	1752.00	49.75
12	–1752.00	294.25	59	1752.00	184.75
13	–1752.00	159.25	60	1752.00	319.75
14	–1752.00	24.25	61	1752.00	454.75
15	–1752.00	–110.75	62	1752.00	589.75
16	–1752.00	–245.75	63	1752.00	724.75
17	–1752.00	–380.75	64	1752.00	859.75
18	–1752.00	–515.75	65	1752.00	994.75
19	–1752.00	–650.75	66	1752.00	1129.75
20	–1752.00	–785.75	67	1752.00	1264.75
21	–1752.00	–920.75	68	1752.00	1399.75
22	–1752.00	–1055.75	69	1752.00	1534.75
23	–1752.00	–1190.75	70	1752.00	1669.75
24	–1752.00	–1325.75	71	1752.00	1804.75
25	–1752.00	–1460.75	72	1574.00	1842.75
26	–1752.00	–1595.75	73	1431.50	1842.75
27	–1695.00	–1842.75	74	1289.00	1842.75
28	–1560.00	–1842.75	75	1146.50	1842.75
29	–1425.00	–1842.75	76	1004.00	1842.75
30	–1064.00	–1842.75	77	861.50	1842.75
31	–916.00	–1842.75	78	719.00	1842.75
32	–673.50	–1842.75	79	576.50	1842.75
33	–417.00	–1842.75	80	434.00	1842.75
34	–161.50	–1842.75	81	291.50	1842.75
35	64.00	–1842.75	82	149.00	1842.75
36	237.0	–1793.25	83	6.50	1842.75
37	462.50	–1793.25	84	–136.00	1842.75
38	595.50	–1842.75	85	–278.50	1842.75
39	730.50	–1842.75	86	–421.00	1842.75
40	865.50	–1842.75	87	–563.50	1842.75
41	1000.50	–1842.75	88	–706.00	1842.75
42	1135.50	–1842.75	89	–848.50	1842.75
43	1270.50	–1842.75	90	–991.00	1842.75
44	1617.00	–1842.75	91	–1133.50	1842.75
45	1752.00	–1842.75	92	–1276.00	1842.75
46	1752.00	–1570.25	93	–1418.50	1842.75
47	1752.00	–1435.25	94	–1561.00	1842.75

Pad Description

Pad No.	Pad Name	I/O	Function
1~80	O1~O80	O	LCD driver output for common signal
81,83, 88,93, 99,100	N.C.	I/O	No connected
82	DIO80	P	Bidirection data pin
84 85 86 87	VEE V1 V2 V5	I	Power supply for LCD driver level V1 and VEE: Select level V2 and V5: Non-select level
89	$\overline{\text{DOFF}}$	I	LCD driver output control
90	VDD	P	Power supply for logic circuit
91	RS/LS	I	Bidirectional shift register shift control pin
92	VSS	P	Power supply for logic circuit (negative)
94	M	I	Alternate signal input pad for LCD driving waveform
95	MODE	I	Single or dual mode control pin
96	CP	I	Clock pulse input pad for the shift register
97	DMIN	I	Dual mode data input pin
98	DIO1	I/O	Bidirection data pin

Note:

Data shift direction control table:

MODE	RS/LS	Data Shift Direction	DIO1	DIO80	DMIN
L (Single)	L (Right)	O1~O80	IN	OUT	Don't care
	H (Left)	O80~O1	OUT	IN	Don't care
H (Dual)	L (Right)	O1~O40 O41~O80	IN	OUT	IN
	H (Left)	O80~O41 O40~O1	OUT	IN	IN

LCD drive output control table:

M	DATA	$\overline{\text{DOFF}}$	OUTPUT
L	L	H	V2
L	H	H	VEE
H	L	H	V5
H	H	H	V1
Don't care	Don't care	L	V1

Absolute Maximum Ratings

Supply Voltage ..... –0.3V~6.5V
Input Voltage ..... V_{SS}–0.3V~V_{DD}+0.3V
Storage Temperature ..... –40°C~125°C
Operating Temperature ..... –20°C~75°C

DC Characteristics (Condition at Ta=–20 to 75°C, V_{SS}=0V)

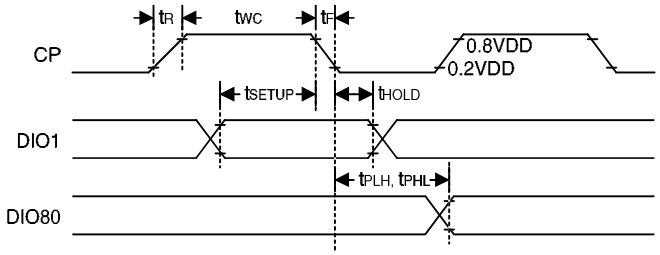
Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.7	—	5.5	V
*1 V_{DD}~V_{EE}	Operating Voltage (LCD)	—	—	12	—	30	V
V_{IH}	Input “H” level voltage	5V	(DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{DOFF}$)	0.8V_{DD}	—	—	V
V_{IL}	Input “L” level voltage	5V	(DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{DOFF}$)	—	—	0.2V_{DD}	V
I_{IH}	Input “H” level current	5V	(DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{DOFF}$)	—	—	1	μA
I_{IL}	Input “L” level current	5V	(DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{DOFF}$)	–1	—	—	μA
V_{OH}	Output “H” level voltage	5V	IOH=–0.4mA, DIO1, DIO80	V_{DD}–0.4	—	—	V
V_{IL}	Output “L” level voltage	5V	IOH=–0.4mA, DIO1, DIO80	—	—	0.4	V
R_{on}	Driver on resistor	5V	O1 to O80, V_{DD}~V_{EE}=30V, $\lvert^{*1}V_{LCD}-V_O\rvert$=0.5V	—	—	1.0	kΩ

*1 The following relation between elements should be maintained:
$V_{DD}\geq V1>V2>V5>V_{EE}$, V_{DD}–V1≤7V, V5–VEE≤7V.

AC Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=5V±10%

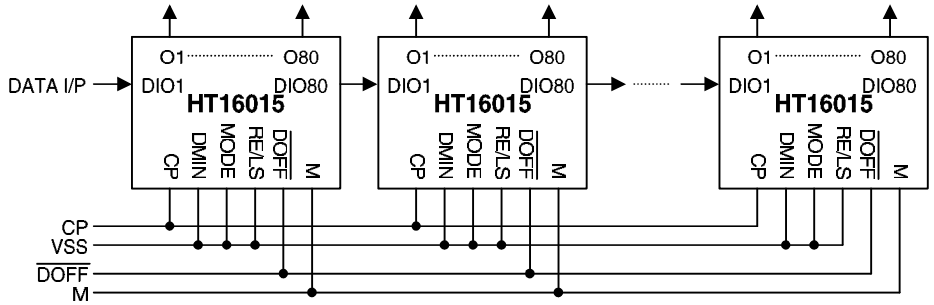
Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
I_{VSS}	Power consumption (1)	5V	V_{DD}~V_{EE}=30V, CP=14KHz, No load, V_{SS}	—	—	100	μA
V_{EE}	Power consumption (2)	5V	VDD~V_{EE}=30V, CP=14KHz, LOAD=14KHz, V_{EE}	—	—	100	μA
C_I	Input capacity	5V	*1	—	5	—	pF
t_{SETUP}	Setup time	5V	*1	30	—	—	ns
t_{HOLD}	Hold time	5V	*1	30	—	—	ns
t_R	CP rise time	5V	*1	—	—	50	ns
t_F	CP fall time	5V	*1	—	—	50	ns
f_{CP}	CP (Shift clock)	5V	*1	—	—	1	MHz
t_{PW}	CP (Pulse width)	5V	*1	60	—	—	ns
t_{PLH}	Output delay time	5V	*1 CL=15pF	—	—	250	ns
t_{PHL}	Output delay time	5V	*1 CL=15pF	—	—	250	ns

*1

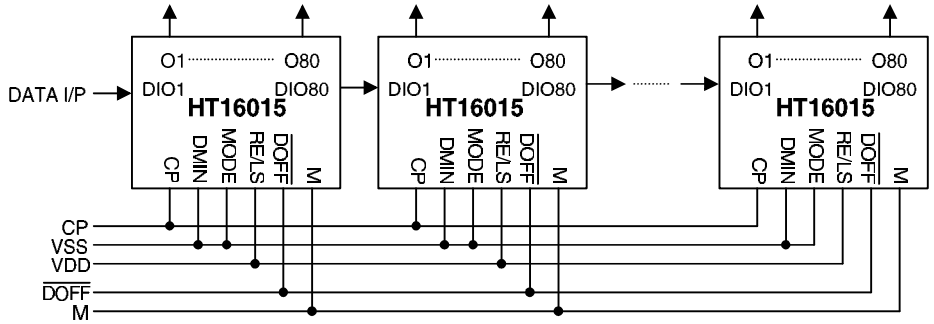


Application Diagram

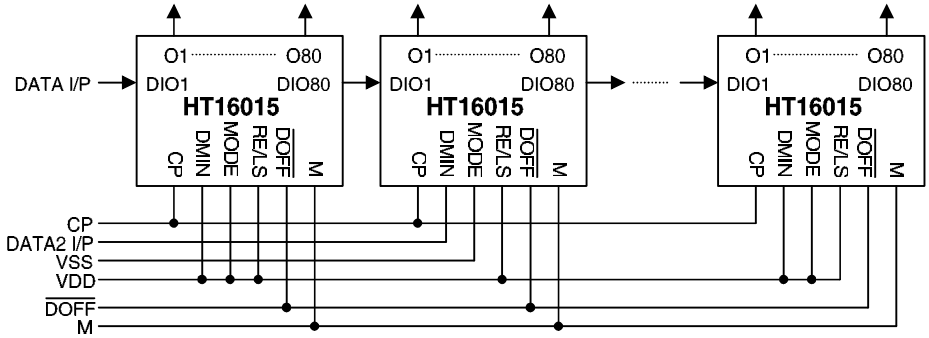
Single Mode-Right Shift



Single Mode-Left Shift



Dual Mode-Right Shift



Dual Mode-Left Shift